ADVANCE INFORMATION

CY62126DV30 MoBL®

64K x 16 Static RAM

Features

- **High speed: 55 ns**
- **Wide voltage range: 2.2V–3.6V**
- **Pin Compatible with CY62126BV**
- **Ultra-low active power**
  - **Typical active current: 0.5 mA @ f = 1MHz**
  - **Typical active current: 5 mA @ f = f_{max}**
- **Low standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in 44-lead TSOP Type II and 48-ball FBGA packages**

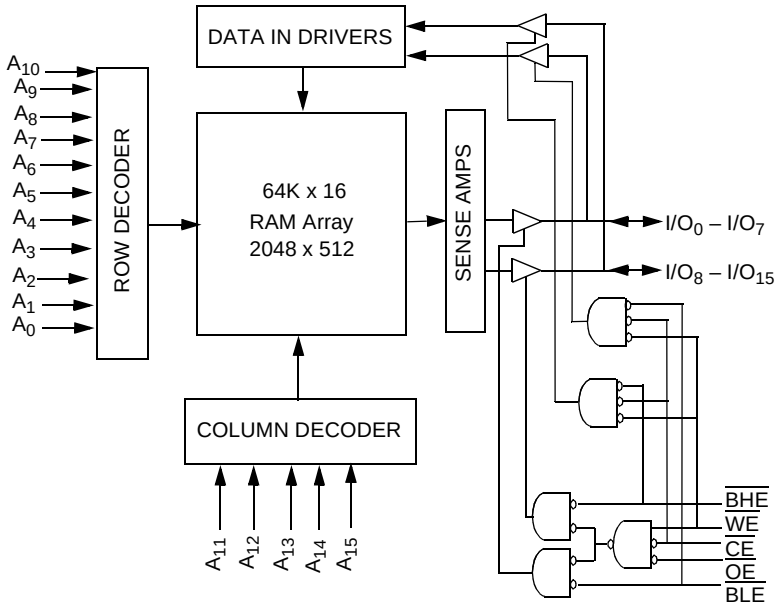
Functional Description[1]

The CY62126DV30 is a high-performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the Truth Table near the back of this data sheet for a complete description of read and write modes.

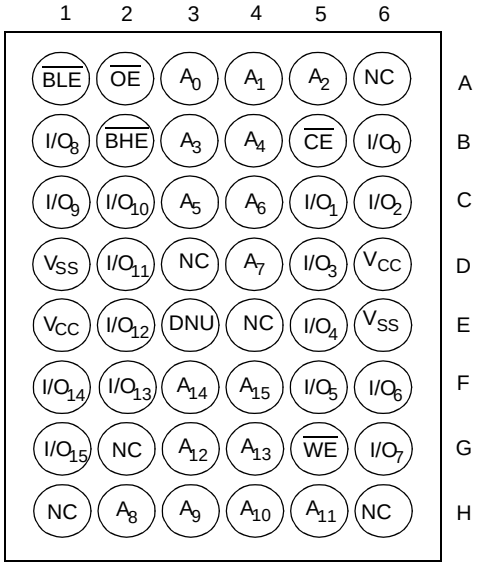
Logic Block Diagram



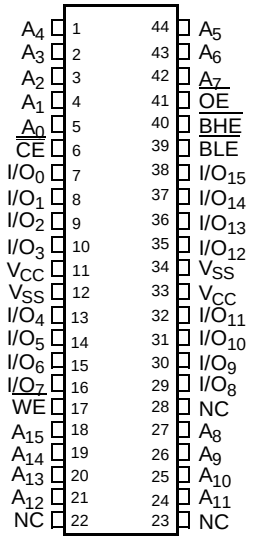
Note:
1. For best practice recommendations, please refer to the Cypress application note 'System Design Guidelines' on http://www.cypress.com

Pin Configurations[2, 3]

FBGA (Top View)



TSOP II (Forward) Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential ... –0.3V to V_{ccmax} + 0.3V

DC Voltage Applied to Outputs in High Z State[5]..... –0.3V to V_{CC} + 0.3V

DC Input Voltage[5] ..... –0.3V to V_{CC} + 0.3V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}[4]
Industrial	–40°C to +85°C	2.2V to 3.6V

Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating, I_{CC} (mA)				Standby, I_{SB2} (µA)	
					f = 1 MHz		f = f_{max}			
	Min.	Typ.[6]	Max.		Typ.[6]	Max.	Typ.[6]	Max.	Typ.[6]	Max.
CY62126DV30L	2.2	3.0	3.6	55	0.5	1	5	10	1.5	4
CY62126DV30LL										3

Notes:
2. NC pins are not connected to the die.
3. E3 (DNU) can be left as NC or V_{SS} to ensure proper application.
4. Full Device AC operation requires linear V_{CC} ramp from 0 to $V_{CC(min.)} \geq 500\mu s$.
5. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62126DV30-55			Unit
					Min.	Typ.[6]	Max.	
V_{OH}	Output HIGH Voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH}= –0.1 mA		2			V
		$2.7 \le V_{CC} \le 3.6$	I_{OH}= –1.0 mA		2.4			
V_{OL}	Output LOW Voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL}= 0.1 mA				0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OL}= 2.1 mA				0.4	
V_{IH}	Input HIGH Voltage	$2.2 \le V_{CC} \le 2.7$			1.8		V_{CC} + 0.3V	V
		$2.7 \le V_{CC} \le 3.6$			2.2			
V_{IL}	Input LOW Voltage	$2.2 \le V_{CC} \le 2.7$			–0.3		0.6	V
		$2.7 \le V_{CC} \le 3.6$					0.8	
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$			-1		+1	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled			-1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	V_{CC} = 3.6V Iout = 0mA CMOS level			5	10	mA
		f = 1 MHz				0.5	1	
I_{SB1}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \ge V_{CC} - 0.2V$ $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, $f = f_{max}$ (Address and Data Only),f=0 (OE,WE,BHE and BLE)		L		1.5	4	µA
				LL			3	
I_{SB2}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \ge V_{CC} - 0.2V$ $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, f = 0, Vcc=3.6V		L		1.5	4	µA
				LL			3	

Capacitance[7]

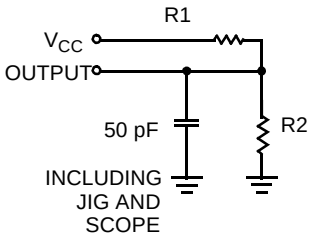
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

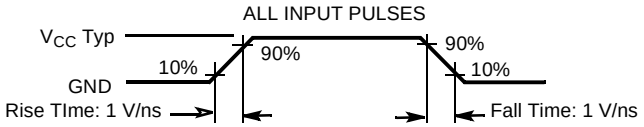
Thermal Resistance

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient)[7]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ_{JA}	55	°C/W
Thermal Resistance (Junction to Case)[7]		Θ_{JC}	16	°C/W

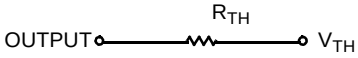
Note:
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT

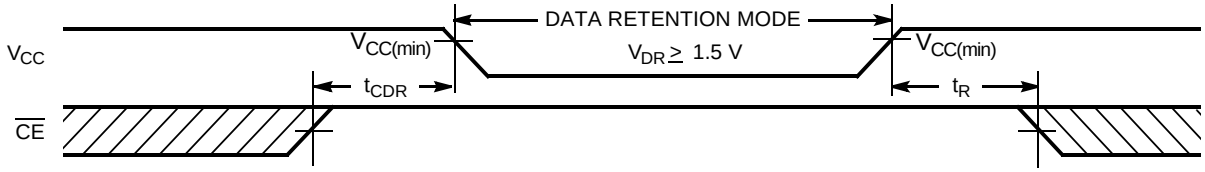


Parameters	2.5V	3.0V	Unit
R1	16600	1216	Ohms
R2	15400	1374	Ohms
R_{TH}	8000	645	Ohms
V_{TH}	1.2	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ.[6]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.5			V
I_{CCDR}	Data Retention Current	V_{CC}= 1.5V $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L			1.2	µA
			LL			0.8	
t_{CDR}[7]	Chip Deselect to Data Retention Time			0			ns
t_R[8]	Operation Recovery Time			100			µs

Data Retention Waveform



Note:
8. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)}$ > 100µs.

Switching Characteristics Over the Operating Range[9]

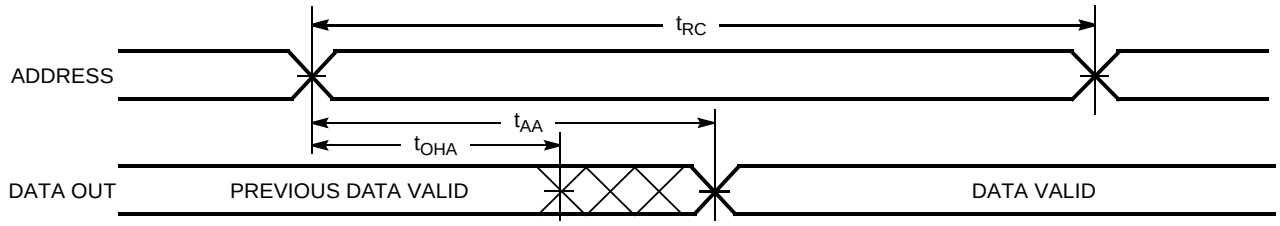
Parameter	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	55		ns
t_{AA}	Address to Data Valid		55	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[10]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[10, 11]		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[10]	10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[10, 11]		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		55	ns
t_{DBE}	$\overline{BHE}$/$\overline{BLE}$ LOW to Data Valid		25	ns
t_{LZBE}	$\overline{BHE}$/$\overline{BLE}$ LOW to Low Z	5		ns
t_{HZBE}	$\overline{BHE}$/$\overline{BLE}$ HIGH to High Z		20	ns
Write Cycle[12]				
t_{WC}	Write Cycle Time	55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	45		ns
t_{AW}	Address Set-Up to Write End	45		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	45		ns
t_{BW}	$\overline{BHE}$/$\overline{BLE}$ Pulse Width	50		ns
t_{SD}	Data Set-Up to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[10, 11]		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[10]	5		ns

Notes:

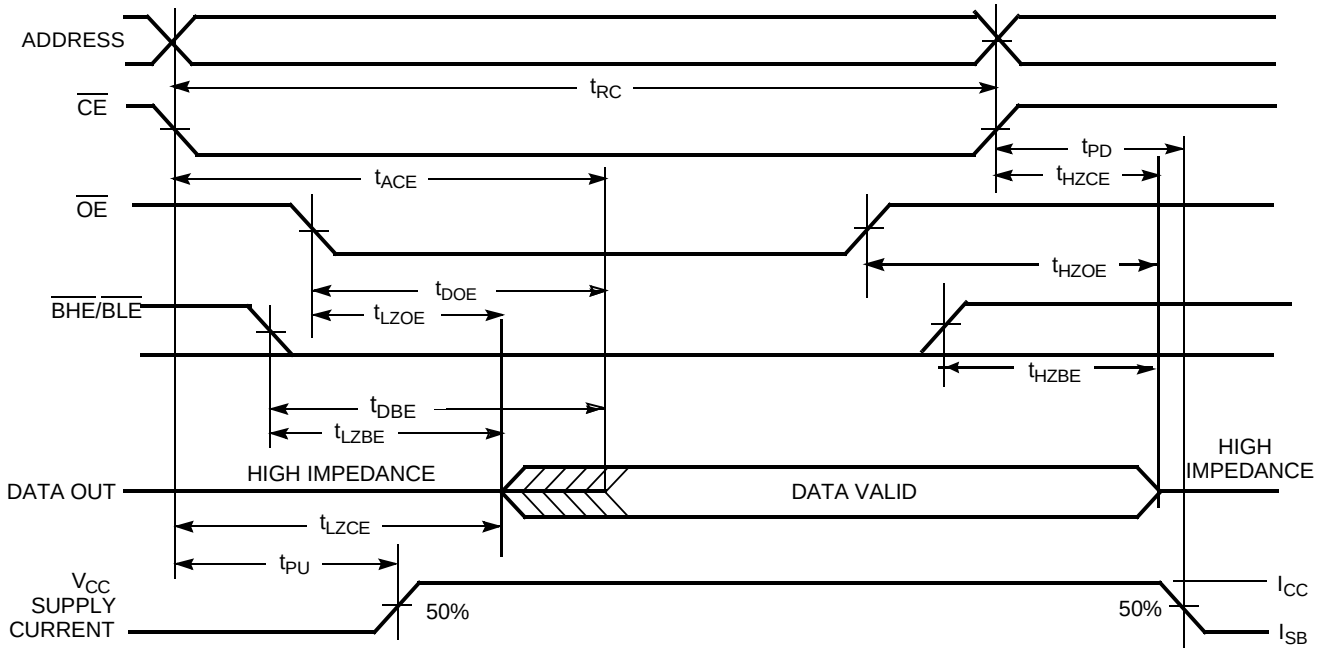
9. Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
11. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
12. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)[13, 14]



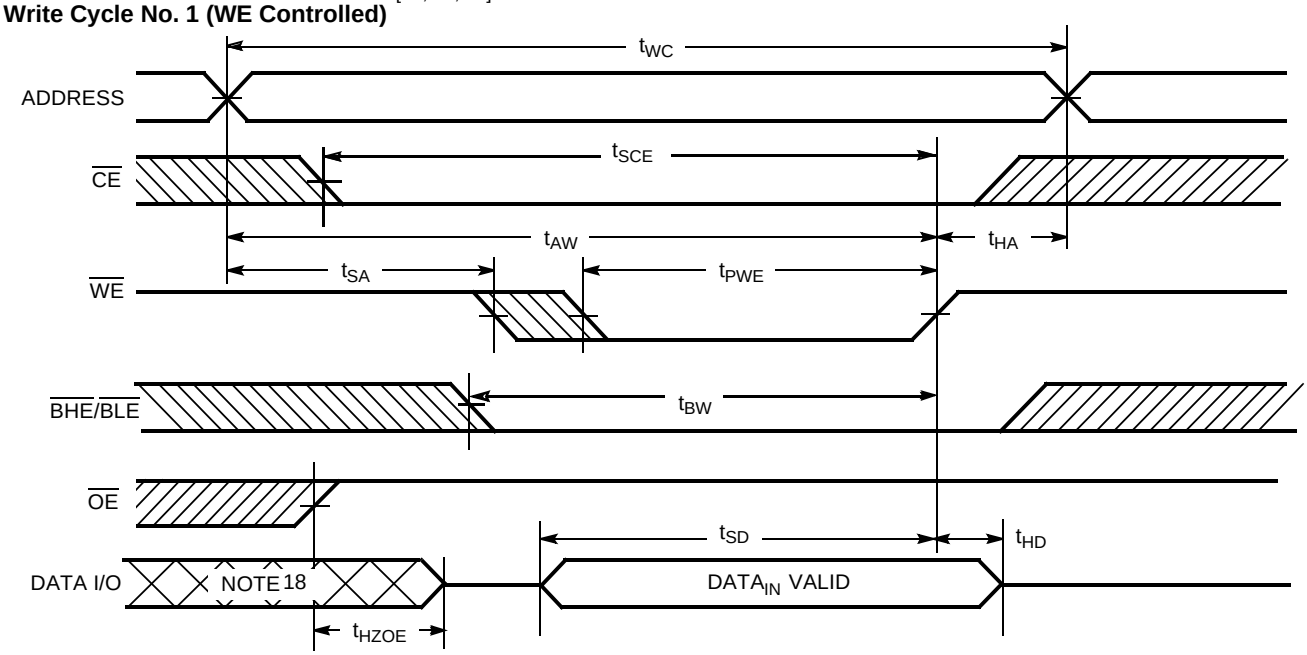
Read Cycle No. 2 ($\overline{OE}$ Controlled)[14, 15]



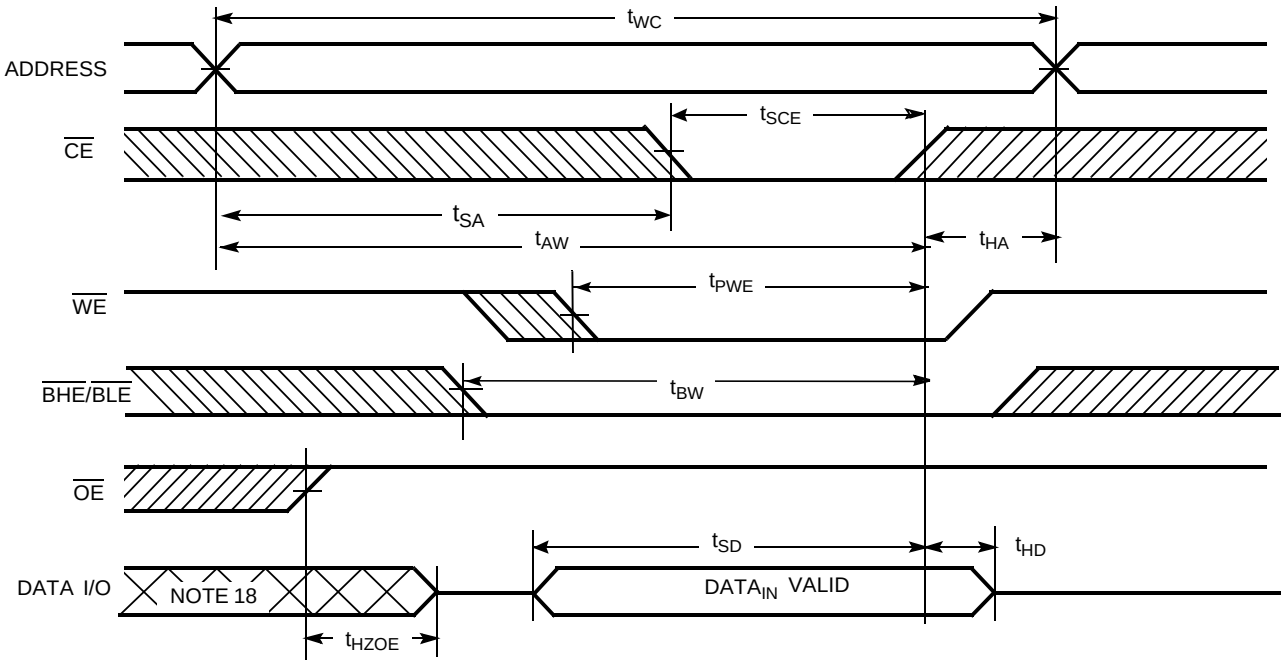
Notes:
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ = V_{IL}.
14. $\overline{WE}$ is HIGH for read cycle.
15. Address valid prior to or coincident with $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled) [12, 16, 17]



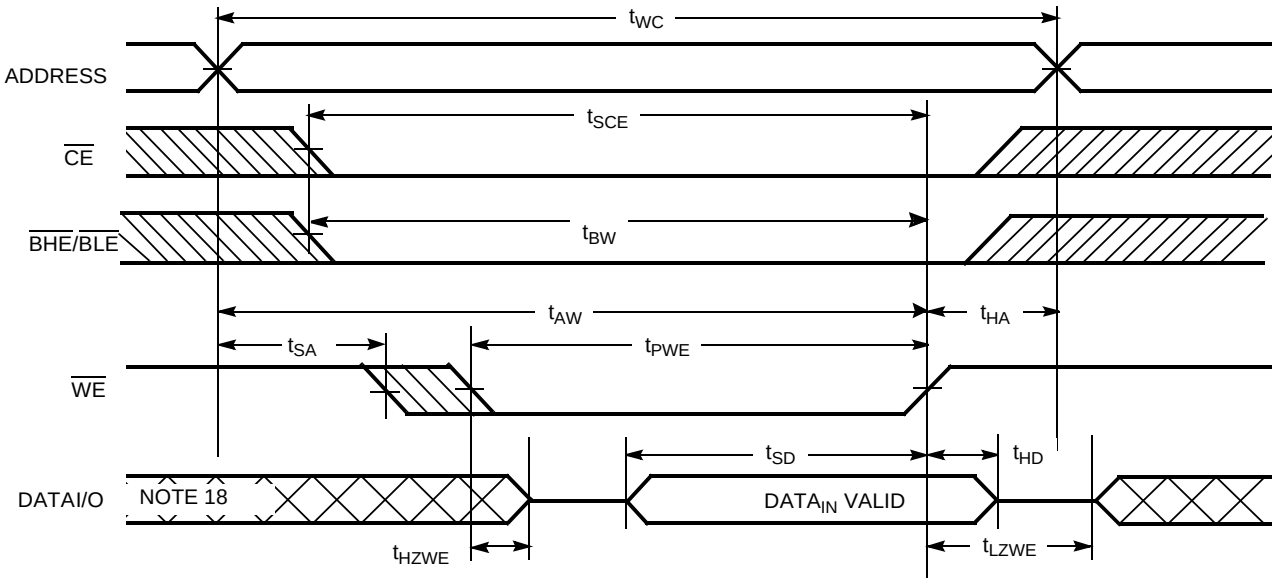
Write Cycle No. 2 ($\overline{CE}$ Controlled) [12, 16, 17]



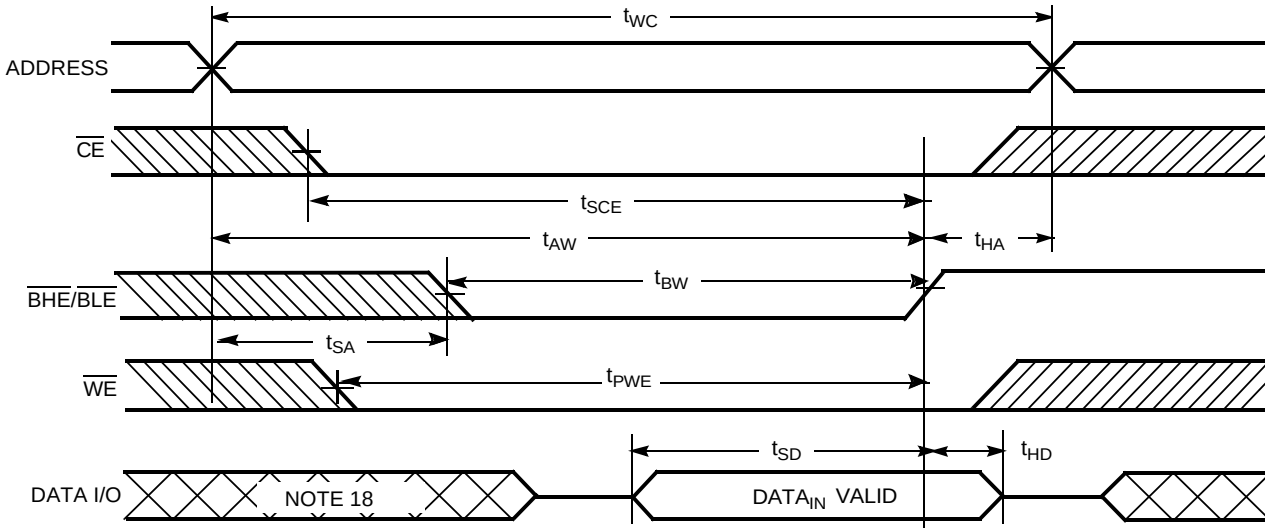
Notes:
16. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
18. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 (WE Controlled, OE LOW) [17]



Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [17]



Truth Table

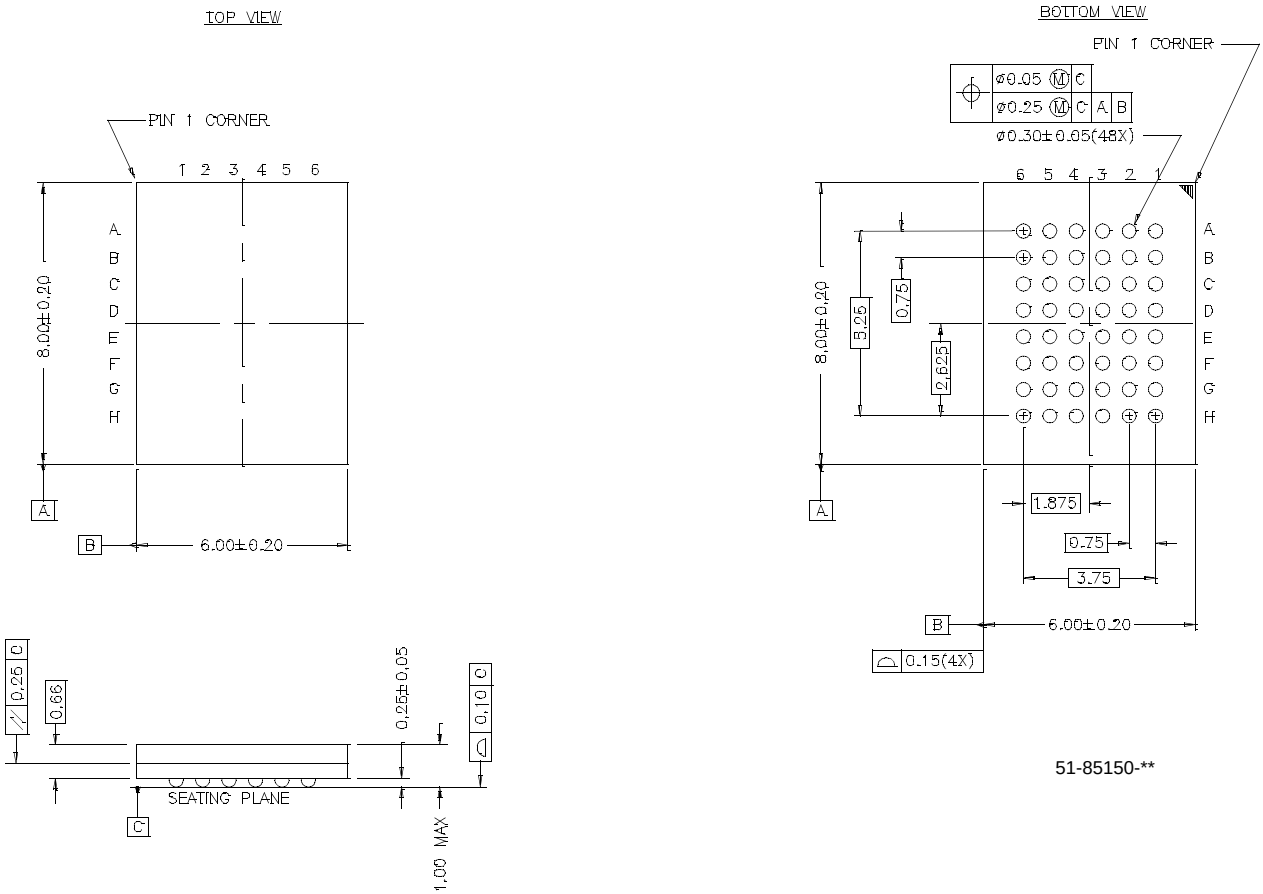
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	X	X	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	L	L	Data Out (I/O_O–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_O–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62126DV30L-55ZI	Z44	44-Lead TSOP II	Industrial
	CY62126DV30LL-55ZI			
	CY62126DV30L-55BAI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62126DV30LL-55BAI			

Package Diagrams

48-Lead VFBGA (6 x 8 x 1 mm) BV48A



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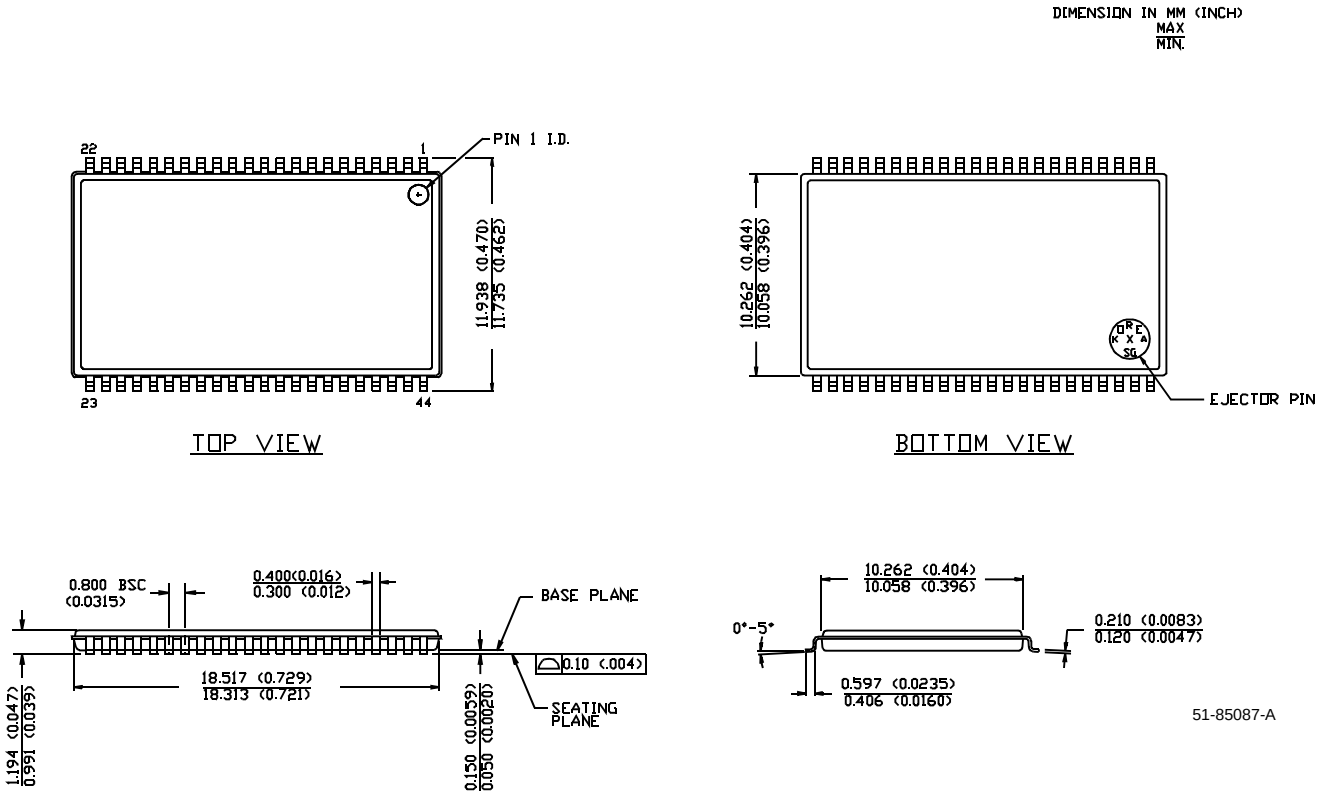
Package Diagrams (continued)

44-Pin TSOP II Z44



Document Title: CY62126DV30 MoBL® 64K x 16 Static RAM Document Number:38-05230				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	117689	08/27/02	JUI	New Data Sheet