MX·COM, INC.

MX214
MX224

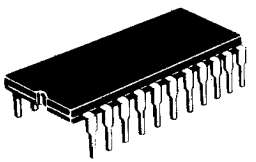
VARIABLE SPLIT BAND INVERTER

FEATURES:

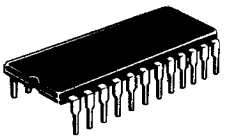
- CTCSS Highpass Filter
- Good Recovered Audio Quality
- Fixed and Rolling Code Modes
- Serial/Parallel Loading Options
- 32 Programmable Split Points
- Half-Duplex Capability

APPLICATIONS:

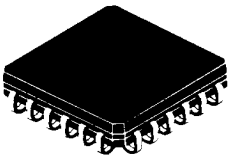
- Mobile Radio Voice Security
- Cellular Telephone Voice Security



MX214J (CDIP)
MX214P (PDIP)
22 pins



MX224J (CDIP)
MX224P (PDIP)
24 pins



MX214LH
MX224LH
(24p PLCC)

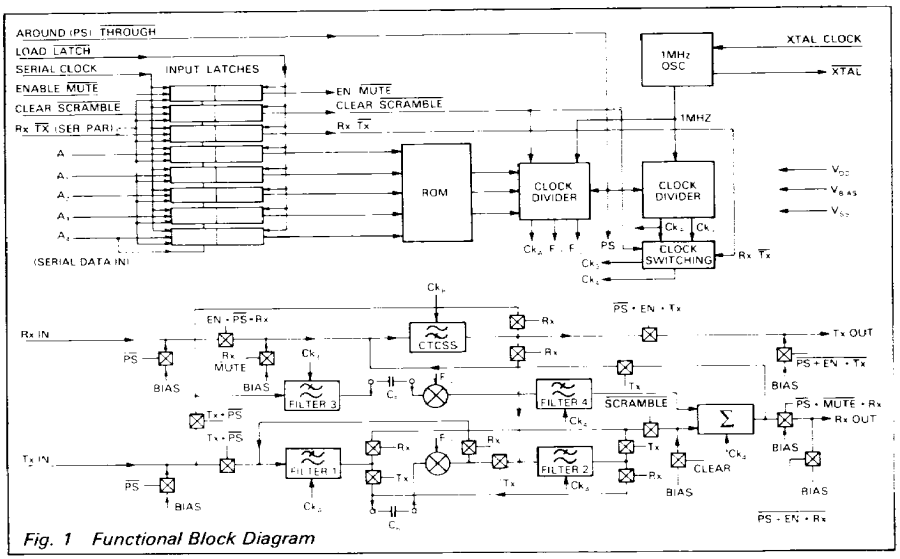


Fig. 1 Functional Block Diagram

DESCRIPTION:

The MX214/MX224 Variable Split Band Inverters are designed for mobile and cellular radio voice security applications. Digital control functions are loaded serially into the MX214. The MX224 is loaded in parallel.

The MX214/MX224 ICs include a highpass filter which rejects subaudio frequencies, ensuring full CTCSS compatibility. This CTCSS filter is not included on the earlier-generation MX204 VSB Inverter.

The MX214/ MX224 splits the voiceband (300-2700 Hz) into upper and lower subbands, and inverts each subband about itself. The "split point" (defined as the frequency where the voice band is subdivided), is externally programmable to 32 distinct values in the 300 to 3000 Hz range. In the "fixed code" mode, a single split point is used. Fixed mode operation nets approximately 4 mutually exclusive voice channels.

In "rolling code" mode, the split point is changed many times per second, usually under control of a microprocessor. Rolling code scrambling requires synchronization, offers higher security than fixed code operation, and provides a much greater number of mutually exclusive secure channels.

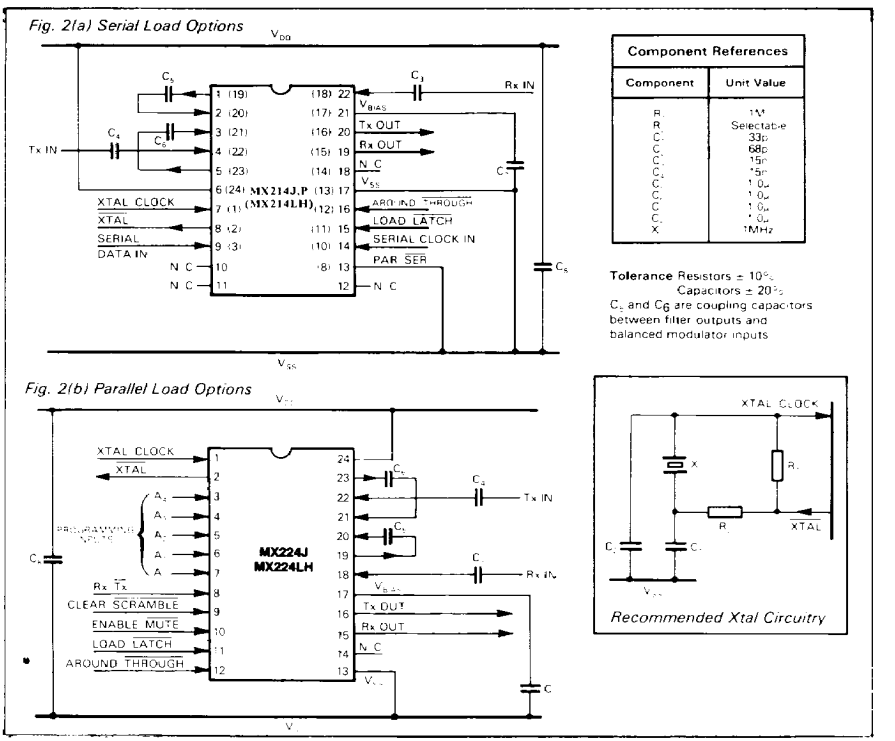
The MX214/224 offers a recovered audio product close to that of a telephone. The on-chip "Mute" function is useful when implementing rolling code continuous synchronization schemes. "Powersave" and "Clear/Scramble" controls are also included on-chip. Timing and filter clocks are derived internally from an on-chip 1 MHz reference oscillator driven by a 1 MHz crystal or clock pulse input.

APPLICATIONS INFORMATION:

Recommended external component connections are shown in Figure 2. In "Scramble" mode, split point frequencies are selected and set in accordance with the ROM address code present at the inputs A_0 to A_4(see Table 2). In "Clear" mode, both the Upper and Lowerband filter limits are used (see Figures 5 or 6), the carrier frequencies are turned off, and the balanced modulators are bypassed internally. The Low Band audio is removed from the output signal prior to summing.

The MUTE function disables the MX214/224's audio outputs to allow periodic transmission of synchronization data. A logic "0" at this input isolates the device while leaving the audio input and output pins at bias level (see Table 1). When the MX214/224 is in POWERSAVE mode, audio signals may be hardwired around the device since the input and output pins are open circuit (see Table 1).

Component Connections



Component References	
Component	Unit Value
R_1	1M
R_2	Selectable
C_1	33p
C_2	68p
C_3	15n
C_4	15n
C_5	1.0µ
C_6	1.0µ
C_7	1.0µ
C_8	1.0µ
X	1MHz

Tolerance Resistors ± 10%
Capacitors ± 20%
C_5 and C_6 are coupling capacitors between filter outputs and balanced modulator inputs

MX214/224 PIN FUNCTION TABLE

PIN NUMBER				FUNCTION
214 J,P	224 J,P	214 LH	224 LH	
7	1	1	1	**Xtal/Clock:** Input to the clock oscillator inverter. A 1 MHz xtal input or externally derived 1 MHz clock is injected here.
8	2	2	2	**$\overline{\text{Xtal}}$:** Output of the clock oscillator inverter.
9	—	3	—	**Serial Data Input:** This pin is used to input an 8-bit word representing the digital control functions. This word is loaded using the serial data clock and is input in the following sequence: MUTE, CLEAR, Rx/$\overline{\text{Tx}}$, A_0, A_1, A_2, A_3, A_4. The load $\overline{\text{latch}}$ pin is operated on completion. Reference the timing diagram in Figure 7.
—	3	—	3	A_4 ┐ **Programming Inputs:** In parallel mode, these five digital inputs define the
—	4	—	4	A_3 ├ split point frequency. Each of the 5 input pins have a 1MΩ internal pullup
—	5	—	5	A_2 ├ resistor. See Table 2 for programming information.
—	6	—	6	A_1 ┤
—	7	—	7	A_0 ┘
—	8	—	8	**Rx/$\overline{\text{Tx}}$:** This digital input selects the Receive or Transmit paths and configures upperband and lowerband filter bandwidths while setting the CTCSS highpass filter position on the signal path. See Table 1 and Figures 5 and 6. 1MΩ internal pullup resistor (Rx).
13	—	8	—	**Parallel/$\overline{\text{Serial}}$:** This pin must be connected to V_{ss} for serial loading. Internal 1MΩ pullup resistor.
—	9	—	9	**Clear/$\overline{\text{Scramble}}$:** This digital input puts the device into "Clear" or "Scramble" mode by controlling the application of carrier frequency to the Upper and Lower band balanced modulators. In "Scramble" mode, the balanced modulator carrier frequency values are selected by the split point address A_0-A_4 (Table2). In "Clear" mode, the carriers are disabled and the balanced modulators are bypassed internally. i.e. the lower band signal is not added to the output signal. 1MΩ internal pullout resistor (Clear).
—	10	—	10	**Enable/$\overline{\text{Mute}}$:** This digital function is used to disable Receive or Transmit signal paths for rolling code synchronization while maintaining bias conditions. Synchronization data can be transmitted during the Mute periods, as is done in the MX1204 VSB Scrambler module. Internal 1MΩ pullup resistor (Enable).
14	—	10	—	**Serial Clock Input:** This is the externally applied data clock frequency used to shift input data along on devices wired in the Serial loading mode. One full data clock cycle is required to shift one data bit completely into the register. See Timing Diagram (Figure 7). 1MΩ internal pullup resistor.
15	11	11	11	**Load/$\overline{\text{Latch}}$:** This pin controls the loading of the 8 digital function inputs (ENABLE, CLEAR, Rx/Tx, A_0-A_4) into the internal register. When this pin is at logic "1," all eight inputs are transparent and new data acts directly. For controlled changing of parameters in the parallel mode, Load $\overline{\text{Latch}}$ must be kept at logic "0" while a new function is loaded, then strobed 0-1-0 to latch the inputs in. For serial loading, the serial data should be loaded with Load/$\overline{\text{Latch}}$ at logic "0" and then Load $\overline{\text{Latch}}$ strobed 0-1-0 on completion of data loading. Internal 1MΩ pullup resistor (Load). See Figure 7.

MX214/224 PIN FUNCTION TABLE

PIN NUMBER				FUNCTION
214 J,P	224 J,P	214 LH	224 LH	
16	12	12	12	**Powersave:** This digital input is used to place the MX214/224 into Powersave mode, where all parts of the device except for the 1 MHz oscillator are shut down. All signal input and output lines are made open circuit, free of all bias. This allows signal paths to be routed externally around the device, while reducing current consumption. A logic "0" at this input enables the device to work normally as shown in Table 1. Internal 1MΩ pullup resistor.
17	13	13	13	**V_{ss}:** Negative Supply (GND).
18	14	14	14	**Internal Connection:** This pin is internally connected. Leave open circuit.
19	15	15	15	**Rx Output:** This is the processed received audio signal output. This pin is held at a DC "bias" voltage for all functions except Powersave. This buffered output is driven by the Summing circuit in the Rx mode. Signal paths and bias levels are detailed in Table 1 and Figure 6.
20	16	16	16	**Tx Output:** This is the processed audio output for the transmission channel. This pin is held at a DC "bias" for all functions except Powersave. This summed and buffered signal is passed through the CTCSS High Pass Filter to the output pin in the Tx mode. Signal paths and bias levels are detailed in Table 1 and Figure 5.
21	17	17	17	**V_{BIAS}:** Normally at $V_{DD}/2$, this pin requires an external decoupling capacitor (C_7) to V_{SS}.
22	18	18	18	**Rx Input:** This is the analog received audio signal input. This pin is held at a DC "bias" voltage by a 300 Kohm on-chip bias resistor which is selected for all functions except Powersave. It must be connected to external circuitry by capacitor C_3 (See Figure 2). This input is routed through the CTCSS High Pass Filter in Rx mode to remove subaudio frequencies from the voiceband. Signal paths and bias levels are detailed in Table 1 and Figure 6.
1	19	19	19	**Highband Filter Output:** The output of the Input Filter of the Upperband limit. The $Rx/\overline{Tx}$ function sets the lowpass filter at 3400 Hz or 2700 Hz respectively. This output must be connected to the Highband Balanced Modulator input via capacitor C_5 (See Figure 2).
2	20	20	20	**Highband Balanced Modulator Input:** The input to the Balanced Modulator of the Upperband limit. This input must be connected to the Highband Filter Output via capacitor C_5 (See Figure 2).
3	21	21	21	**Lowband Balanced Modulator Input:** The input to the Balanced Modulator of the Lowerband limit. This input must be connected to the Lowband Filter Output via capacitor C_6 (See Figure 2).
4	22	22	22	**Tx Input:** This is the analog "Clear" audio input for the VSB scrambler. This pin is held at a DC "bias" voltage by a 300 Kohm on-chip bias resistor, which is selected for all functions except Powersave. It must be connected to external circuitry by capacitor C_4 (See Figure 2). This input, in the Tx mode, is connected to Upper and Lowerband input filters. Signal paths and bias levels are detailed in Table 1 and Figure 5.

MX214/224 PIN FUNCTION TABLE

PIN NUMBER				FUNCTION
214 J,P	224 J,P	214 LH	224 LH	
5	23	23	23	**Lowband Filter Output:** The output of the Input Filter of the Lowerband limit. The Rx/$\overline{Tx}$ function determines which filter is used (Filter 1 or 2). See figures 5 and 6. This output must be connected to the Lowband Balanced Modulator Input via capacitor C_6 (See Figure 2).
6	24	24	24	V_{DD}: A single + 5V supply is required.

Note: Pins 10, 11, and 12 on the MX214J and MX214P are not connected. Pins 4, 5, 6, 7 and 9 on the MX214LH are not connected.

MX214/224 TRUTH TABLE

	Rx/$\overline{Tx}$ = 1	Rx/$\overline{Tx}$ = 0	$\overline{MUTE}$ = 0	POWERSAVE
Rx Path	Enabled	Disabled	Disabled	Disabled
Rx Out Level	Bias	Bias	Bias	High Impedance
Tx Path	Disabled	Enabled	Disabled	Disabled
Tx Out Level	Bias	Bias	Bias	High Impedance

TABLE 1 FUNCTIONS INFLUENCING SIGNAL PATHS

APPLICATIONS INFORMATION

The term "MX214" can be taken to mean MX214 or MX224.

Audio Quality

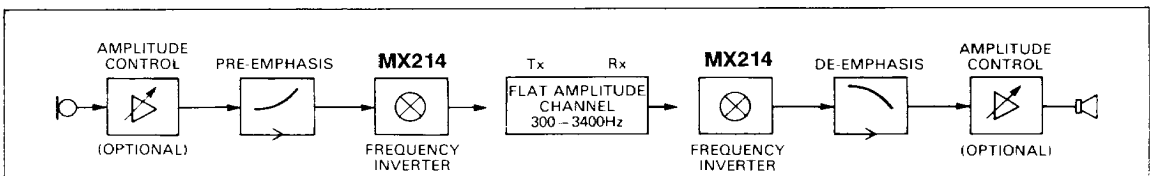


Fig. 3 Recommended Basic Communication Audio System Layout

Figure 3 shows the recommended basic audio system layout using added pre- and deemphasis circuitry to maintain good recovered speech quality. In the Transmit mode, *Do Not* preemphasise the audio output of the MX214. In the Receive mode, deemphasis should be used after the MX214.

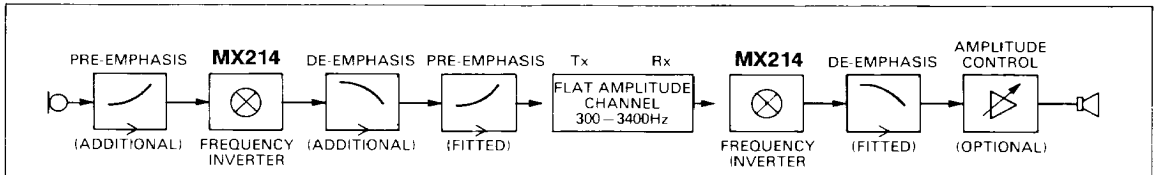


Fig. 4 Recommended Basic Radio Communication Audio System Layout

Figure 4 shows the recommended basic audio system layout if it is necessary to install the MX214 within a radio having pre- and deemphasis circuitry as a standard. This is where post-emphasis access is not possible in the transmitter.

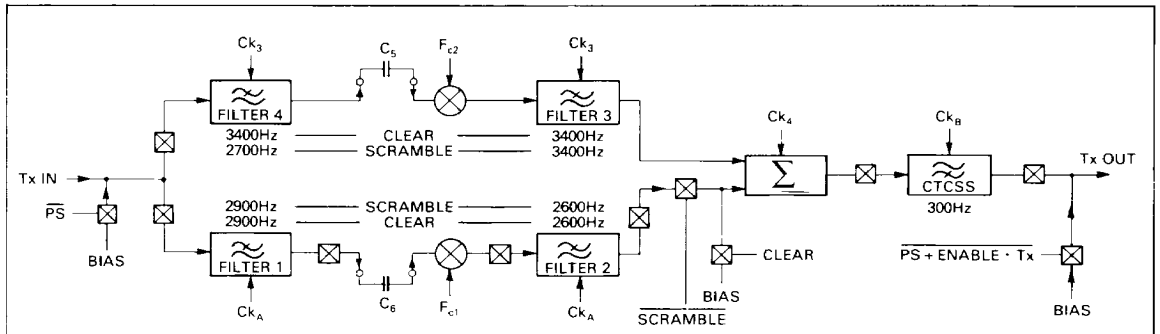


Fig. 5 Basic Tx Path

During the Transmit function the Low Pass and CTCSS filters are configured automatically as shown in Figure 5, with cut-off frequencies (-3dB) indicated.

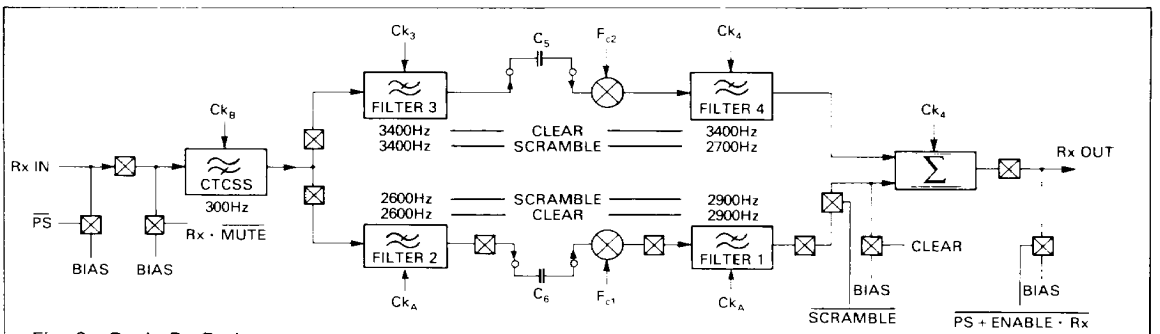


Fig. 6 Basic Rx Path

During the Receive function the Low Pass and CTCSS filters are configured automatically as shown in Figure 6, with cut-off frequencies (-3dB) indicated.

MX214/224 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref. V_{ss} = 0V)		−0.3V to (V_{DD} + 0.3V)
Sink/source current (supply pins)		±30mA
(other pins)		±20mA
Total device dissipation @ 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	MX214J/224J	−30°C + 85 °C (Ceramic)
	MX214P/214LH/224P/224LH	−30°C + 70°C (Plastic)
Storage temperature range:	MX214J/224J	−55°C to + 125° (Ceramic)
	MX214P/214LH/224P/224LH	−40° to + 85°C (Plastic)

Operating Limits:

All characteristics measured using the following parameters unless otherwise specified:

V_{DD} = 5.0V, T_{amb} = 25°C, F_{clk} = 1.0MHz, Audio Level Ref: 0dB = 775 mVrms.

Characteristics	See Note	Min	Typ	Max	Unit
Static Values					
Supply Voltage		4.5	5	5.5	V
Supply Current (Enabled)		—	8	—	mA
Supply Current (Powersave)		—	1.2	—	mA
Analog Input Impedances					
Tx/Input (Enabled)		—	100	—	kΩ
Tx/Rx Input (Powersave)		1	—	—	MΩ
Balanced Modulator		—	40	—	kΩ
Analog Output Impedances					
Rx Output (Tx Mode)		—	100	—	kΩ
Rx Output (Rx Mode)		—	—	2	kΩ
Rx Output (Powersave)		1	—	—	MΩ
Tx Output (Tx Mode)		—	—	2	kΩ
Tx Output (Rx Mode)		—	100	—	kΩ
Tx Output (Powersave)		1	—	—	MΩ
Input LPF		—	—	1	kΩ
Digital Values					
Digital Input Impedance		100	—	—	kΩ
Dynamic Values					
Input Logic '1'		3.5	—	—	V
Input Logic '0'		—	—	1.5	V
Xtal/Clock Frequency		—	1	—	MHz
Analog Input Level		−18	—	+6	dB
Carrier Breakthrough	1	—	−55	—	dB
Baseband Breakthrough	1, 2 or 3	—	−33	—	dB
Filter Clock Breakthrough	1, 2, or 3	—	−50	—	dB
Output Noise	1, 4	—	−45	—	dB

Characteristics	See Note	Min	Typ	Max	Unit
Passband Characteristics					
Clear Mode	7				
Passband Gain		—	0	—	dB
Output Lower 3dB Point (Rx or Tx)		—	300	—	Hz
Output Upper 3dB Point (Rx or Tx)		—	3400	—	Hz
Scramble-Descramble	5				
Received Signal Passband Gain	6	—	0	—	dB
Received Signal Lower 3dB Point		—	400	—	Hz
Received Signal Upper 3dB Point		—	2700	—	Hz
Transmitted Signal Lower 3dB Point		—	300	—	Hz
Transmitted Signal Upper 3dB Point		—	3400	—	Hz
CTCSS (Highpass Filter)					
−3dB Point		—	300	—	Hz
Passband Gain		—	0	—	dB
Stopband Attenuation at f < 250 Hz		—	40	—	dB
Timing *(Figure 7)*					
Serial Mode Enable Set Up (t_{SMS})		250	—	—	ns
Serial Clock 'High' Pulse Width (t_{PWH})		250	—	—	ns
Serial Clock 'Low' Pulse Width (t_{PWL})		250	—	—	ns
Data Set Up Time (t_{DS})		150	—	—	ns
Data Hold Time (t_{DHS})		50	—	—	ns
Load/$\overline{\text{Latch}}$ Set Up Time (t_{LL})		250	—	—	ns
Load/$\overline{\text{Latch}}$ Pulse Width (t_{LLW})		150	—	—	ns
Data Set Up Time(t_{DSP})		150	—	—	ns
Data Hold Time (t_{DHP})		20	—	—	ns

Notes: *1. Measured at the output of a single device.*
2. Tx Mode.
3. Rx Mode.
4. With input A.C. short-circuited to V_{ss}.
5. Measured at the output of a receiving device in a scrambler-descrambler system with a transmission channel having a flat amplitude response and a bandwidth of 300Hz to 3400 Hz and measured relative to the input signal at the transmitting device.
6. Excluding split point ± 150 Hz.
7. Measured at the Rx or Tx output pin of a single device.

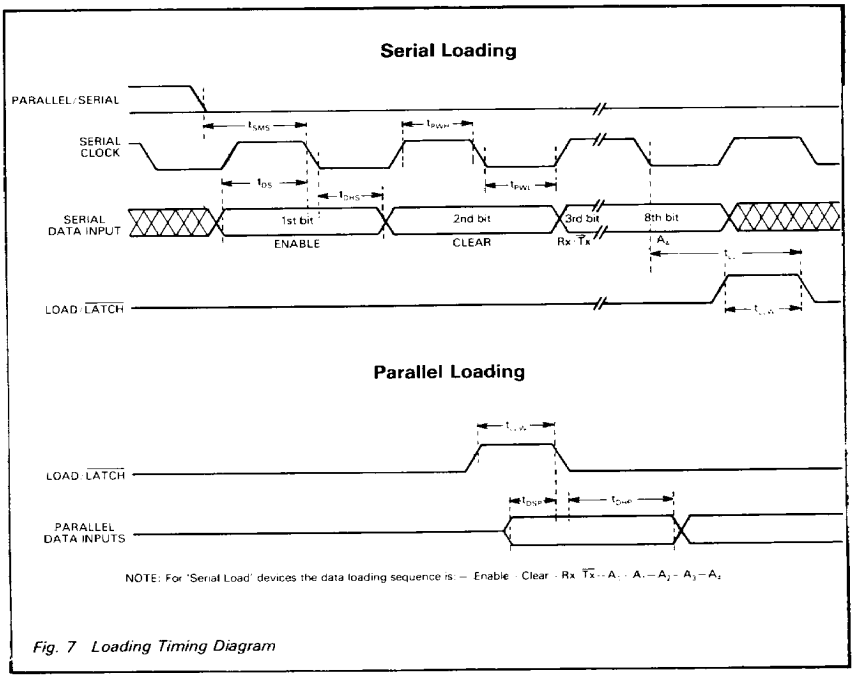


Fig. 7 Loading Timing Diagram

ROM Address A_4–A_0	Split Point Hz	Low Band Carrier, Hz f_{c_1}	High Band Carrier, Hz f_{c_2}	ROM Address A_4–A_0	Split Point Hz	Low Band Carrier, Hz f_{c_1}	High Band Carrier, Hz f_{c_2}
00000	2800	3105	6172	10000	1135	1436	4504
00001	2625	2923	6024	10001	1050	1351	4424
00010	2470	2777	5813	10010	976	1278	4347
00011	2333	2631	5681	10011	913	1213	4310
00100	2210	2512	5555	10100	857	1157	4273
00101	2100	2403	5494	10101	792	1094	4166
00110	2000	2304	5376	10110	736	1037	4132
00111	1909	2212	5263	10111	688	988	4065
01000	1826	2127	5208	11000	636	936	4032
01001	1750	2049	5102	11001	591	891	3968
01010	1680	1984	5050	11010	552	853	3937
01011	1555	1858	4950	11011	512	813	3906
01100	1448	1748	4807	11100	471	772	3846
01101	1354	1655	4716	11101	428	728	3816
01110	1272	1572	4629	11110	388	688	3787
01111	1200	1501	4587	11111	350	650	3731

Table 2 ROM Address Programming Table