VME 3000

VMEbus Interrupt Generator

January 1989

Distinctive Features

- **Provides random logic and high current drive for VMEbus interrupt generator in 300 mil 24 pin DIP or 28 pin LCC package**
- **IRQ* can be connected to any single interrupt request level**
- **Includes interrupter arbitration logic**
- **Drives 48mA IRQ* signal**
- **Input hysteresis filters bus noise**

Programmable Version Available

If the VME 3000 does not match the requirements of the design, a programmable version is available (the PLX 448) which allows the user to customize all inputs, outputs and logic. Programming is performed using industry standard tools such as ABEL™ or CUPL™ software and commonly available PLD programming hardware. Contact PLX for a data sheet on the PLX 448 and other information.

Applications

- **Single level interrupt generator logic for VMEbus slave modules generating an 8 bit interrupt vector**

General Description

The VME 3000 is a CMOS single level interrupt generator for the VMEbus which is packaged in a compact 24 pin 300 mil wide DIP or 28 pin LCC. The protocols of the VME 3000 meet the VMEbus Revision C.1 timing requirements. The device buffers and drives the VMEbus signals to the Rev. C.1 electrical specifications.

The VME 3000 will respond to an interrupt cycle when it receives IACKIN* from the daisy chain. It arbitrates between IACKIN* and the interrupt request signal, compares priority levels and generates an interrupt acknowledge or IACKOUT* depending on which is appropriate.

This part will function with any interrupt handler and master module which meets the Rev. C.1 VMEbus specification.

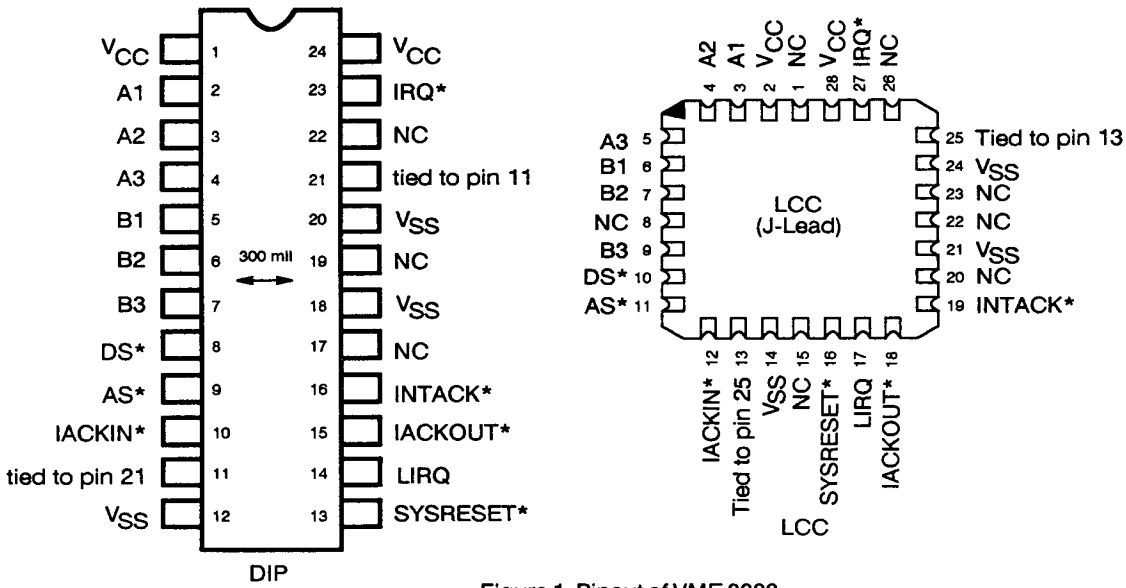

Figure 1. Pinout of VME 3000

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Patent Pending

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Pin Description

28 Pin LCC	24 Pin DIP	Signal	Type	Function
2	1	V_{CC}	–	5V Power Supply.
3	2	A_1	I	Active high, Address bit 1; VME address bit.
4	3	A_2	I	Active high, Address bit 2; VME address bit.
5	4	A_3	I	Active high, Address bit 3; VME address bit.
6	5	B_1	I	Active high, Encode level bit 1; Encode bit for IRQ* priority level.
7	6	B_2	I	Active high, Encode level bit 2; Encode bit for IRQ* priority level.
9	7	B_3	I	Active high, Encode level bit 3; Encode bit for IRQ* priority level.
10	8	DS*	I	Active low, Data Strobe; DS0* for interrupt vector size.
11	9	AS*	I	Active low, VMEbus Address Strobe; Indicates valid address.
12	10	IACKIN*	I	Active low, Interrupt Acknowledge In; VMEbus IACK* daisy chain input.
13	11		I	Tied to pin 21 (DIP) or 25 (LCC).
14	12	V_{SS}	–	Chip Ground.
16	13	SYSRESET*	I	Active low, System Reset; VMEbus System Reset.
17	14	LIRQ	I	Active high, Local Interrupt Request; Interrupt Request from local slave.
18	15	IACKOUT*	O	Active low, Interrupt Acknowledge Out; IACK* daisy chain output if interrupt cycle does not belong to local slave.
19	16	INTACK*	O	Active low, Interrupt Acknowledge; VME 3000 generates INTACK* if interrupt cycle belongs to local slave.
20	17	NC	–	No connect.
21	18	V_{SS}	–	Chip Ground.
23	19	NC	–	No connect.
24	20	V_{SS}	–	Chip Ground.
25	21		O	Tied to pin 11 (DIP) or pin 13 (LCC).
26	22	NC	–	No connect.
27	23	IRQ*	O	Active low, Interrupt Request; Interrupt request can be connected to any priority level, 48 mA OC.
28	24	V_{CC}	–	5V Power Supply.
1, 8 15,22	–	NC	–	No Connect

Note: OC is Open Collector

Detailed Description

The VME 3000 generates an interrupt request, IRQ*, and will respond to an interrupt cycle when it receives IACKIN*. The VME 3000 will then assert IACKOUT* or INTACK* depending on whether or not it was selected to participate in the interrupt cycle.

Figure 2 contains a block diagram of a typical interrupt generator configuration. Figure 3 shows the critical timing relationships.

The local slave generates an interrupt request by asserting LIRQ high. The VME 3000, in turn, drives IRQ* low, which indicates to the VME system interrupt handler that an interrupt request is pending. The IRQ* output of the VME 3000 should be hardwired or connected through jumpers to the desired VMEbus interrupt request level IRQ_n* (n = 1 to 7). If multiple interrupt request levels or dynamic selection of the interrupt request levels is required, contact PLX for information on how to meet these requirements.

After receiving one or more interrupt requests, the system interrupt handler will drive IACKIN* down the IACK daisy chain, which indicates the beginning of a VMEbus interrupt cycle. When the VME 3000 receives IACKIN*, it will arbitrate between IACKIN* and the interrupt request it generates (IRQ*) to determine which occurred first.

If the VME 3000 receives IACKIN* **before** it has asserted IRQ*, then the local slave has "lost" the arbitration and must generate IACKOUT* down the IACK* daisy chain. The local slave will not participate in this interrupt cycle. Another slave in the system will participate in the cycle. In this case, the VME 3000 will continue to assert IRQ* until it is eventually selected to participate.

If the VME 3000 receives IACKIN* **after** it has asserted IRQ* then the VME 3000 will compare the valid addresses A1-A3 to the encoded priority levels B1-B3. If these do not match, the VME 3000 will not participate in the interrupt cycle and must generate IACKOUT* down the daisy chain. As in the case described in the previous paragraph, the VME 3000 will continue to assert IRQ* until it is eventually selected to participate.

If the VME 3000 receives IACKIN* **after** it asserts IRQ* **and** A1-A3 matches B1-B3 then the local slave has been selected to participate in the interrupt cycle. In this case the VME 3000 asserts the interrupt acknowledge signal, INTACK*. It does not pass IACKOUT* down the daisy chain.

DS0* is connected to DS* to generate an 8 bit interrupt vector. Please contact factory for information on generating a 16/32 bit interrupt vector generator device.

When the VME 3000 asserts INTACK*, the local slave enables the data buffers for the interrupt vector. To complete the interrupt cycle, the local slave asserts DTACK*.

NOTE: The VME3000 is edge triggered. The assertion of INTACK* releases IRQ*. Also, the assertion of SYSRESET* clears the pending interrupt request, IRQ*. Please contact the factory for information on level sensitive devices.

If the VME 3000 is used in conjunction with PLX Technology's VME 2000 slave module selector, then the INTACK* output from the VME 3000 can be connected to the INTACK* input of the VME 2000. Once the VME 2000 receives INTACK*, it will enable MODSEL* which enables the data buffers for the interrupt vector. The VME 2000 will also generate DTACK* to finish the cycle. (See the VME 2000 data sheet).

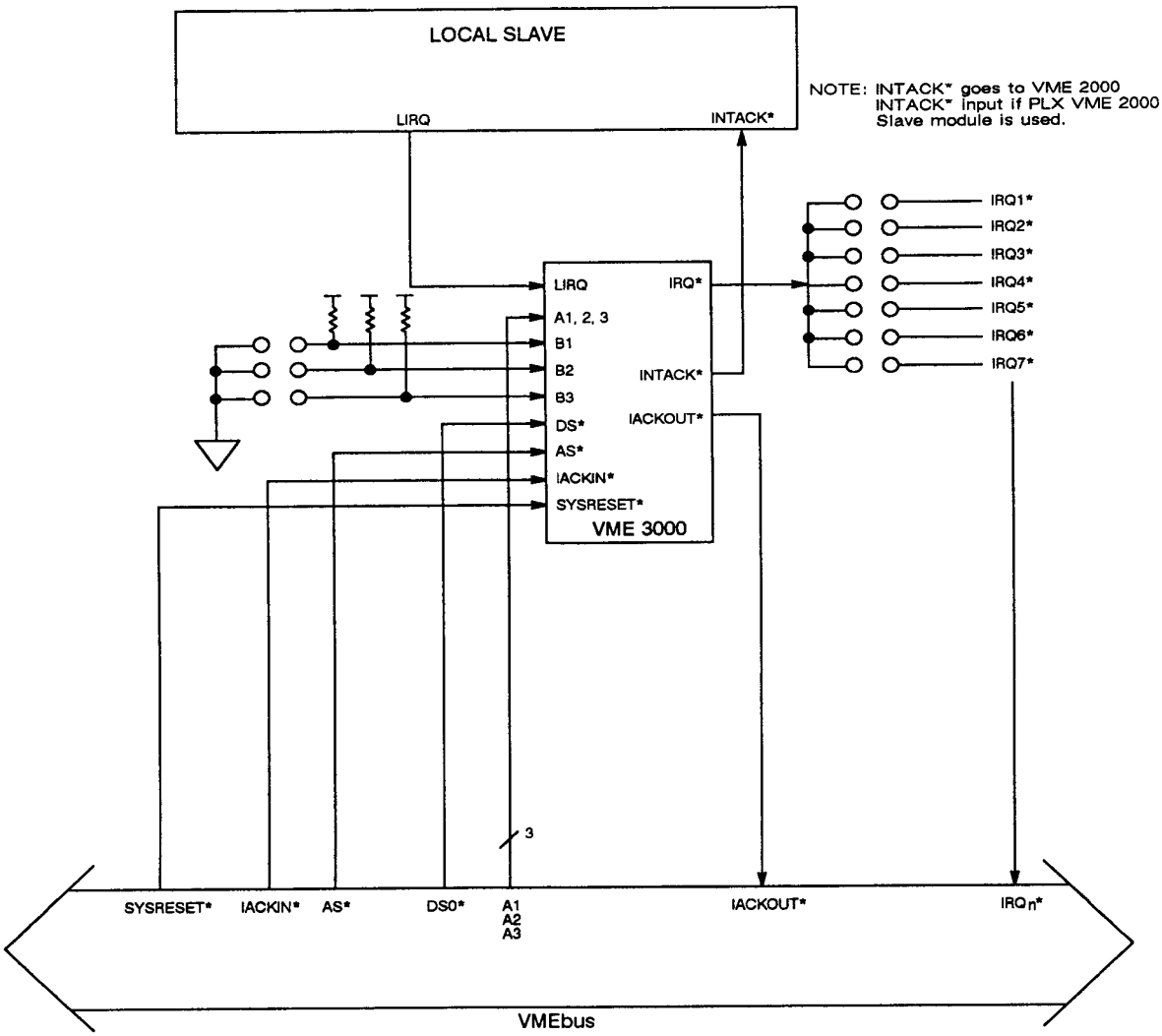

Figure 2. Interrupt Generator

INTERRUPT GENERATOR TIMING

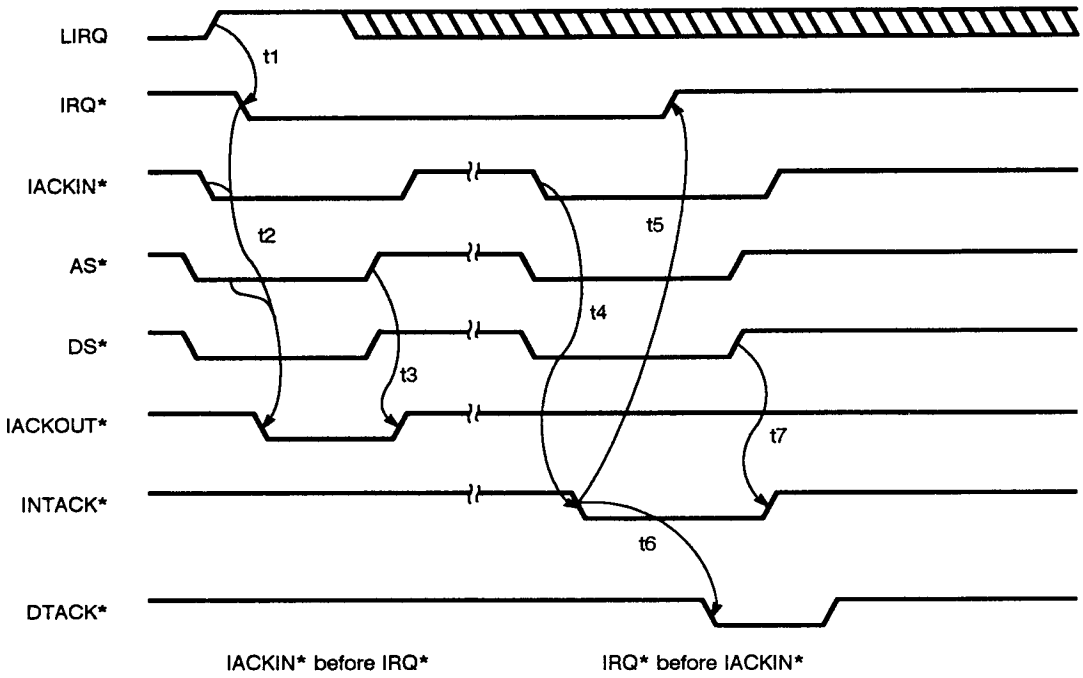

Figure 3. VMEbus Interrupt Generator Timing Diagram

VME 3000 Timing Specifications

Timing Parameter	Signals	Max. Time (ns) -25, -35, -45 parts unless otherwise specified	Description
t1	LIRQ to IRQ* enable	15, 25, 35	LIRQ is positive edge sensitive, LIRQ needs to be high for min. of 20 ns, 30 ns, 40 ns for -25, -35, -45 parts to enable IRQ*
t2	IRQ* to IACKOUT* enable	25, 35, 45	If IACKIN* is received 75, 135 ns before IRQ*. AS* must be low.
	IACKIN* to IACKOUT*	95, 105, 135	If IRQ* and IACKIN* are received at the same time. This allows for worst case arbitration timing. AS* must be low.
t3	AS* to IACKOUT* disable	25, 35, 45	
t4	IACKIN* to INTACK* enable	75, 105, 135	
t5	INTACK* (or SYSRESET*) to IRQ* disable	50, 70, 90	
t6	INTACK* to DTACK* enable	@ local slave	DTACK* finishes the interrupt cycle.
t7	DS* to INTACK* disable	25, 35, 45	

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature with
Power Applied ..... -55°C to +125°C
Supply Voltage to Ground
(pin 24 to pins 12, 18, & 20 on DIP) .. -0.5V to +7.0V
DC Voltage to Outputs in
High Z State ..... -0.5V to +7.0V

Operating Ranges

Commercial (C) Devices
Temperature Ambient ..... 0°C to +70°C
Supply Voltage (V_{CC}) ..... 5V ±5%

Electrical Characteristics Tested over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	Output pins I_{OL} = 24mA		0.5	V
			Pin 23 only (DIP) I_{OL} = 48mA		0.5	V
V_{IH}	Input HIGH Level			2.0		V
V_{IL}	Input LOW Level				0.8	V
I_{IX}	Input Leakage Current	V_{SS} <= V_{IN} <= V_{CC}, V_{CC} = Max		-10	10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{SS} <= V_{OUT} <= V_{CC}		-40	40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0.5V		-30	-90	mA
I_{CC}	Power Supply Current	V_{CC} = Max, V_{IN} = GND Outputs Open			90	mA

Capacitance (sample tested only)

Parameter	Test Conditions	Pins	Typ	Units
C_{IN}	V_{IN} = 2.0V @ f = 1MHz	2-11, 14 (DIP)	5	pF
		13, 15-17, 18, 20-23 (DIP)	10	pF
C_{OUT}	V_{IN} = 2.0V @ f = 1MHz	13, 15-17, 18, 20-23 (DIP)	10	pF

Package Information

The devices are available in 24 pin slimline DIP (300 mil wide) or 28 pin LCC.

See PLX 448 or PLX 464 January 1989 or later data sheets for package dimensions. Contact PLX for further packaging information.