32-Channel ±40V Liquid Crystal Display Row Driver

Ordering Information

Device	Package Options	
	44-Lead Quad Plastic Chip Carrier	44-Lead Quad Plastic Gullwing
HV6008	HV6008PJ	HV6008PG

Features

- ❏ Symmetrical ± 40V output swing
- ❏ Active return to GND
- ❏ 15mA peak source/sink/GND current per channel
- ❏ +5V control logic
- ❏ Special shift register with clear
- ❏ Phase shift control
- ❏ Output enable
- ❏ Data out enable
- ❏ 1MHz shift register
- ❏ Surface mount package available

General Description

Not recommended for new designs.

The HV60 is a 32-channel liquid crystal display driver with 3-state DMOS outputs. Each output can be set to +40V, -40V, or GND. A symmetric waveform can be applied to a capacitive load using the phase shift feature of the HV60.

The HV60 consists of a 32-bit shift register with Clear, Enable, and Phase Shift logic, and 32 high voltage output buffers. With the Enable pin held low, all outputs are placed in the return to zero (GND) state. When Enable is high, each output reflects the data in its shift register bit. All outputs with a logic “0” in their shift register will be in the return to zero state. Outputs with a logic “1” in their shift register will reflect the state of the phase shift pin. These outputs will be switched to V_{PP} when phase shift is high and V_{NN} when phase shift is logic “0”.

Additional functions provided are Shift Register Clear and Data Out. All bits of the shift register are changed to logic “0” when Clear is pulled low. With Clear at a logic “1”, normal shift register operation proceeds. The data output reflects the status of the 32nd shift register stage.

Absolute Maximum Ratings

Supply voltage, V_{DD1}[1]	-6V
Supply voltage V_{DD2}[1]	+6V
Supply voltage V_{PP}[1,2]	+42V
Supply voltage V_{NN}[1]	-42V
Logic input levels[1]	V_{DD1} - 0.3V to V_{DD2} + 0.3V
Ground currrent[2]	700mA
Continuous total power dissipation[3]	1W
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Notes:
1. All voltages are referenced to GND.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to 85°C at 16.7mW/°C.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
$I_{DD1,2}$	V_{DD} supply current	V_{DD1}			500	μA	V_I = 4V, V_{DD1} = -6V
		V_{DD2}					V_I = 4V, V_{DD2} = +6V
V_{IH}	Logic input high		+2		V_{DD2}	V	V_{DD1} = -4.5V,
V_{IL}	Logic input low		V_{DD1}		-2	V	V_{DD2} = +4.5V
V_{OH}	Logic output high		+2			V	V_{DD1} = -4.5V V_{DD2} = +4.5V I_{OH} = -15μA I_{OL} = 250μA
V_{OL}	Logic output low				-2	V	
I_{IH}	High-level logic input current				+3	μA	$V_I = V_{DD}$, $V_{DD1,2}$ = max
I_{IL}	Low-level logic input current				-50	μA	V_I = 0V, $V_{DD1,2}$ = max
I_{PP}	High voltage supply current				+1	mA	Static, no load
I_{NN}	High voltage supply current				-1	mA	Static, no load
V_{OH}	Output voltage high		+39			V	V_{PP}, V_{NN} = ±40 No load
V_{CL}	Output voltage clamp		-20		+20	mV	
V_{OL}	Output voltage low				-39	V	
Z_{OH}	Output switch impedence high			1000		Ω	V_{PP}, V_{NN} = ±40 I_O = ±15mA
Z_{CL}	Output switch impedance clamp			500			
Z_{OL}	Output switch impedance low			700			
I_O	DC output current	Output H or L			5	mA	1 output only
		Data out H or L			150	μA	

AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{WH}	Width of high data pulse	500			ns	
t_{WL}	Width of low data pulse	500			ns	
t_{SU}	Data set-up time before clock falls	25			ns	
t_H	Data hold time after clock falls	10			ns	
	Phase shift duty cycle		50		%	

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD1}	Logic supply voltage	-4		-6	V
V_{DD2}	Logic supply voltage	+4		+6	V
V_{PP}	High voltage supply	+10		+40	V
V_{NN}	High voltage supply	-10		-40	V
V_{IH}	High-level input voltage	+2V		V_{DD2}	V
V_{IL}	Low-level input voltage	-2V		V_{DD1}	V
$I_{O\ Pk.}$	Peak output current (any state)			±80	mA
T_A	Operating free-air temperature	-40		+70	°C
f_{DIN}	Input data rate			1	MHz
f_{PS}	Phase shift rate			20	KHz

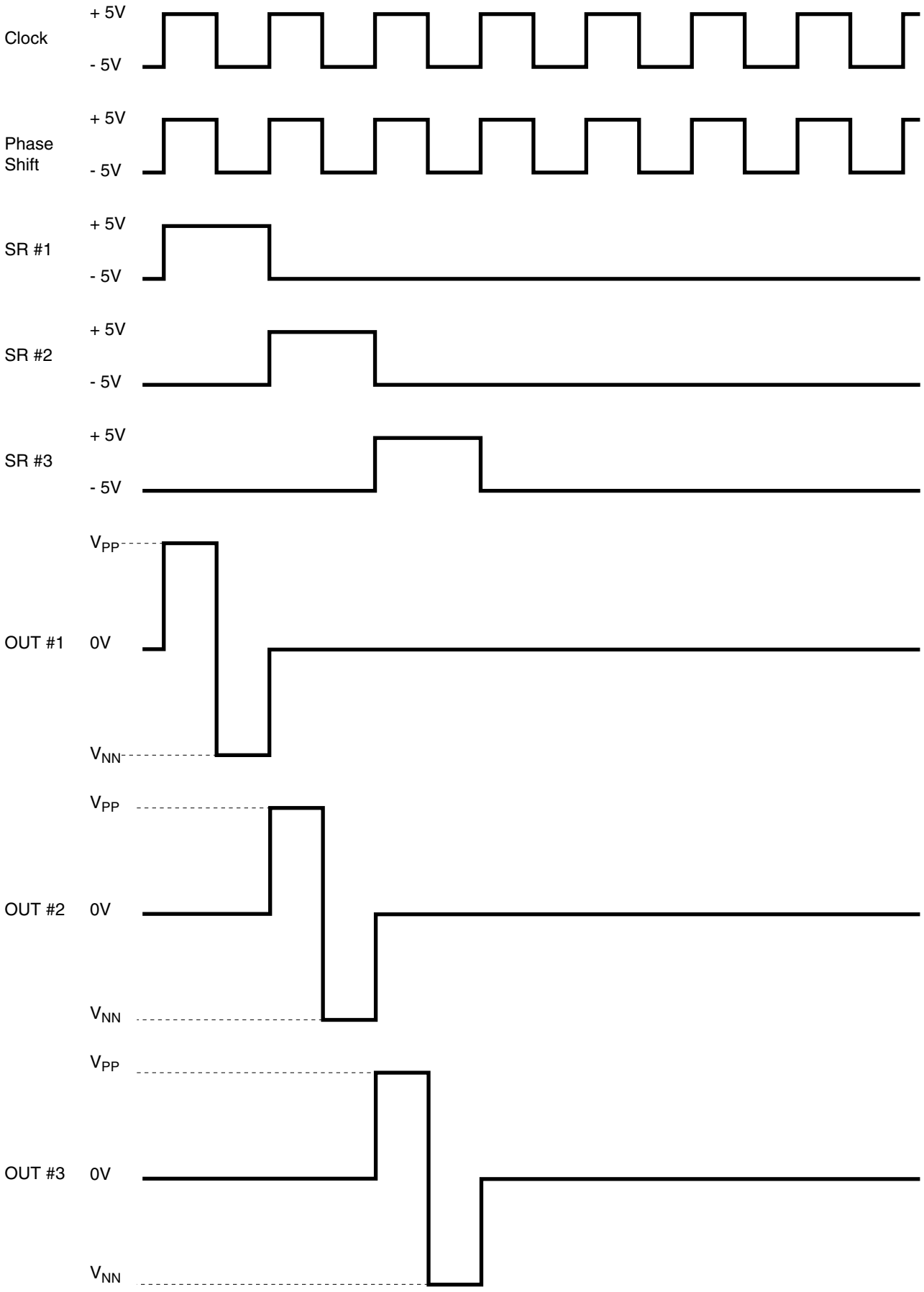
Note:

Power-up sequence should be the following:

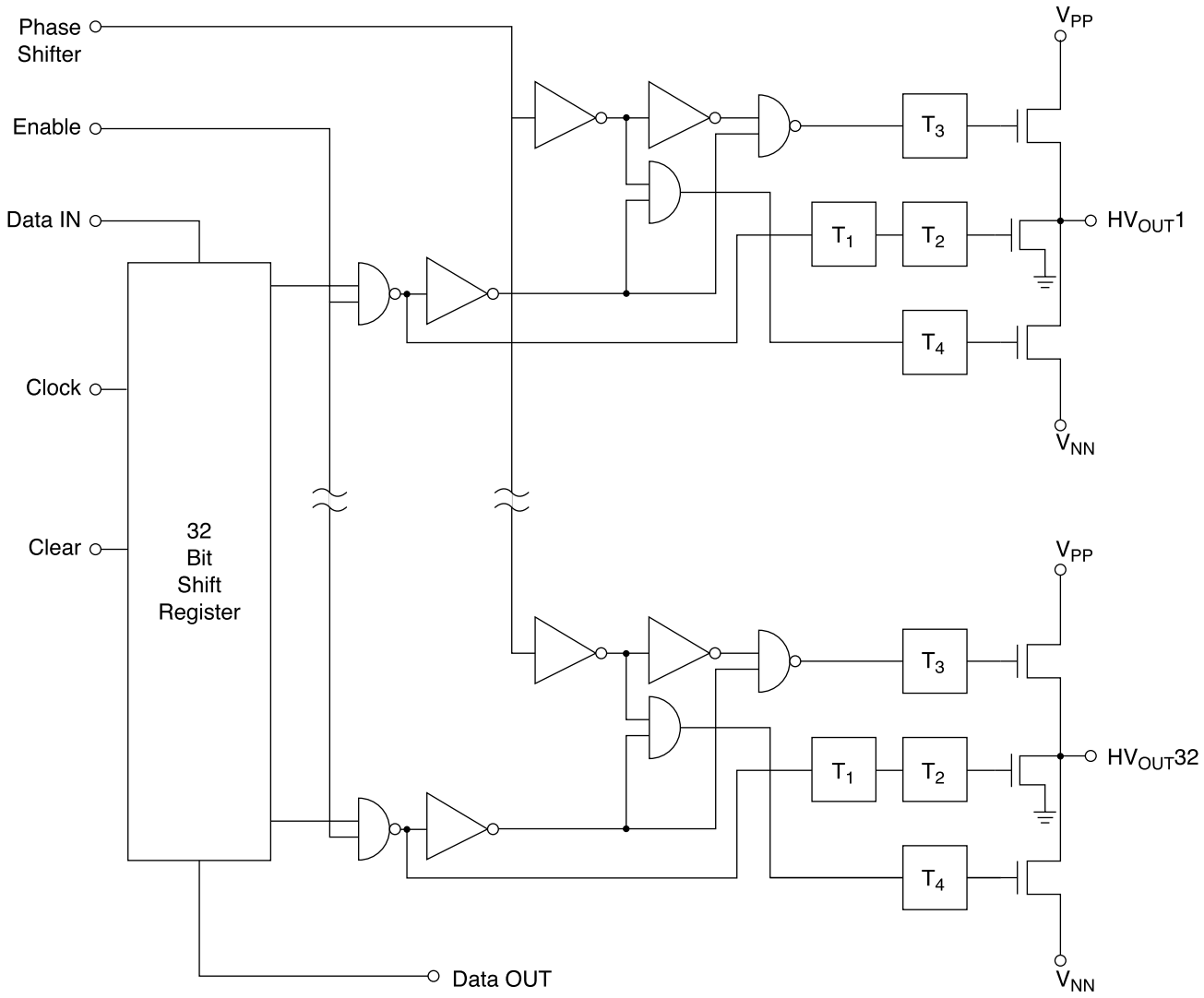
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP} and V_{NN}.

Power-down sequence should be the reverse of the above.

Switching Waveform



Functional Block Diagram



Function Table

Function	Inputs					Shift Reg	Outputs	
	Data In	CLK	CLR	Enable	Phase Shift	1 2…32	HV Outputs 1 2…32	Data Out
CLR Reg	X	X	H	X	X	ALL L	ALL GND	L
All output GND	X	X	X	L	X	* *…*	ALL GND	*
Load S/R	H or L	↓	L	L	X	H or L *…*	ALL GND	*
Output State	X	H or L	L	H	X	L L…L	GND GND…GND	*
					H	H H…H	V_{PP} V_{PP}…V_{PP}	*
					L	H H…H	V_{NN} V_{NN}…V_{NN}	*

Notes:
X = Irrelevant
* = Dependent on previous stage's state before the last CLK
↓ = High to low transition
H = High level
L = Low level

Pin Configurations

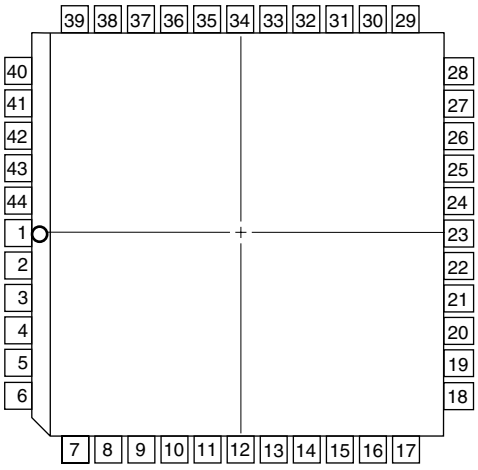
44-Pin J-Lead

Pin	Function	Pin	Function
1	HV_{OUT} 16	23	$V_{DD\ 1}$
2	HV_{OUT} 15	24	Enable
3	HV_{OUT} 14	25	$V_{DD\ 2}$
4	HV_{OUT} 13	26	GND
5	HV_{OUT} 12	27	Data Out
6	HV_{OUT} 11	28	HV_{OUT} 32
7	HV_{OUT} 10	29	HV_{OUT} 31
8	V_{PP}	30	HV_{OU} 30
9	HV_{OUT} 9	31	HV_{OUT} 29
10	HV_{OUT} 8	32	HV_{OUT} 28
11	HV_{OUT} 7	33	HV_{OUT} 27
12	HV_{OUT} 6	34	HV_{OUT} 26
13	HV_{OUT} 5	35	HV_{OUT} 25
14	HV_{OUT} 4	36	HV_{OUT} 24
15	HV_{OUT} 3	37	V_{NN}
16	HV_{OUT} 2	38	HV_{OUT} 23
17	HV_{OUT} 1	39	HV_{OUT} 22
18	Data In	40	HV_{OUT} 21
19	GND	41	HV_{OUT} 20
20	Phase Shift	42	HV_{OUT} 19
21	Clock	43	HV_{OUT} 18
22	Clear	44	HV_{OUT} 17

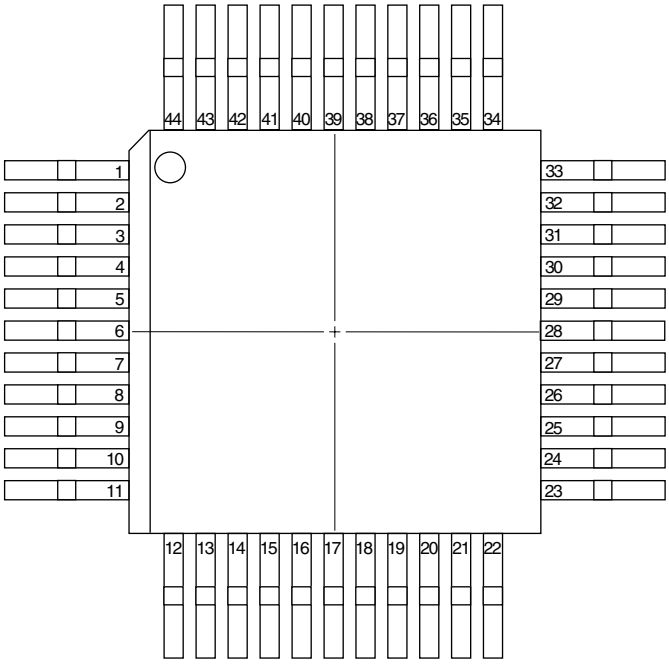
44-Pin Quad Palstic Package

Pin	Function	Pin	Function
1	HV_{OUT} 21	23	Data In
2	HV_{OUT} 20	24	GND
3	HV_{OUT} 19	25	Phase Shift
4	HV_{OUT} 18	26	Clock
5	HV_{OUT} 17	27	Clear
6	HV_{OUT} 16	28	V_{DD1}
7	HV_{OUT} 15	29	Enable
8	HV_{OUT} 14	30	V_{DD2}
9	HV_{OUT} 13	31	GND
10	HV_{OUT} 12	32	Data Out
11	HV_{OUT} 11	33	HV_{OUT} 32
12	HV_{OUT} 10	34	HV_{OUT} 31
13	V_{PP}	35	HV_{OUT} 30
14	HV_{OUT} 9	36	HV_{OUT} 29
15	HV_{OUT} 8	37	HV_{OUT} 28
16	HV_{OUT} 7	38	HV_{OUT} 27
17	HV_{OUT} 6	39	HV_{OUT} 26
18	HV_{OUT} 5	40	HV_{OUT} 25
19	HV_{OUT} 4	41	HV_{OUT} 24
20	HV_{OUT} 3	42	V_{NN}
21	HV_{OUT} 2	43	HV_{OUT} 23
22	HV_{OUT} 1	44	HV_{OUT} 22

Package Outlines



top view
44-pin J Lead Package

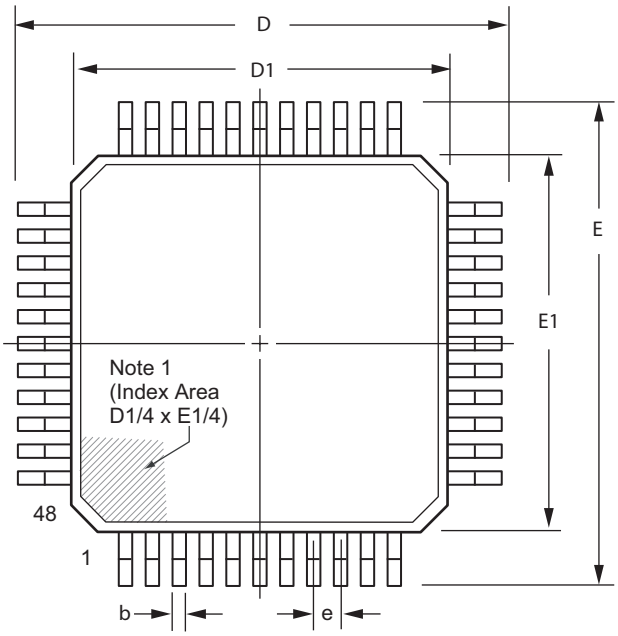


top view
44-pin Quad Plastic Gullwing Package

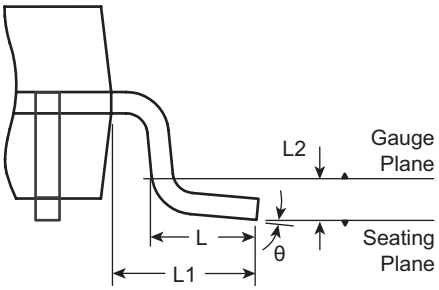
Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 744-0100 • FAX: (408) 222-4895
www.supertex.com

44-Lead PQFP Package Outline (PG)

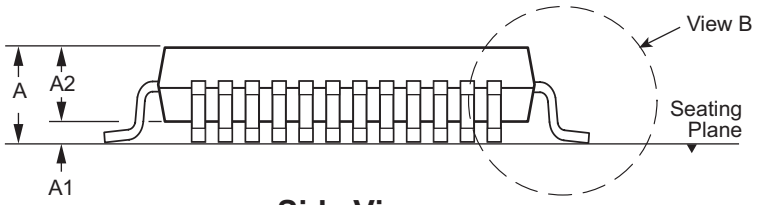
10x10mm body, 2.45mm height (max.), 0.80mm pitch



Top View



View B



Side View

Note 1:

A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	-	0.25	1.95	0.30	13.65	9.80	13.65	9.80	0.80 BSC	0.73	1.95 REF	0.25 BSC	3.5°	5°
	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00		0.88			-	-
	MAX	2.45	-	2.10	0.45	14.15	10.20	14.15	10.20		1.03			7°	16°

JEDEC Registration M0-112, Variation AA-2, Issue B, Sep.1995.

Drawings not to scale.

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 222-8888 / FAX: (408) 222-4895
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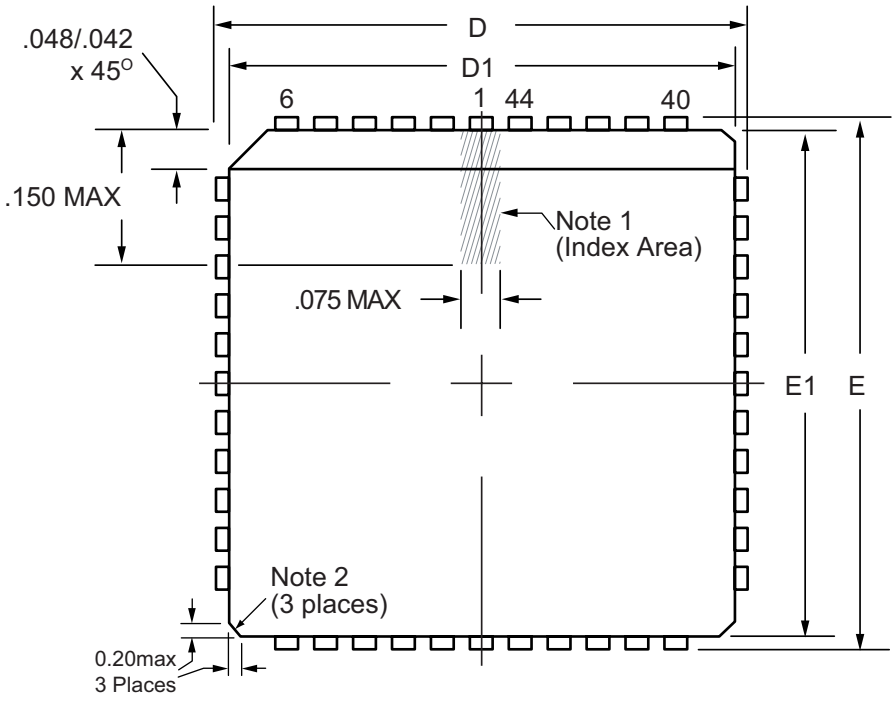
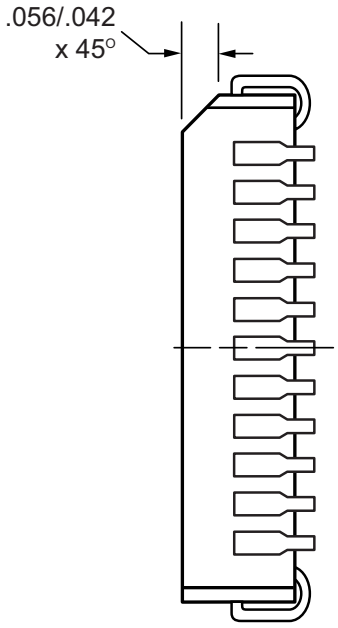
44-Lead PLCC Package Outline (PJ)

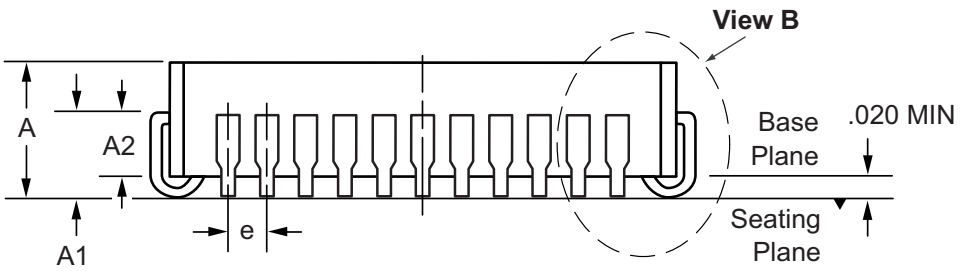
.653x.653in body, .180in height (max.), .050in pitch



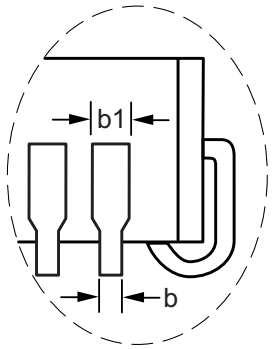
Top View



Side View



Side View



View B

Note:

1. A Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

2. Exact shape of this feature is optional.

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC
	NOM	.172	.105	-	-	-	.690	.653	.690	.653	
	MAX	.180	.120	.083	.021	.036	.695	.656	.695	.656	

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

Drawings are not to scale.

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