

CC112x, CC1175

Silicon Errata



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CC112x, CC1175 Silicon Errata

1.1 VCO Calibration

1.1.1 Description

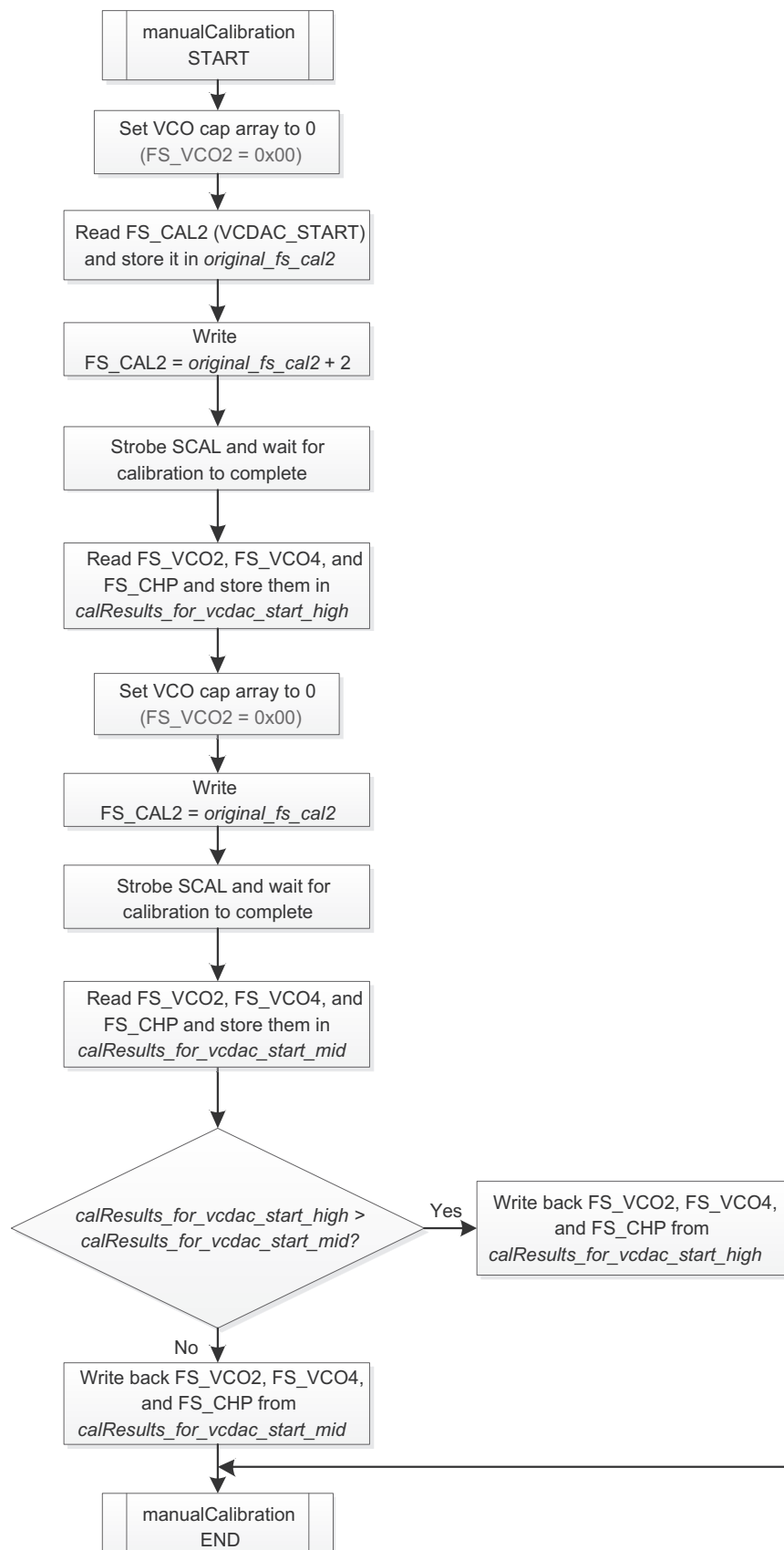
The RF frequency is set by the on-chip inductor, a capacitor array and a varactor. There is a finite possibility that the calibration fails because a non-optimum index to the capacitor array is chosen during the calibration. When the calibration fails the chip will always use a too low index for the capacitor array (that is, too high capacitance).

1.2 Suggested Workaround

For the CC1120, CC1121, CC1125, and CC1175 devices with the PARTVERSION register equal to 0x21, two manual calibrations must be performed as shown in the flow diagram [Figure 1-1](#). The software implementation is shown in [Figure 1-2](#).

For CC1120, CC1121, CC1125, and CC1175 with the PARTVERSION register equal to 0x23, the VCO calibration issue is corrected. These devices can be calibrated using one manual calibration option (using SCAL), and the three automatic calibration options that are controlled by the `SETTLING_CFG.FS_AUTOCAL` setting, which is explained in the *CC112x/CC1175 User's Guide* ([SWRU295](#)).

Applications using the workaround calibration procedure required for PARTVERSION 0x21 can safely continue to use the workaround procedure with PARTVERSION 0x23 or higher.


Figure 1-1. Flow Diagram

```
#define VCDAC_START_OFFSET 2
#define FS_VCO2_INDEX 0
#define FS_VCO4_INDEX 1
#define FS_CHP_INDEX 2

void manualCalibration(void) {

    uint8 original_fs_cal2;
    uint8 calResults_for_vcdac_start_high[3];
    uint8 calResults_for_vcdac_start_mid[3];
    uint8 marystate;
    uint8 writeByte;

    // 1) Set VCO cap- array to 0 (FS_VCO2 = 0x00)
    writeByte = 0x00;
    cc112xSpiWriteReg(CC112X_FS_VCO2, &writeByte, 1);

    // 2) Start with high VCDAC (original VCDAC_START + 2):
    cc112xSpiReadReg(CC112X_FS_CAL2, &original_fs_cal2, 1);
    writeByte = original_fs_cal2 + VCDAC_START_OFFSET;
    cc112xSpiWriteReg(CC112X_FS_CAL2, &writeByte, 1);

    // 3) Calibrate and wait for calibration to be done (radio back in IDLE state)
    trxSpiCmdStrobe(SCAL);
    do {
        cc112xSpiReadReg(CC112X_MARystate, &marystate, 1);
    } while (marystate != 0x41);

    // 4) Read FS_VCO2, FS_VCO4 and FS_CHP register obtained with high VCDAC_START value
    cc112xSpiReadReg(CC112X_FS_VCO2, &calResults_for_vcdac_start_high[FS_VCO2_INDEX], 1);
    cc112xSpiReadReg(CC112X_FS_VCO4, &calResults_for_vcdac_start_high[FS_VCO4_INDEX], 1);
    cc112xSpiReadReg(CC112X_FS_CHP, &calResults_for_vcdac_start_high[FS_CHP_INDEX], 1);

    // 5) Set VCO cap- array to 0 (FS_VCO2 = 0x00)
    writeByte = 0x00;
    cc112xSpiWriteReg(CC112X_FS_VCO2, &writeByte, 1);

    // 6) Continue with mid VCDAC (original VCDAC_START):
    writeByte = original_fs_cal2;
    cc112xSpiWriteReg(CC112X_FS_CAL2, &writeByte, 1);

    // 7) Calibrate and wait for calibration to be done (radio back in IDLE state)
    trxSpiCmdStrobe(SCAL);
    do {
        cc112xSpiReadReg(CC112X_MARystate, &marystate, 1);
    } while (marystate != 0x41);

    // 8) Read FS_VCO2, FS_VCO4 and FS_CHP register obtained with mid VCDAC_START value
    cc112xSpiReadReg(CC112X_FS_VCO2, &calResults_for_vcdac_start_mid[FS_VCO2_INDEX], 1);
    cc112xSpiReadReg(CC112X_FS_VCO4, &calResults_for_vcdac_start_mid[FS_VCO4_INDEX], 1);
    cc112xSpiReadReg(CC112X_FS_CHP, &calResults_for_vcdac_start_mid[FS_CHP_INDEX], 1);

    // 9) Write back highest FS_VCO2 and corresponding FS_VCO and FS_CHP result
    if (calResults_for_vcdac_start_high[FS_VCO2_INDEX] > calResults_for_vcdac_start_mid[FS_VCO2_INDEX]) {
        writeByte = calResults_for_vcdac_start_high[FS_VCO2_INDEX];
        cc112xSpiWriteReg(CC112X_FS_VCO2, &writeByte, 1);
        writeByte = calResults_for_vcdac_start_high[FS_VCO4_INDEX];
        cc112xSpiWriteReg(CC112X_FS_VCO4, &writeByte, 1);
        writeByte = calResults_for_vcdac_start_high[FS_CHP_INDEX];
        cc112xSpiWriteReg(CC112X_FS_CHP, &writeByte, 1);
    }
    else {
        writeByte = calResults_for_vcdac_start_mid[FS_VCO2_INDEX];
        cc112xSpiWriteReg(CC112X_FS_VCO2, &writeByte, 1);
        writeByte = calResults_for_vcdac_start_mid[FS_VCO4_INDEX];
        cc112xSpiWriteReg(CC112X_FS_VCO4, &writeByte, 1);
        writeByte = calResults_for_vcdac_start_mid[FS_CHP_INDEX];
        cc112xSpiWriteReg(CC112X_FS_CHP, &writeByte, 1);
    }
}
```

Figure 1-2. Software Implementation

Known Design Exceptions to Functional Specifications

2.1 Advisory List

Extra Bit Transmitted for Sync Mode Configuration 6 and 7

Description:	When sync mode configuration 6 or 7 (SYNC_CFG0.SYNC_MODE = 110b or 111b) are used in TX mode the radio transmits 17 bits instead of 16. For both sync modes, SYNC23_16[0] is sent as the MSB of the sync word. SYNC_MODE = 110b: [SYNC23_16[0]:SYNC31_24:SYNC23_16] SYNC_MODE = 111b: [SYNC23_16[0]:SYNC15_8:SYNC7_0] In RX, the radio search for a 16-bit sync word [SYNC31_24:SYNC23_16] or [SYNC15_8:SYNC7_0].
Workaround(s):	SYNC_MODE = 101b can be used on the TX side to transmit a 16-bit sync word. [SYNC15_8:SYNC7_0] will then be sent.

Revision History

Revision	Date	Description
SWRZ039	2011-06-29	Initial release
SWRZ039A	2012-04-30	Added CC1125 and CC1175
SWRZ039B	2013-12-05	Added issue related to transmitting a 16 bits sync word
SWRZ039C	2014-01-06	Added note that VCO calibration bug is fixed on PARTVERSION 0x23
SWRZ039D	2015-04-23	Added note that the VCO calibration workaround for PARTVERSION 0x21 can also be used for PARTVERSION 0x23

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