

DATA SHEET

BT136X series D Triacs logic level

Product specification

June 2001



Triacs logic level

BT136X series D

GENERAL DESCRIPTION

Passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

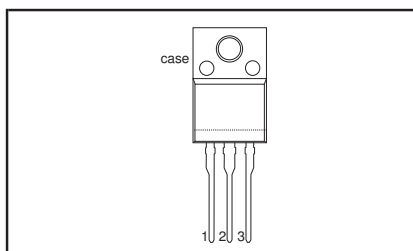
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DRM}	BT136X- Repetitive peak off-state voltages	600D 600	V
$I_{\text{T(RMS)}}$	RMS on-state current	4	A
I_{TSM}	Non-repetitive peak on-state current	25	A

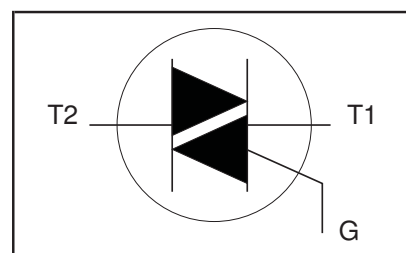
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DRM}	Repetitive peak off-state voltages		-	-600 600	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{HS}} \leq 92\text{ }^{\circ}\text{C}$	-	4	A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$ prior to surge	-	25	A
		$t = 20\text{ ms}$	-	27	A
		$t = 16.7\text{ ms}$	-	3.1	A ² s
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-		
dI_{T}/dt	Repetitive rate of rise of on-state current after triggering	$I_{\text{TM}} = 6\text{ A}$; $I_{\text{G}} = 0.2\text{ A}$; $dI_{\text{G}}/dt = 0.2\text{ A}/\mu\text{s}$	-		
		T2+ G+	-	50	A/ μs
		T2+ G-	-	50	A/ μs
		T2- G-	-	50	A/ μs
		T2- G+	-	10	A/ μs
I_{GM}	Peak gate current		-	2	A
V_{GM}	Peak gate voltage		-	5	V
P_{GM}	Peak gate power		-	5	W
$P_{\text{G(AV)}}$	Average gate power	over any 20 ms period	-	0.5	W
T_{stg}	Storage temperature		-40	150	$^{\circ}\text{C}$
T_{J}	Operating junction temperature		-	125	$^{\circ}\text{C}$

Triacs

logic level

BT136X series D

ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	$f = 50\text{--}60\text{ Hz}$; sinusoidal waveform; $R.H. \leq 65\%$; clean and dustfree	-	-	2500	V
C_{isol}	Capacitance from T2 to external heatsink	$f = 1\text{ MHz}$	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to heatsink	full or half cycle with heatsink compound	-	-	5.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	without heatsink compound in free air	-	55	7.2	K/W

STATIC CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$	-	2.0	5	mA
		T2+ G+	-	2.5	5	mA
		T2+ G-	-	2.5	5	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	1.6	10	mA
I_L	Latching current	$V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$	-	4.5	15	mA
		T2+ G+	-	1.2	10	mA
		T2+ G-	-	2.2	15	mA
		T2- G-	-	1.2	10	mA
		T2- G+	-	1.2	10	mA
I_H	Holding current	$V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$	-	1.4	1.70	V
V_T	On-state voltage	$I_T = 5\text{ A}$	-	0.7	1.5	V
V_{GT}	Gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$	-	0.4	-	V
I_D	Off-state leakage current	$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^{\circ}\text{C}$	0.25	0.1	0.5	mA
		$V_D = V_{DRM(max)}$; $T_j = 125\text{ }^{\circ}\text{C}$	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}$; $T_j = 125\text{ }^{\circ}\text{C}$; exponential waveform; $R_{GK} = 1\text{ k}\Omega$	-	5	-	V/ μs
t_{gt}	Gate controlled turn-on time	$I_{TM} = 6\text{ A}$; $V_D = V_{DRM(max)}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	μs

Triacs

logic level

BT136X series D

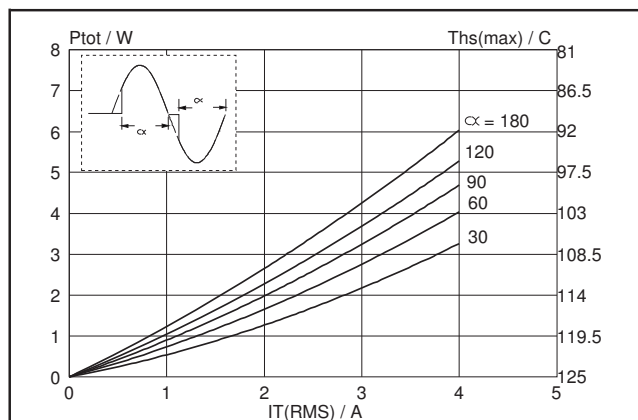


Fig.1. Maximum on-state dissipation, P_{tot} , versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

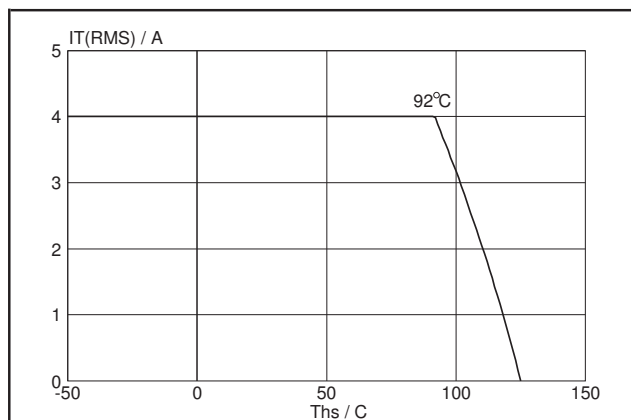


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs} .

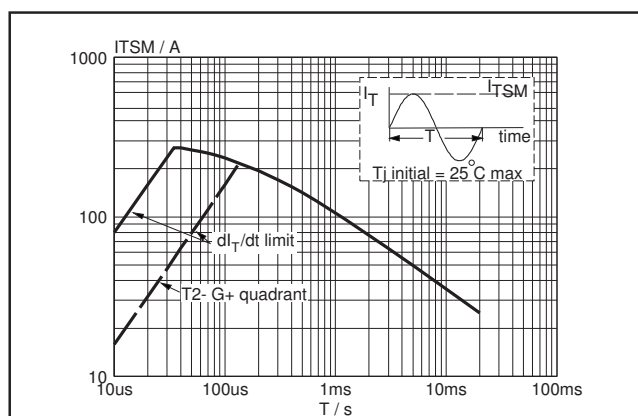


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 20\text{ms}$.

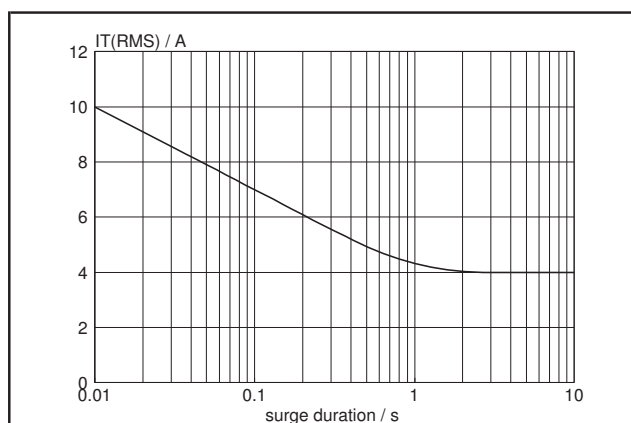


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50\text{ Hz}$; $T_{hs} \leq 92^\circ\text{C}$.

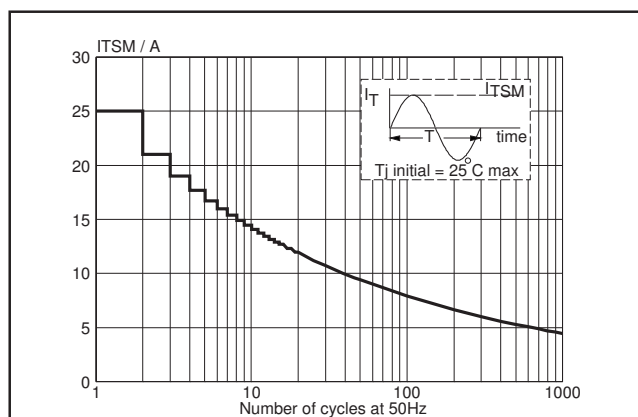


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50\text{ Hz}$.

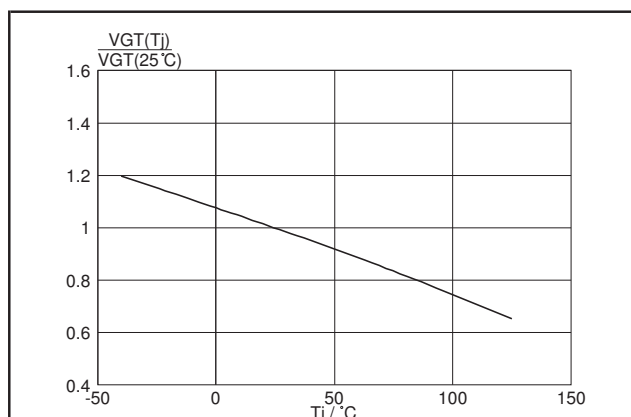
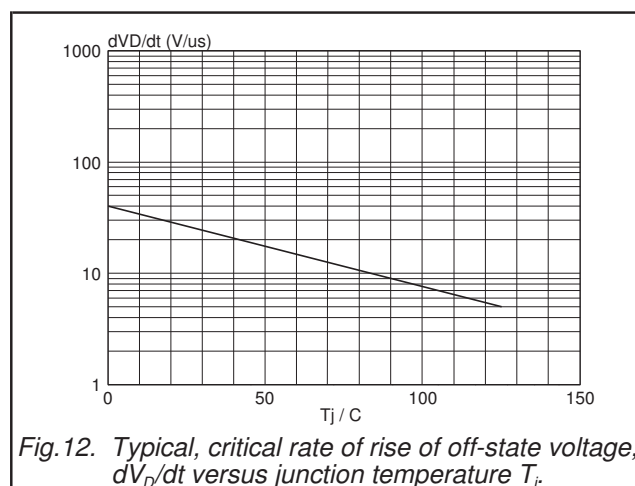
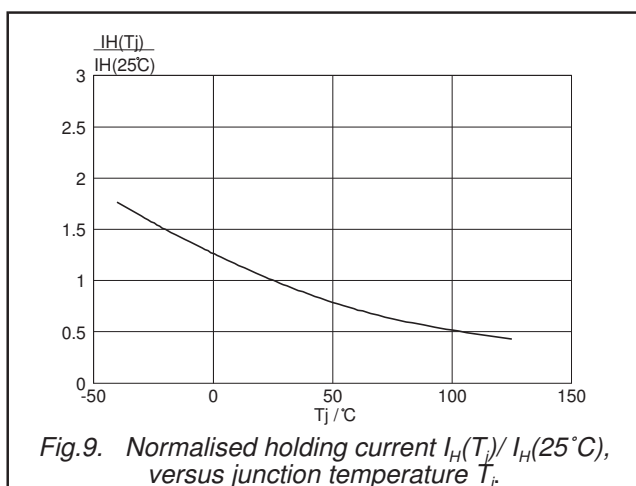
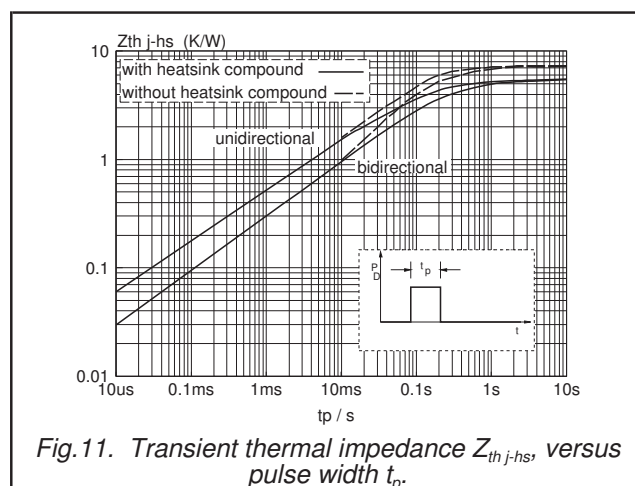
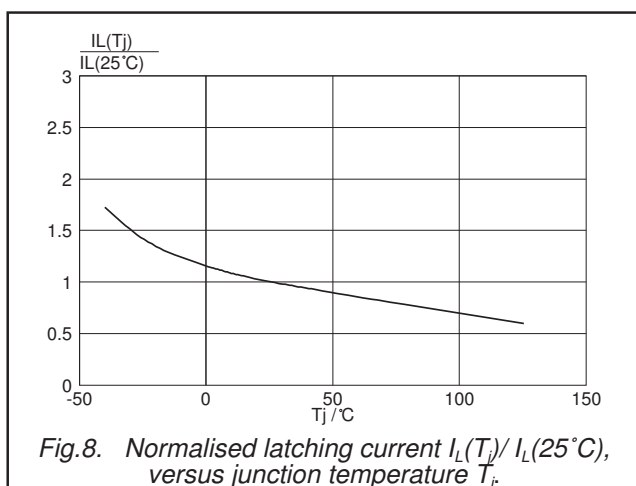
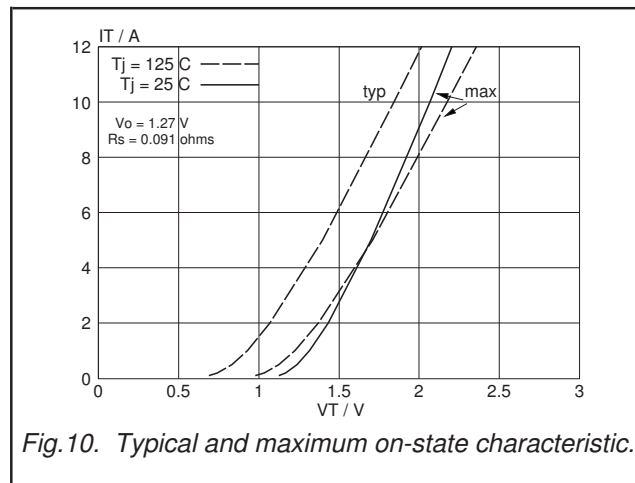
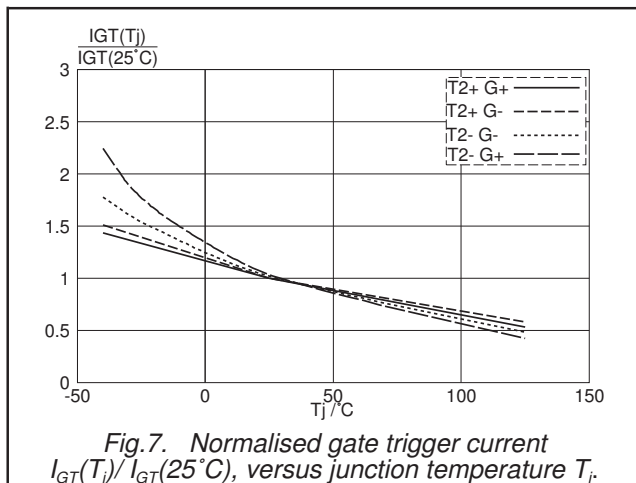


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

Triacs

logic level

BT136X series D



Triacs
logic level

BT136X series D

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

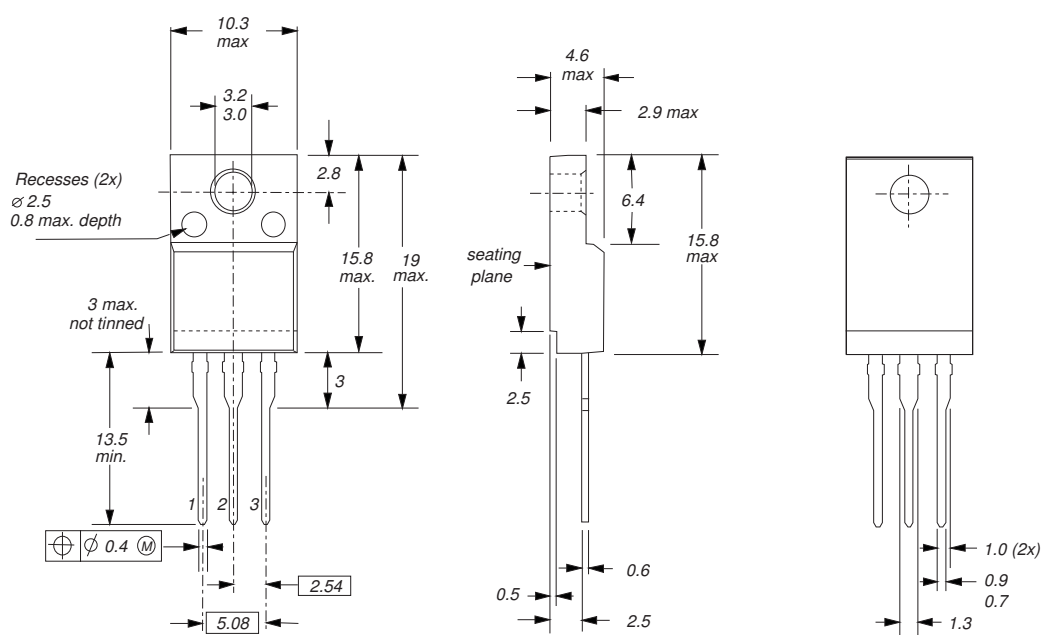


Fig. 13. SOT186A; The seating plane is electrically isolated from all terminals.

Notes

1. Refer to mounting instructions for F-pack envelopes.
2. Epoxy meets UL94 V0 at 1/8".

Legal information

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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For sales offices addresses send e-mail to: salesaddresses@nxp.com

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