TEA1713LT

Resonant power supply control IC with PFC

Rev. 1 — 24 June 2011 Product data sheet

1. General description

The TEA1713LT integrates a Power Factor Corrector (PFC) controller and a controller for a Half-Bridge resonant Converter (HBC) in a multi-chip IC. It provides the drive function for the discrete MOSFET in an up-converter and for the two discrete power MOSFETs in a resonant half-bridge configuration.

The efficient operation of the PFC is achieved by implementing functions such as quasi-resonant operation at high power levels and quasi-resonant operation with valley skipping at lower power levels. OverCurrent Protection (OCP), OverVoltage Protection (OVP), and demagnetization sensing ensure safe operation under all conditions.

The HBC module is a is a high-voltage controller for a zero-voltage switching LLC resonant converter. It contains a high-voltage level shift circuit and several protection circuits including OverCurrent Regulation (OCR), open-loop protection, capacitive mode protection and a general purpose latched protection input.

The high-voltage chip is fabricated using a proprietary high-voltage Bipolar-CMOS-DMOS power logic process that enables efficient direct start-up from the rectified universal mains voltage. The low-voltage Silicon On Insulator (SOI) chip is used for accurate, high-speed protection functions and control.

The topology of a PFC circuit and a resonant converter controlled by the TEA1713LT is very flexible, enabling it to be used in a broad range of applications with a wide mains voltage range. Combining PFC and HBC controllers in a single IC makes the TEA1713LT ideal for controlling power supplies in LCD and plasma televisions.

Highly efficient and reliable power supplies providing over 100 W can be designed easily using the TEA1713LT, with a minimum of external components.

2. Features and benefits

2.1 General features

- Integrated PFC and HBC controllers
- Universal mains supply operation (70 V to 276 V (AC))
- High level of integration resulting in a low external component count and a cost effective design
- Enable input (enable only PFC or both PFC and HBC controllers)
- On-chip high-voltage start-up source
- Stand-alone operation or IC supplied from external DC source

2.2 PFC controller features

- Boundary mode operation with on-time control
- Valley/zero voltage switching for minimum switching losses
- Frequency limiting to reduce switching losses
- Accurate boost voltage regulation
- Burst mode switching with soft start and soft stop

2.3 HBC controller features

- Integrated high-voltage level shifter
- Adjustable minimum and maximum frequency
- Maximum 500 kHz half-bridge switching frequency
- Adaptive non-overlap time
- Burst mode switching

2.4 Protection features

- Safe restart mode for system fault conditions
- General latched protection input for output overvoltage protection or external temperature protection
- Protection timer for time-out and shutdown
- Overtemperature protection
- Soft (re)start for both controllers
- Undervoltage protection for mains (brownout), boost, IC supply and output voltage
- Overcurrent regulation and protection for both controllers
- Accurate overvoltage protection for boost voltage
- Capacitive mode protection for HBC controller

3. Applications

- LCD television
- Plasma television
- Adapters

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4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1713LT	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

5. Block diagram

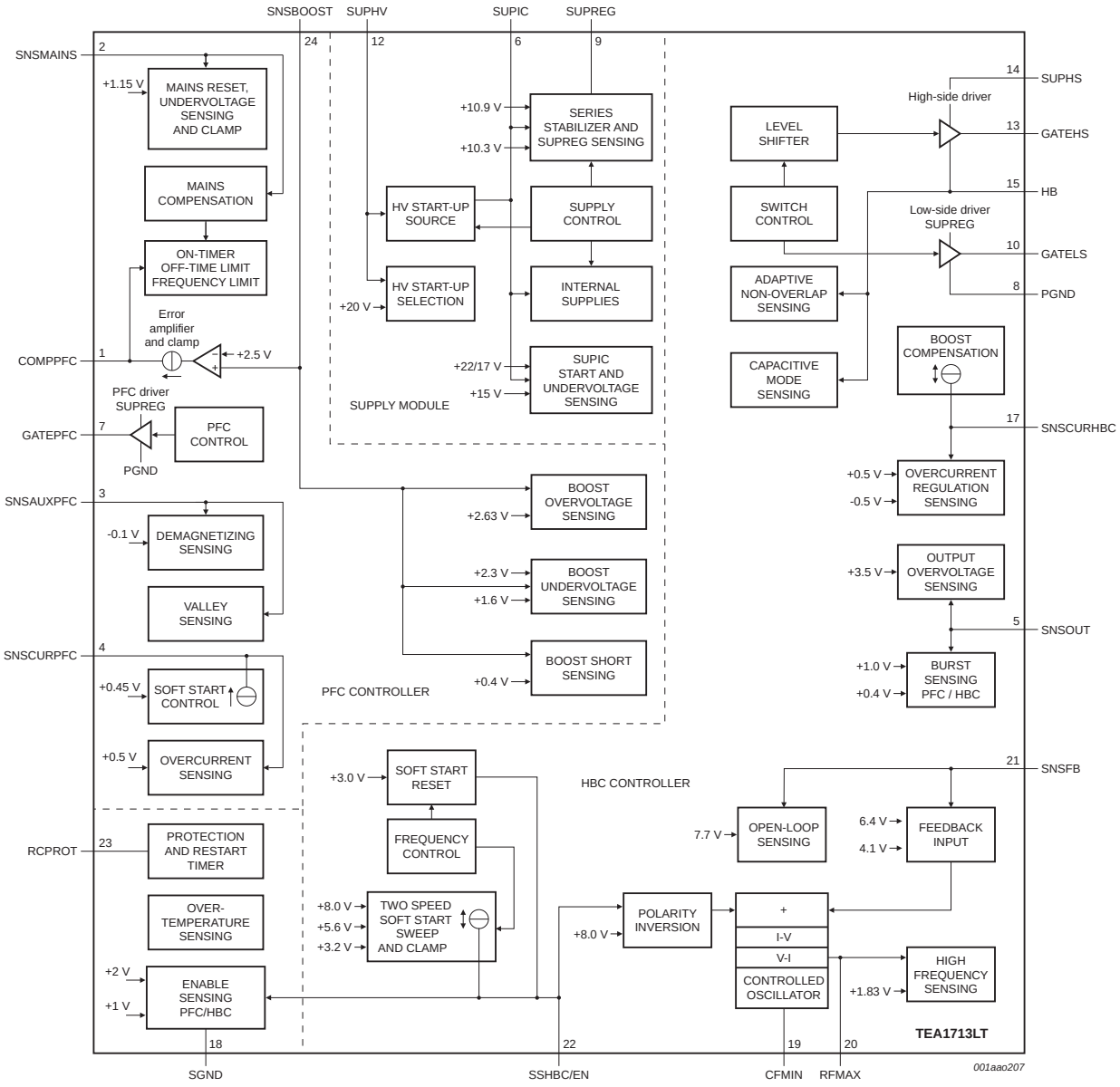

Fig 1. Block diagram of TEA1713LT

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6. Pinning information

6.1 Pinning

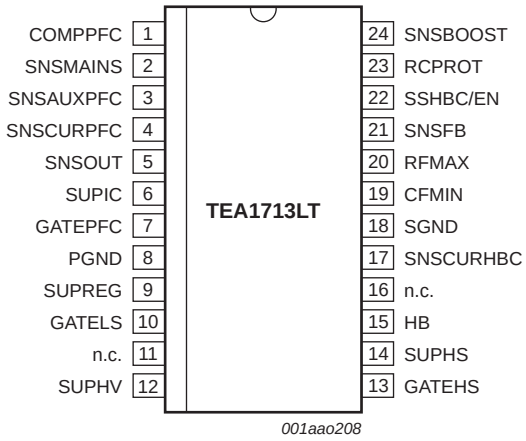

Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
COMPPFC	1	frequency compensation for PFC controller; externally connected to filter
SNSMAINS	2	sense input for mains voltage; externally connected to resistive divided mains voltage
SNSAUXPFC	3	sense input for PFC demagnetization timing; externally connected to auxiliary winding of PFC
SNSCURPFC	4	sense input for momentary current and soft start of the PFC controller; externally connected to current sense resistor and soft start filter
SNSOUT	5	sense input for monitoring the output voltage of the HBC; externally connected to the auxiliary winding; sense input for burst mode of HBC controller or PFC and HBC controllers
SUPIC	6	low-voltage supply for SUPIC input; output of internal HV start-up source; externally connected to auxiliary winding of HBC or to external DC supply
GATEPFC	7	gate driver output for PFC MOSFET
PGND	8	power ground; reference (ground) for HBC low-side and PFC driver
SUPREG	9	regulated SUPREG IC supply; output from internal regulator; input for drivers; externally connected to SUPREG buffer capacitor
GATELS	10	gate driver output for low-side MOSFET of HBC
n.c.	11	not connected; high-voltage spacer.
SUPHV	12	high-voltage supply input for internal HV start-up source; externally connected to boost voltage
GATEHS	13	gate driver output for high-side MOSFET of HBC
SUPHS	14	high-side driver supply input; externally connected to bootstrap capacitor (C_{SUPHS})

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Table 2. Pin description *...continued*

Symbol	Pin	Description
HB	15	reference for high-side driver; input for half-bridge slope detection; externally connected to half-bridge node HB between HBC MOSFETs (see Figure 19)
n.c.	16	not connected; high-voltage spacer
SNSCURHBC	17	sense input for momentary HBC current; externally connected to resonant current sense resistor
SGND	18	signal ground; reference (ground) for IC.
CFMIN	19	minimum frequency setting for HBC; externally connected to capacitor
RFMAX	20	maximum frequency setting for HBC; externally connected to resistor
SNSFB	21	sense input for output voltage regulation feedback; externally connected to opto-coupler
SSHBC/EN	22	combined soft start timing of HBC and IC enable input; enabling of PFC or PFC and HBC controllers; externally connected to soft start capacitor and enable pull-down signal
RCPROT	23	protection timer setting for time-out and restart; externally connected to resistor and capacitor
SNSBOOST	24	sense input for boost voltage; externally connected to resistive divided boost voltage

7. Functional description

7.1 Overview of IC modules

The functionality of the TEA1713LT can be grouped as follows:

- Supply module:

  Supply management for the IC; includes the restart and (latched) shutdown states
- Protection and restart timer:

  Externally adjustable timer used for delayed protection and restart timing
- Enable input:

  Control input for enabling and disabling the controllers; very low current consumption when disabled
- PFC controller:

  Controls and protects the power factor converter; generates a 400 V (DC) boost voltage from the rectified AC mains input with a high power factor
- HBC controller:

  Controls and protects the resonant converter; generates a regulated (mains isolated) output voltage from the 400 V (DC) boost voltage

Figure 1 shows the block diagram of the TEA1713LT. A typical application is illustrated in Figure 19.

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7.2 Power supply

The TEA1713LT contains several supply related pins.

7.2.1 Low-voltage supply input (pin SUPIC)

The SUPIC pin is the main low-voltage supply input to the IC. All internal circuits (other than the high voltage circuit) are directly or indirectly (via SUPREG) supplied from this pin. SUPIC is connected externally to a buffer capacitor C_{SUPIC}. This buffer capacitor can be charged in several ways:

- from the internal high voltage start-up source
- from the auxiliary winding of the HBC transformer
- from the capacitive supply of the switching half-bridge node
- from an external DC supply, e.g. a standby supply

The IC starts operating when voltage on SUPIC reaches the start level, provided that the voltage on SUPREG has also reached the start level. The start level depends on the condition of the SUPHV pin:

- High voltage present on SUPHV, $V_{SUPHV} > V_{det(SUPHV)}$.

  This is the case with a stand-alone application where C_{SUPIC} is initially charged from the HV start-up source. The start level is $V_{start(hvd)(SUPIC)}$ (typ. 22 V). The wide difference between the start and stop ($V_{uvp(SUPIC)}$) levels allows energy to be stored in the SUPIC buffer capacitor which is used to supply the IC until the output voltage has stabilized.
- Not connected or no voltage present at SUPHV, $V_{SUPHV} < V_{det(SUPHV)}$.

  This is the case when the TEA1713LT is supplied from an external DC source. The start level is $V_{start(nohvd)(SUPIC)}$ (typ. 17 V). The IC is supplied from the DC supply during start-up. To minimize power dissipation, the DC supply to pin SUPIC should be above, but close to, $V_{uvp(SUPIC)}$ (typ. 15 V).

The IC will stop operating when V_{SUPIC} drops below $V_{uvp(SUPIC)}$. This is the SUPIC UnderVoltage Protection (UVP) voltage (UVP-SUPIC; see Section 7.9). The PFC controller will stop switching immediately, but the HBC controller will continue operating until the low-side MOSFET becomes active.

The current consumption depends on the state of the IC. The TEA1713LT operating states are described in Section 7.3.

- Disabled IC state

  When the IC is disabled via the SSHBC/EN pin, the current consumption is very low ($I_{dism(SUPIC)}$).
- SUPIC charge, SUPREG charge, Thermal hold, Restart and Protection shutdown states

  Only a small section of the IC is active while C_{SUPIC} and C_{SUPREG} are charging during a restart sequence prior to start-up or during shutdown after a protection function has been activated. The PFC and HBC controllers are disabled. Current consumption is limited to $I_{protm(SUPIC)}$.

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- Boost charge state

  The PFC controller is switching; the HBC controller is off. The current from the high voltage start-up source is large enough to supply SUPIC (current consumption < $I_{ch(nom)(SUPIC)}$).
- Operational supply state

  Both the PFC and HBC controllers are switching. Current consumption is $I_{oper(SUPIC)}$. When the HBC controller is enabled, the switching frequency will be high initially and the current consumption of the HBC MOSFET drivers will be dominant. The stored energy in C_{SUPIC} will supply the initial SUPIC current before the SUPIC supply source takes over.

Pin SUPIC has a low short-circuit detection voltage ($V_{scp(SUPIC)}$; typ. 0.65 V). The current dissipated in the HV start-up source is limited while $V_{SUPIC} < V_{scp(SUPIC)}$ (see Section 7.2.4).

7.2.2 Regulated supply (pin SUPREG)

The voltage range on pin SUPIC exceeds that of the gate voltages of the external MOSFETs. For this reason, the TEA1713LT contains an integrated series stabilizer. The series stabilizer creates an accurate regulated voltage ($V_{reg(SUPREG)}$; typ. 10.9 V) at the buffer capacitor C_{SUPREG}. This stabilized voltage is used to:

- supply the internal PFC driver
- supply the internal low-side HBC driver
- supply the internal high-side driver via external components
- as a reference voltage for optional external circuits

The SUPREG series stabilizer is enabled after C_{SUPIC} has been fully charged. This ensures that any optional external circuitry connected to SUPREG will not dissipate any of the start-up current.

To ensure that the external MOSFETs receive sufficient gate drive current, the voltage on SUPREG must reach $V_{start(SUPREG)}$ (and the voltage on SUPIC must reach the start level) before the IC starts operating.

SUPREG is provided with undervoltage protection (UVP-SUPREG; see Section 7.9). When V_{SUPREG} falls below $V_{uvp(SUPREG)}$ (typ. 10.3 V), two events will be triggered:

- The IC will stop operating to prevent unreliable switching because the gate driver voltage is too low. The PFC controller will stop switching immediately, but the HBC controller will continue until the low-side stroke is active.
- The maximum current from the internal SUPREG series stabilizer is reduced to $I_{ch(red)(SUPREG)}$ (typ. 5.4 mA). This will reduce the dissipation in the series stabilizer in the event of an overload at SUPREG while SUPIC is supplied from an external DC source.

7.2.3 High-side driver floating supply (pin SUPHS)

The high-side driver is supplied by an external bootstrap buffer capacitor, C_{SUPHS}. The bootstrap capacitor is connected between the high-side reference pin HB and the high-side driver supply input pin SUPHS. C_{SUPHS} is charged from pin SUPREG via an

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external diode D_{SUPHS}. The voltage drop between SUPREG and SUPHS can be minimized by carefully selecting the appropriate diode, especially when using large MOSFETs and high switching frequencies.

7.2.4 High voltage supply input (pin SUPHV)

In a stand-alone power supply application, this pin is connected to the boost voltage. C_{SUPIC} and C_{SUPREG} will be charged by the HV start-up source (which delivers a constant current from SUPHV to SUPIC) via this pin.

Short-circuit protection on pin SUPIC (SCP-SUPIC; see Section 7.9) limits the dissipation in the HV start-up source when SUPIC is shorted to ground and limits the current on SUPHV (to $I_{red(SUPHV)}$) as long as the voltage on SUPIC is below $V_{scp(SUPIC)}$.

Under normal operating conditions, the voltage on pin SUPIC will exceed $V_{scp(SUPIC)}$ very quickly after start-up and the HV start-up source will switch to the nominal current $I_{nom(SUPHV)}$.

During start-up and restart, the HV start-up source will charge C_{SUPIC} and regulate the voltage on SUPIC by hysteretic control. So the start level has a small degree of hysteresis $V_{start(hys)(SUPIC)}$. The HV start-up source switches-off when V_{SUPIC} exceeds the start level $V_{start(hvd)(SUPIC)}$. Current consumption through pin SUPHV will be low ($I_{tko(SUPHV)}$).

Once start-up is complete and the HBC controller is operating, SUPIC can be supplied from the auxiliary winding of the HBC transformer. In this operational state, the HV start-up source is disabled.

7.3 Flow diagram

The operation of the TEA1713LT can be divided into a number of states - see Figure 3. The abbreviations used in Figure 3 are explained In Table 8.

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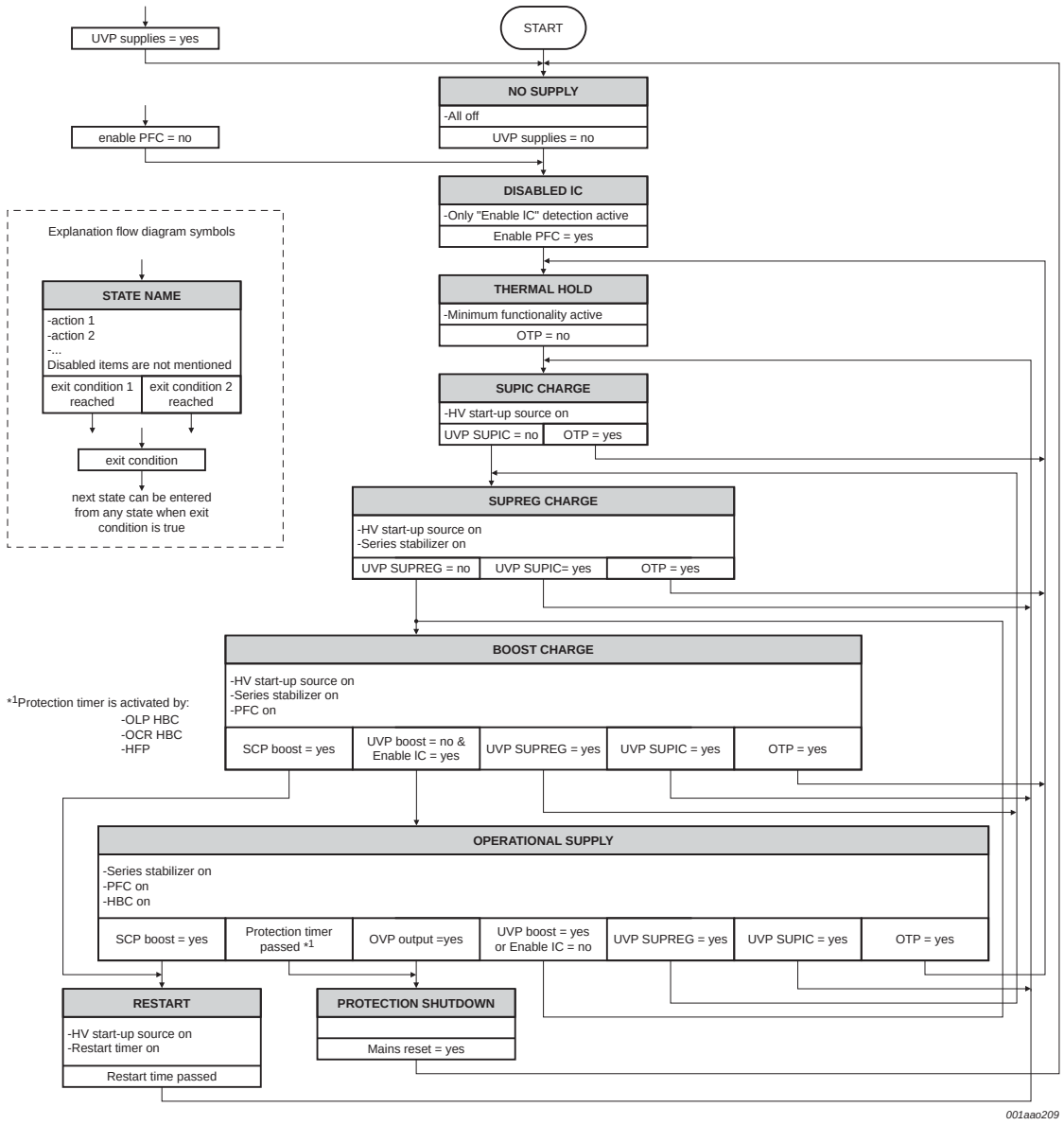

Fig 3. Flow diagram of the TEA1713LT

Table 3. Operating states

State	Description
No supply	Supply voltages on SUPIC and SUPHV are too low to provide any functionality. Undervoltage protection (UVP-supplies; see Section 7.9) is active when $V_{SUPHV} < V_{rst(SUPHV)}$ and $V_{SUPIC} < V_{rst(SUPIC)}$. The IC is reset.
Disabled IC	IC is completely disabled because pin SSHBC/EN is LOW.
Thermal hold	Activated as long as OTP is active. IC is not operating. PFC and HBC controllers are disabled and C_{SUPIC} and C_{SUPREG} are not charged.
SUPIC charge	IC supply capacitor (C_{SUPIC}) is charged by HV start-up source. C_{SUPREG} is not charged.
SUPREG charge	Stabilized supply capacitor (C_{SUPREG}) is charged by series regulator.

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Table 3. Operating states *...continued*

State	Description
Boost charge	Boost voltage is built up by operational PFC.
Operational supply	Output voltage is generated. Both PFC and HBC controllers are fully operational.
Restart	Activated when a protection function is triggered. Restart timer is activated. During this time, PFC and HBC controllers are disabled and C_{SUPREG} is not charged. C_{SUPIC} is charged.
Protection shutdown	Activated when a protection function is triggered. IC is not operational. PFC and HBC controllers are disabled and C_{SUPIC} and C_{SUPREG} are not charged.

7.4 Enable input (pin SSHBC/EN)

The power supply application can be completely disabled by pulling pin SSHBC/EN LOW.

Figure 4 illustrates the internal functionality. When a voltage is present on pin SUPHV or on pin SUPIC, a current $I_{pu(EN)}$ (typ. 42 μA) flows out of SSHBC/EN. If the pin is not pulled-down, this current will lift the voltage up to $V_{pu(EN)}$ (typ. 3 V). Since this voltage is above both $V_{en(PFC)(EN)}$ (typ. 1.2 V) and $V_{en(IC)(EN)}$ (typ. 2.2 V), the IC will be completely enabled.

The IC can be completely disabled by pulling the voltage on SSHBC/EN down below both $V_{en(PFC)(EN)}$ and $V_{en(IC)(EN)}$ via an opto-coupler driven from the secondary side of the HBC transformer (see Figure 4). The PFC controller will stop switching immediately, but the HBC controller will continue switching until the low-side stroke is active. It is also possible to control the voltage on SSHBC/EN from another circuit on the secondary side via a diode. The external pull-down current must be larger than the internal soft start charge current $I_{ss(hf)(SSHBC)}$.

If the voltage on SSHBC/EN is pulled down below $V_{en(IC)(EN)}$, but not below $V_{en(PFC)(EN)}$, only the HBC will be disabled. This feature can be useful when another power converter is connected to the boost voltage of the PFC.

The low-side power switch of the HBC will be on when the HBC is disabled via the SSHBC/EN pin.

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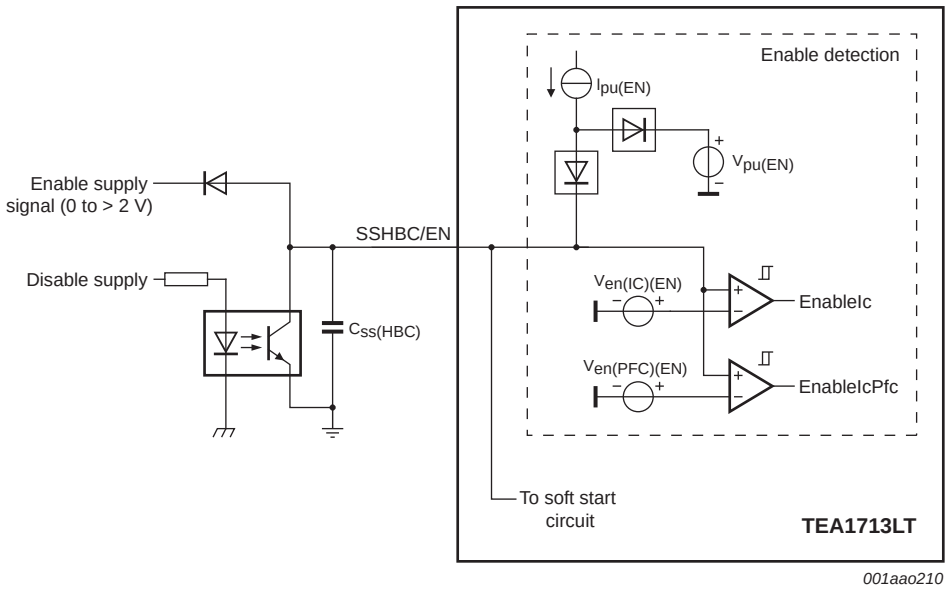

Fig 4. Circuit configuration around pin SSHBC/EN

7.5 IC protection

7.5.1 IC restart and shutdown

In addition to the protection functions that influence the operation of the PFC and HBC controllers, a number of protection functions are provided that disable both controllers. See the protection overview in Section 7.9 for details on which protections trigger a restart or a protection shutdown.

- Restart

  When the TEA1713LT enters the Restart state, the PFC and HBC controllers are switched off. After a period defined by the Restart timer, the IC automatically restarts following the normal start-up cycle.

- Protection shutdown

  When the TEA1713LT enters the Protection shutdown state, the PFC and HBC controllers are switched off. The Protection shutdown state is latched, so the IC will not start up again automatically. It can be restarted by resetting the Protection shutdown state in one of the following ways:

  – by lowering V_{SUPIC} and V_{SUPHV} below their respective reset levels, $V_{rst(SUPIC)}$ and $V_{rst(SUPHV)}$
  – via a fast shutdown reset (see Section 7.5.3).
  – via the enable pin (see Section 7.4)

- Thermal hold

  In the Thermal hold state, the PFC and HBC controllers are switched off. The Thermal hold state remains active until the IC junction temperature drops to about 10 °C below T_{otp} (see Section 7.5.5).

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7.5.2 Protection and restart timer

The TEA1713LT contains a programmable timer which can be used for timing several protection functions. The timer can be used in two ways - as a protection timer and as a restart timer. The timing of the timers can be set independently via an external resistor R_{prot} and capacitor C_{prot} connected to pin RCPROT.

7.5.2.1 Protection timer

Certain error conditions can be allowed to persist for a period of time before protective action needs to be taken. The protection timer defines the protection period - how long the error is allowed to persist before the protection function is triggered. The protection functions that use the protection timer can be found in the protection overview in Section 7.9.

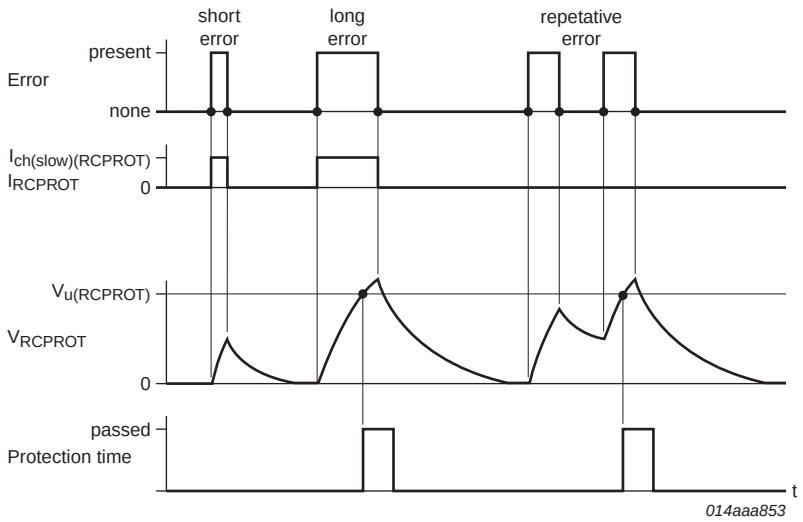

Fig 5. Operation of the protection timer

Figure 5 shows the operation of the protection timer. When an error condition occurs, a fixed current $I_{ch(slow)(RCPROT)}$ (typ. 100 μA) flows out of the RCPROT pin and charges C_{prot}. R_{prot} will cause the voltage to rise exponentially. The protection time has elapsed when the voltage on RCPROT reaches the upper switching level $V_{u(RCPROT)}$ (typ. 4 V). At this instant, the appropriate protective action is taken and C_{prot} is discharged.

If the error condition is removed before the voltage on RCPROT reaches $V_{u(RCPROT)}$, C_{prot} is discharged via R_{prot} and no action is taken.

The voltage on RCPROT may be raised above $V_{u(RCPROT)}$ by an external circuit to force a protection shutdown.

7.5.2.2 Restart timer

Certain error conditions require the IC to be disabled for a period of time, particularly when the error condition can cause components to overheat. In such cases, the IC should be disabled to allow the power supply to cool down, before restarting automatically. The restart time is determined by the restart timer. The restart timer is active in the Restart state. The protection functions that trigger a restart can be found in the protection overview in Section 7.9.

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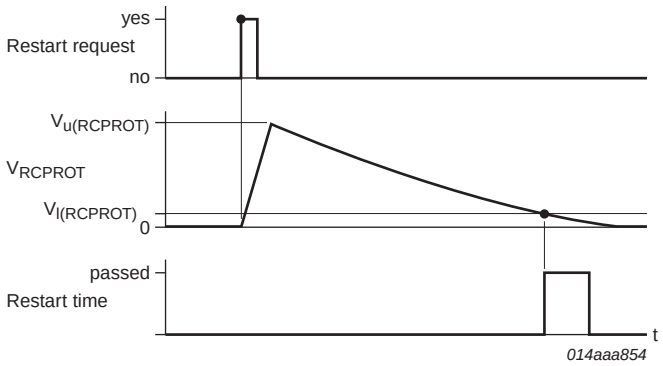

Fig 6. Operation of the restart timer

Figure 6 shows the operation of the restart timer. Normally C_{prot} is discharged to 0 V. When a restart is requested, C_{prot} is quickly charged to the upper switching level $V_{u(RCPROT)}$. Then the RCPROT pin becomes high ohmic and C_{prot} discharges through R_{prot}. The restart time has elapsed when V_{RCPROT} reaches the lower switching level $V_{l(RCPROT)}$ (typ. 0.5 V). The IC then restarts and C_{prot} is discharged.

7.5.3 Fast shutdown reset (pin SNSMAINS)

The latched Protection shutdown state will be reset when V_{SUPIC} and V_{SUPHV} drop below their respective reset levels, $V_{rst(SUPIC)}$ and $V_{rst(SUPHV)}$. Typically, the PFC boost capacitor, C_{boost}, will need to discharge before V_{SUPIC} and V_{SUPHV} drop below their reset levels, which can take a long time.

Fast shutdown reset facilitates a faster reset. When the mains supply is interrupted, the voltage on pin SNSMAINS will fall. As soon as $V_{SNSMAINS}$ falls below $V_{rst(SNSMAINS)}$ and subsequently rises again by a hysteresis value, the IC will leave the Protection shutdown state. The boost capacitor C_{boost} does not need to be discharged to initiate a new start-up.

The Protection shutdown state can also be ended by pulling down the enable input (pin SSHBC/EN).

7.5.4 Output overvoltage protection (pin SNSOUT)

The TEA1713LT outputs are provided with overvoltage protection (OVP-output; see Section 7.9). The output voltage can be measured via the auxiliary winding of the resonant transformer. This voltage can be sensed at the SNSOUT pin via an external rectifier and resistive divider. An overvoltage is detected when the SNSOUT voltage exceeds $V_{ovp(SNSOUT)}$ (typ. 3.5 V). Once an overvoltage has been detected, the TEA1713LT will go to the Protection shutdown state.

Additional external protection circuits, such as an external overtemperature protection circuit, can be connected to this pin. They should be connected to pin SNSOUT via a diode so that the error condition will trigger an OVP event.

7.5.5 OverTemperature Protection (OTP)

Accurate internal overtemperature protection is provided in the TEA1713LT. When the junction temperature exceeds the overtemperature protection activation temperature, T_{otp} (typ. 150 °C), the IC will go to the Thermal hold state. The TEA1713LT will exit the Thermal hold state when the temperature falls again, to around 10 °C below T_{otp}.

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7.6 Burst mode operation (pin SNSOUT)

The HBC and PFC controllers can be operated in Burst mode. In Burst mode the controllers will be on for a period, then off for a period. Burst mode operation increases efficiency under low-load conditions.

A low-load condition can be detected using a simple external circuit that makes use of the information from the feedback loop or from the average primary current. The detection circuit can pull down pin SNSOUT to pause operation of the TEA1713LT for a burst-off time. Both controllers, or only the HBC controller, can be paused during the burst-off time:

- Burst-off level for HBC, $V_{burst(HBC)}$ (typ. 1 V).

  When V_{SNSOUT} drops below $V_{burst(HBC)}$, operation of the HBC controller will be suspended. Both the high-side and the low-side power switches will be off. The PFC continues to operate normally. When V_{SNSOUT} rises above $V_{burst(HBC)}$ again, the HBC controller will resume normal operation, without executing a soft start sequence.
- Burst-off level for PFC, $V_{burst(PFC)}$ (typ. 0.4 V).

  When V_{SNSOUT} drops below $V_{burst(PFC)}$, operation of the PFC controller will also be suspended (the HBC will have been paused already). When V_{SNSOUT} rises above $V_{burst(PFC)}$ again, the PFC controller will resume normal operation via a PFC soft start (see Section 7.7.6).

To ensure Burst mode is not activated before the output voltage becomes valid, a current from the SNSOUT pin (typ. 100 μA) will hold V_{SNSOUT} at $V_{pu(SNSOUT)}$, which is above both burst levels. The resistance between the SNSOUT pin and ground should therefore be greater than 20 kΩ.

7.7 PFC controller

The PFC controller converts the rectified universal mains voltage into an accurately regulated boost voltage of 400 V (DC). It operates in quasi-resonant or discontinuous conduction mode and is controlled via an on-time control system. The resulting mains harmonic current emissions of a typical application will easily meet the class-D MHR requirements.

The PFC controller uses valley switching to minimize losses. A primary stroke is only started once the previous secondary stroke has ended and the voltage across the PFC MOSFET has reached a minimum value.

7.7.1 PFC gate driver (pin GATEPFC)

The circuit driving the gate of the power MOSFET has a high current sourcing capability $I_{source(GATEPFC)}$ (typ. 500 mA) and a high current sink capability $I_{sink(GATEPFC)}$ (typ. 1.2 A). This permits fast turn-on and turn-off of the power MOSFET to ensure efficient operation. The driver is supplied from the regulated SUPREG supply.

7.7.2 PFC on-time control

The PFC operates under on-time control. The on-time of the PFC MOSFET is determined by:

- The error amplifier and the loop compensation via the voltage on pin COMPPFC

  At $V_{ton(COMPPFC)zero}$ (typ. 3.5 V), the on-time is reduced to zero. At $V_{ton(COMPPFC)max}$ the on-time is at a maximum

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- Mains compensation via the voltage on pin SNSMAINS

7.7.2.1 PFC error amplifier (pins COMPPFC and SNSBOOST)

The boost voltage is divided via a high-ohmic resistive divider. It is fed to the SNSBOOST pin. The transconductance error amplifier, which compares the SNSBOOST voltage with an accurate trimmed reference voltage $V_{reg(SNSBOOST)}$, is connected to this pin. The output current is filtered by the external loop compensation network at the COMPPFC pin. In a typical application, the bandwidth of the regulation loop is set by a resistor and two capacitors.

The COMPPFC voltage is clamped at a maximum of $V_{clamp(COMPPFC)}$. This avoids a long recovery time in the event that the boost voltage rises above the regulation level for a period of time.

7.7.2.2 PFC mains compensation (pin SNSMAINS)

The mathematical equation for the transfer function of a power factor corrector contains the square of the mains input voltage. In a typical application, this will result in a low bandwidth for low mains input voltages, while at high mains input voltages the MHR requirements may be hard to meet.

The TEA1713LT contains a correction circuit to compensate for this effect. The average mains voltage is measured via the SNSMAINS pin and this information is fed to an internal compensation circuit. Figure 7 illustrates the relationship between the SNSMAINS voltage, the COMPPFC voltage, and the on-time. This compensation makes it is possible to keep the regulation loop bandwidth constant over the full mains input range, yielding a fast transient response on load steps, while still complying with class-D MHR requirements.

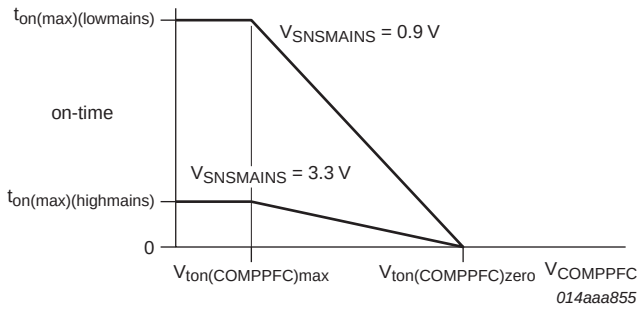

Fig 7. Relationship between on-time, SNSMAINS voltage and COMPPFC voltage

7.7.3 PFC demagnetization sensing (pin SNSAUXPFC)

The voltage on the SNSAUXPFC pin is used to detect transformer demagnetization. During the secondary stroke, the transformer is magnetized and current flows in the boost output. During this time, $V_{SNSAUXPFC} < V_{demag(SNSAUXPFC)}$ (typ. −100 mV) and the PFC MOSFET is kept off.

After some time, the transformer becomes demagnetized and current stops flowing in the boost output. From that moment, $V_{SNSAUXPFC} > V_{demag(SNSAUXPFC)}$ and valley detection is started. The MOSFET remains off.

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To ensure switching continues under all circumstances, the MOSFET is forced to switch on if the magnetizing of the transformer ($V_{SNSAUXPFC} < V_{demag(SNSAUXPFC)}$) is not detected within $t_{to(mag)}$ (typ. 50 μs) after GATEPFC goes LOW.

It is recommended that a 5 kΩ series resistor be connected to this pin to protect the internal circuitry, against lightning for example. The resistor should be placed close to the IC on the printed circuit board to prevent incorrect switching due to external disturbances.

7.7.4 PFC valley sensing (pin SNSAUXPFC)

The PFC MOSFET is switched on for the next stroke to reduce switching losses and EMI if the voltage at the drain of the MOSFET is at its minimum (valley switching), see Figure 8.

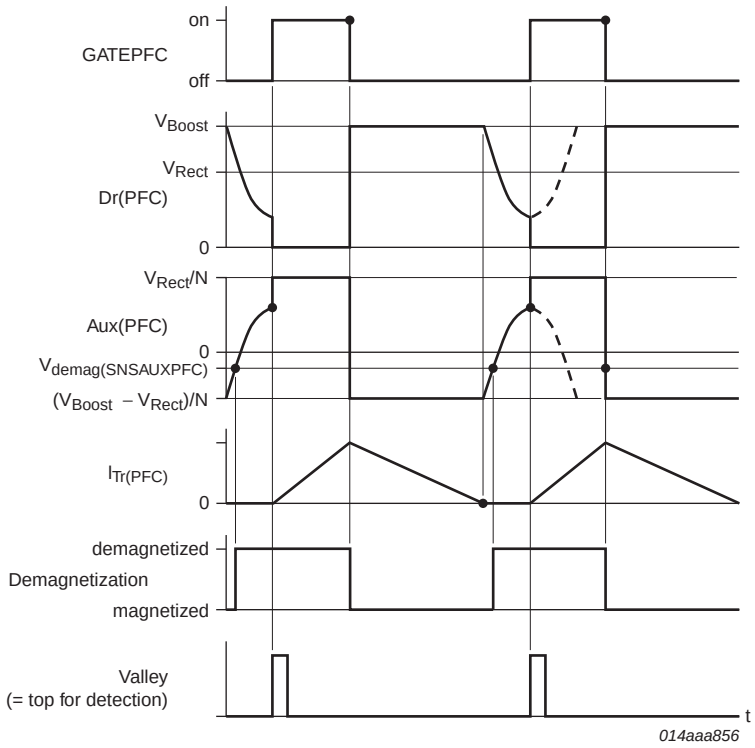

Fig 8. Demagnetization and valley detection

Valleys are detected by the valley sensing block connected to the SNSAUXPFC pin. This block measures the voltage at the auxiliary winding of the PFC transformer, which is a reduced and inverted copy of the MOSFET drain voltage. When a valley of the drain voltage (= top at SNSAUXPFC voltage) is detected, the MOSFET is switched on.

If no top is detected on the SNSAUXPFC pin (= valley at the drain) within $t_{to(vrec)}$ (typ. 4 μs) after demagnetization was detected, the MOSFET is forced to switch on.

7.7.5 PFC frequency and off-time limiting

For transformer optimization and to minimize switching losses, the switching frequency is limited to $f_{max(PFC)}$. If the frequency for quasi-resonant operation is above $f_{max(PFC)}$, the system will switch to Discontinuous conduction mode. The PFC MOSFET is switched on when the drain-source voltage is at a minimum (valley switching).

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The minimum off-time is limited to $t_{off(PFC)min}$ to ensure proper control of the PFC MOSFET under all circumstances.

7.7.6 PFC soft start and soft stop (pin SNSCURPFC)

The PFC controller features a soft start function which slowly increases the primary peak current at start-up and a soft stop function which slowly decreases the transformer peak current, before operations are halted. This is to prevent transformer rattle at start-up or during Burst mode operation.

This is achieved by connecting a resistor $R_{ss(PFC)}$ and a capacitor $C_{ss(PFC)}$ between pin SNSCURPFC and the current sense resistor $R_{cur(PFC)}$. At start-up, an internal current source $I_{ch(ss)(PFC)}$ charges the capacitor to $V_{SNSCURPFC} = I_{ch(ss)(PFC)} \times R_{ss(PFC)}$. The voltage is limited to the maximum PFC soft start clamp voltage, $V_{clamp(ss)PFC}$. The additional voltage across the charged capacitor results in a reduced peak current. After start-up, the internal current source is switched-off, capacitor $C_{ss(PFC)}$ discharges across $R_{ss(PFC)}$ and the peak current increases.

The start level and the time constant of the rising primary current can be adjusted externally by changing the values of $R_{ss(PFC)}$ and $C_{ss(PFC)}$.

$$I_{Cur(PFC)(pk)} = \frac{V_{ocr(PFC)} - (I_{ch(ss)(PFC)} \times R_{ss(PFC)})}{R_{cur(PFC)}}$$

$$\tau = R_{ss(PFC)} \times C_{ss(PFC)}$$

Soft stop is achieved by switching on the internal current source $I_{ch(ss)(PFC)}$.This current charges $C_{ss(PFC)}$ and the increasing capacitor voltage reduces the peak current. The charge current will flow as long as the voltage on pin SNSCURPFC is below the maximum PFC soft start voltage (typ. 0.5 V). If $V_{SNSCURPFC}$ exceeds the maximum PFC soft start voltage, the soft start current source will start limiting the charge current. To accurately determine if the capacitor is charged, the voltage is only measured during the off-time of the PFC power switch. The operation of the PFC is stopped when $V_{SNSCURPFC} > V_{stop(ss)(PFC)}$.

7.7.7 PFC overcurrent regulation, OCR-PFC (pin SNSCURPFC)

The maximum peak current is limited cycle-by-cycle by sensing the voltage across an external sense resistor ($R_{cur(PFC)}$) connected to the source of the external MOSFET. The voltage is measured via the SNSCURPFC pin and is limited to $V_{ocr(PFC)}$.

A voltage peak will appear on $V_{SNSCURPFC}$ when the PFC MOSFET is switched on due to the discharging of the drain capacitance. The leading edge blanking time, $t_{leb(PFC)}$, ensures that the overcurrent sensing block will not react to this transitory peak.

7.7.8 PFC mains undervoltage protection/brownout protection, UVP-mains (pin SNSMAINS)

The voltage on the SNSMAINS pin is sensed continuously to prevent the PFC trying to operate at very low mains input voltages. PFC switching stops as soon as $V_{SNSMAINS}$ drops below $V_{uvp(SNSMAINS)}$. Mains undervoltage protection is also called brownout protection.

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$V_{SNSMAINS}$ is clamped to a minimum value of $V_{pu(SNSMAINS)}$ for fast restart as soon as the mains input voltage recovers after a mains-dropout. The PFC (re)starts once $V_{SNSMAINS}$ exceeds the start level $V_{start(SNSMAINS)}$.

7.7.9 PFC boost overvoltage protection, OVP-boost (pin SNSBOOST)

An overvoltage protection circuit has been built in to prevent boost overvoltages during load steps and mains transients.

Switching of the power factor correction circuit is inhibited as soon as the voltage on the SNSBOOST pin rises above $V_{ovp(SNSBOOST)}$. PFC switching resumes as soon as $V_{SNSBOOST}$ drops below $V_{ovp(SNSBOOST)}$ again.

Overvoltage protection will also be triggered in the event of an open circuit at the resistor connected between SNSBOOST and ground.

7.7.10 PFC short circuit/open-loop protection, SCP/OLP-PFC (pin SNSBOOST)

The power factor correction circuit will not start switching until the voltage on the SNSBOOST pin rises above $V_{scp(SNSBOOST)}$. This acts as short circuit protection for the boost voltage (SCP-boost).

The SNSBOOST pin draws a small input current $I_{prot(SNSBOOST)}$. If this pin gets disconnected, the residual current will pull down $V_{SNSBOOST}$, triggering short circuit protection (SCP-boost). This combination creates an open-loop protection (OLP-PFC).

7.8 HBC controller

The HBC controller converts the 400 V boost voltage from the PFC into one or more regulated DC output voltages and drives two external MOSFETS in a half-bridge configuration connected to a transformer. The transformer, which has a leakage inductance and a magnetizing inductance, forms the resonant circuit in combination with the resonant capacitor and the load at the output. The regulation is realized via frequency control.

7.8.1 HBC high-side and low-side driver (pin GATEHS and GATELS)

Both drivers have identical driving capability. The output of each driver is connected to the equivalent gate of an external high-voltage power MOSFET.

The low-side driver is referenced to pin PGND and is supplied from SUPREG.

The high-side driver is floating. The reference for the high-side driver is pin HB, connected to the midpoint of the external half-bridge. The high-side driver is supplied from SUPHS which is connected to the external bootstrap capacitor C_{SUPHS}. The bootstrap capacitor is charged from SUPREG via external diode D_{SUPHS} when the low-side MOSFET is on.

7.8.2 HBC boost undervoltage protection, UVP-boost (pin SNSBOOST)

The voltage on the SNSBOOST pin is sensed continuously to prevent the HBC controller trying to operate at very low boost input voltages. Once $V_{SNSBOOST}$ drops below $V_{uvp(SNSBOOST)}$, HBC switching stops the next time GATELS goes HIGH. HBC switching resumes as soon as $V_{SNSBOOST}$ rises above $V_{start(SNSBOOST)}$.

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7.8.3 HBC switch control

HBC switch control determines when the MOSFETs switch on and off. It uses the output from several other blocks.

- A divider is used to realize alternate switching of the high- and low-side MOSFETs for each oscillator cycle. The oscillator frequency is twice the half-bridge frequency.
- The controlled oscillator determines the switch-off point.
- Adaptive non-overlap time sensing determines the switch-on point. This is the adaptive non-overlap time function.
- Several protection circuits and the state of the SSHBC/EN input determine whether the resonant converter is allowed to start switching.

Figure 9 provides an overview of typical switching behavior.

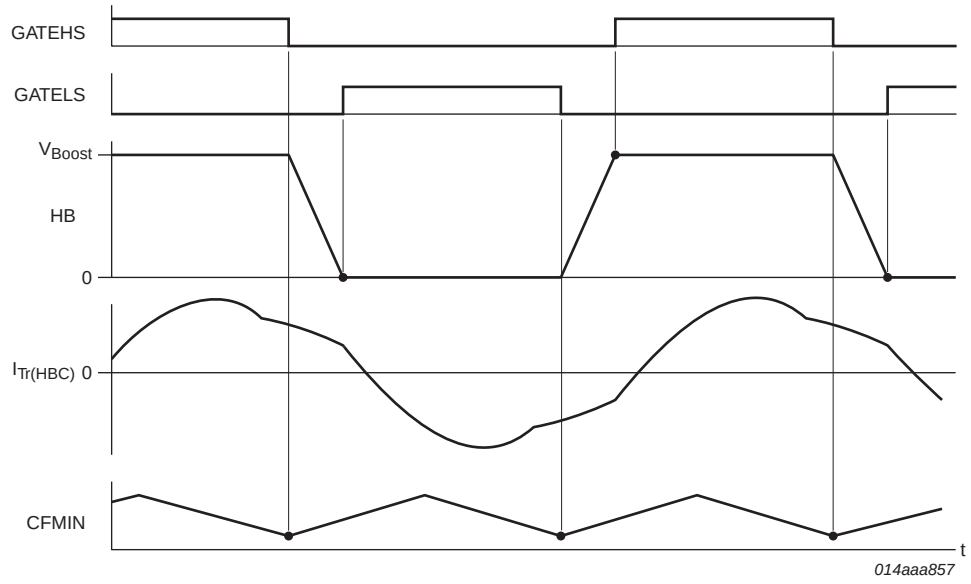

Fig 9. Switching behavior of the HBC

7.8.4 HBC Adaptive Non-Overlap (ANO) time function (pin HB)

7.8.4.1 Inductive mode (normal operation)

The high efficiency characteristic of a resonant converter is the result of Zero-Voltage Switching (ZVS) of the power MOSFETs, also called soft switching. To facilitate soft switching, a small non-overlap time is required between the on-times of the high- and low-side MOSFETs. During this non-overlap time, the primary resonant current (dis-)charges the capacitance of the half-bridge between ground and the boost voltage. After this (dis-)charge, the body diode of the MOSFET starts conducting and because the voltage across the MOSFET is zero, there are no switching losses when the MOSFET is switched on. This mode of operation is called inductive mode because the switching frequency is above the resonance frequency and the resonant tank has an inductive impedance.

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The time required for the HB transition depends on the amplitude of the resonant current at the instant of switching. There is a complex relationship between this amplitude, the frequency, the boost voltage and the output voltage. Ideally the IC should switch the MOSFET on as soon as the HB transition has been completed. If it waits any longer, the HP voltage may swing back, especially at high output loads. The advanced adaptive non-overlap time function takes care of this timing, so that it's not necessary to chose a fixed dead time (which is always a compromise). This saves on external components.

Adaptive non-overlap time sensing measures the HB slope after one MOSFET has been switched off. Normally, the HB slope starts immediately (the voltage starts rising or falling). Once the transition at the HB node is complete, the slope ends (the voltage stops rising/falling). This is detected by the ANO time sensor and the other MOSFET is switched on. In this way the non-overlap time is optimized automatically, minimizing switching losses, even if the HB transition cannot be fully completed. Figure 10 illustrates the operation of the adaptive non-overlap time function in Inductive mode.

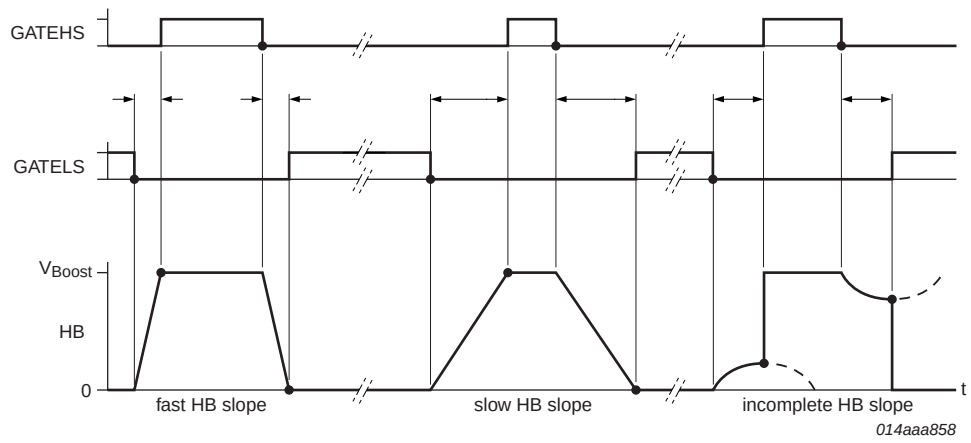

Fig 10. Adaptive non-overlap time function (normal inductive operation)

The non-overlap time depends on the HB slope, but has upper and lower limits.

An integrated minimum non-overlap time, $t_{no(min)}$, prevents cross conduction occurring under any circumstances.

The maximum non-overlap time is limited to the oscillator charge time. If the HB slope lasts longer than the oscillator charge time (= ¼ of HB switching period) the MOSFET is forced to switch on. In this case the MOSFET is not soft switching. This limitation ensures that, at very high switching frequencies, the MOSFET on-time is at least ¼ of the HB switching period.

7.8.4.2 Capacitive mode

The description above holds for normal operation with a switching frequency above the resonance frequency. When an error condition occurs (e.g. output short, load pulse too high) the switching frequency can be lower than the resonance frequency. The resonant tank then has a capacitive impedance. In Capacitive mode, the HB slope does not start after the MOSFET has switched off. Switching on the other MOSFET is not recommended in this situation. The absence of soft switching increases dissipation in the MOSFETs. In

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Capacitive mode, the body diode in the switched-off MOSFET may start conducting. Switching on the other MOSFET at this instant can result in the immediate destruction of the MOSFETs.

The advanced adaptive non-overlap time of the TEA1713LT will always wait until the slope at the half-bridge node starts. It guarantees safe switching of the MOSFETs in all circumstances. Figure 11 illustrates the operation of the adaptive non-overlap time function in Capacitive mode.

In Capacitive mode, half the resonance period may elapse before the resonant current changes back to the correct polarity and starts charging the half-bridge node. The oscillator is slowed down until the half-bridge slope starts to allow this relatively long waiting time. See Section 7.8.5 for more details on the oscillator.

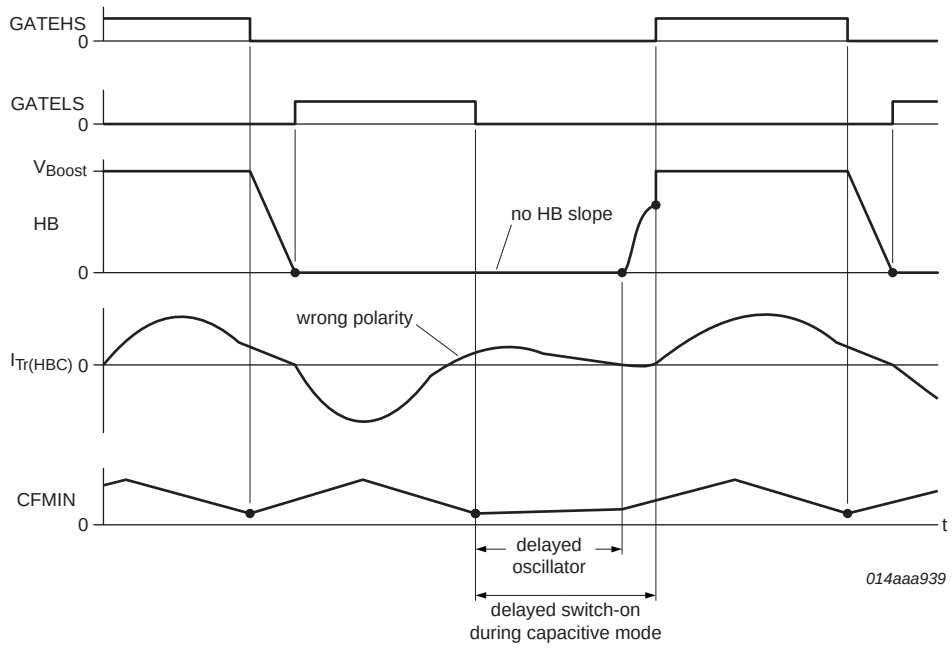

Fig 11. Adaptive non-overlap time function (capacitive operation)

The MOSFET will be forced to switch on if the half-bridge slope fails to start and the oscillator voltage reaches $V_{u(CFMIN)}$.

The switching frequency is increased to eliminate the problems associated with Capacitive mode operation. This is explained in Section 7.8.11.

7.8.5 HBC slope controlled oscillator (pins CFMIN and RFMAX)

The slope-controlled oscillator determines the switching frequency of the half-bridge. The oscillator generates a triangular waveform between $V_{u(CFMIN)}$ and $V_{l(CFMIN)}$ at the external capacitor C_{fmin}.

Figure 12 shows how the frequency is determined.

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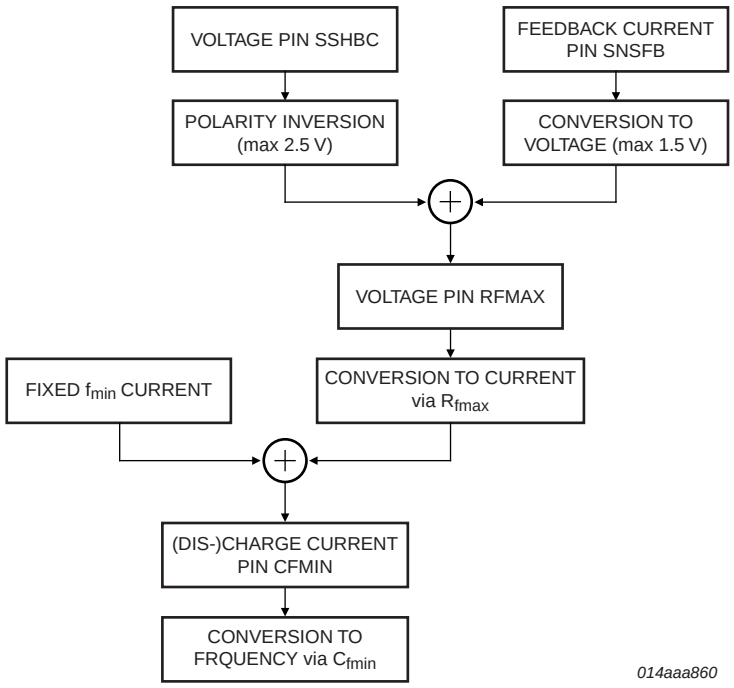

Fig 12. Determination of frequency

Two external components determine the frequency range:

- Capacitor C_{fmin} connected between pin CFMIN and ground sets the minimum frequency in combination with an internally trimmed current source $I_{osc(min)}$.
- Resistor R_{fmax} connected between pin RFMAX and ground sets the frequency range and thus the maximum frequency.

The oscillator frequency depends on the charge and discharge currents of C_{fmin}. The (dis-)charge current contains a fixed component, $I_{osc(min)}$, that determines the minimum frequency, and a variable component that is 4.9 times greater than the current in pin RFMAX. I_{RFMAX} is determined by the value of R_{fmax} and the voltage on pin RFMAX:

- The voltage on pin RFMAX is $V_{fmin(RFMAX)}$ (typ. 0 V) at the minimum frequency.
- The voltage on pin RFMAX is $V_{fmax(fb)(RFMAX)}$ (typ. 1.5 V) at the maximum feedback frequency.
- The voltage on pin RFMAX is $V_{fmax(ss)(RFMAX)}$ (typ. 2.5 V) at the maximum soft start frequency.

The maximum frequency of the oscillator is limited internally. The HB frequency is limited to $f_{limit(HB)}$ (min. 500 kHz). Figure 13 illustrates the relationship between V_{RFMAX}, R_{fmax}, C_{fmin} and f_{HB}.

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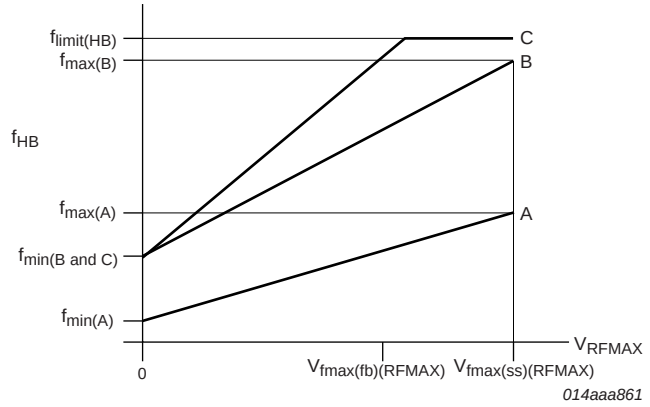

A: C_{fmin} = high, R_{fmax} = high

B: C_{fmin} = low, R_{fmax} = low

C: C_{fmin} = low, R_{fmax} = too low

Fig 13. Function of R_{fmax} and C_{fmin}

The oscillator is controlled by the slope of the half-bridge. The oscillator charge current is initially set to a low value $I_{osc(red)}$ (typ. 30 μA). When the start of the half-bridge slope is detected, the charge current is increased to its normal value. This feature is used in combination with the adaptive non-overlap time function as described in Section 7.8.4.2 and Figure 11. Since the half-bridge slope normally starts directly after the MOSFET is switched off, the length of time the oscillator current is low will be negligible under normal operating conditions.

7.8.6 HBC feedback input (pin SNSFB)

In a typical power supply application, the output voltage is compared and amplified on the secondary side. The output of the error amplifier is transferred to the primary side via an opto-coupler. This opto-coupler can be connected directly to the SNSFB pin.

The SNSFB pin supplies the opto-coupler from an internal voltage source $V_{pu(SNSFB)}$ (typ. 8.4 V) with a series resistance $R_{O(SNSFB)}$. The series resistance allows spike filtering via an external capacitor. To ensure sufficient bias current for the opto-coupler, the feedback input has a threshold current $I_{fmin(SNSFB)}$ (typ. 0.66 mA) at which the frequency is at a minimum. The maximum frequency is reached at $I_{fmax(SNSFB)}$ (typ 2.2 mA). The maximum frequency that can be reached via the SNSFB pin is lower (typ. 60 %) than the maximum frequency that can be reached via the SSHBC/EN pin. Figure 14 shows the relationship between I_{SNSFB}, V_{SNSFB} and V_{RFMAX}.

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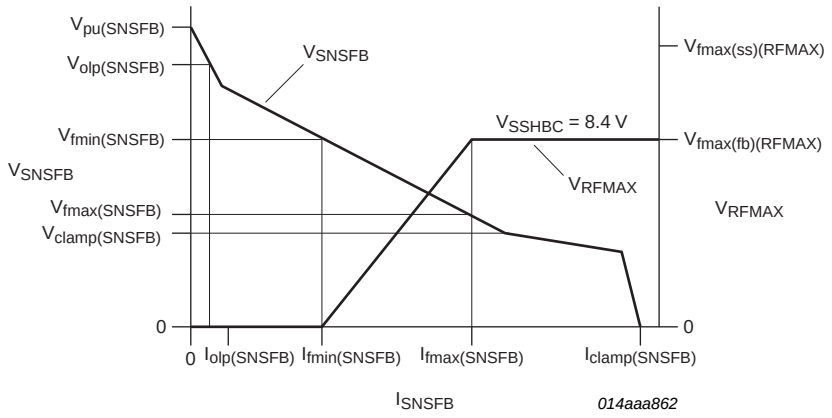

Fig 14. Transfer function of feedback input

Below the level for minimum frequency, V_{SNSFB} is clamped at $V_{clamp(SNSFB)}$ (typ. 3.2 V). This clamp enables a fast recovery of the output voltage regulation loop after an overshoot of the output voltage. The maximum current the clamp can deliver is $I_{clamp(SNSFB)}$ (typ. 7.3 mA).

7.8.7 HBC open-loop protection, OLP-HBC (pin SNSFB)

Under normal operating conditions, the opto-coupler current will be between $I_{fmin(SNSFB)}$ and $I_{fmax(SNSFB)}$ and will pull down the voltage at pin SNSFB. Due to an error in the feedback loop, the current could be less than $I_{fmin(SNSFB)}$ with the HBC controller delivering maximum output power.

The HBC controller features open-loop protection (OLP-HBC), which monitors the voltage on pin SNSFB. When V_{SNSFB} exceeds $V_{olp(SNSFB)}$, the protection timer is started. The Protection shutdown state is activated if the OLP condition is still present after the protection time has elapsed.

7.8.8 HBC soft start (pin SSHBC/EN)

The relationship between switching frequency and output current is not constant. It depends strongly on the output voltage and the boost voltage. This relationship can be complex. The TEA1713LT contains a soft start function to ensure that the resonant converter starts or restarts with safe currents. This soft start function forces a start at such a high frequency that currents will be acceptable under all conditions. Soft start then slowly decreases the frequency. Normally, output voltage regulation will have taken over frequency control before soft start has reached its minimum frequency. Limiting the output current during start-up also limits the rate at which the output voltage rises and prevents an overshoot.

Soft start utilizes the voltage on pin SSHBC/EN. The timing of the soft start is set by external capacitor $C_{ss(HBC)}$. Pin SSHBC/EN is also used as an enable input. Soft start voltage levels are above the enable voltage thresholds.

7.8.8.1 Soft start voltage levels

The relationship between the soft start voltage at pin SSHBC/EN and the voltage at pin RFMAX, which is directly related to the frequency, is illustrated in Figure 15.

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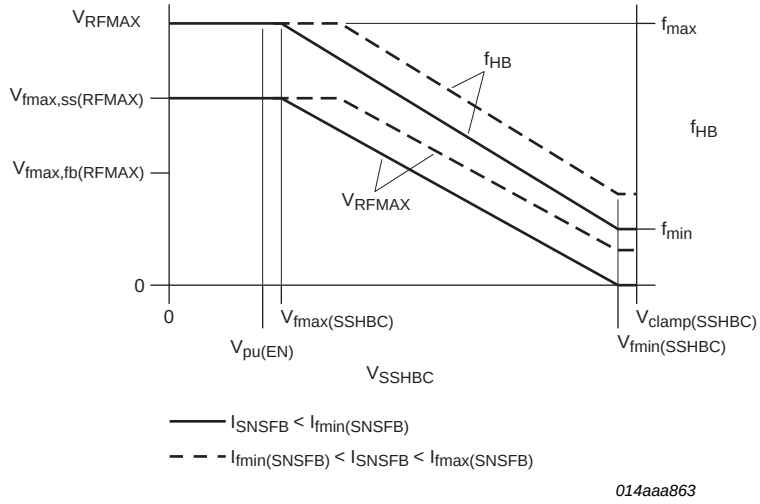

Fig 15. Relation between SSHBC/EN voltage and frequency

V_{RFMAX} and $V_{SSHBC/EN}$ are of opposite polarity. At initial start-up, $V_{SSHBC/EN}$ is below $V_{fmax(SSHBC)}$ (typ. 3.2 V), which corresponds to the maximum frequency. During start-up, $C_{ss(HBC)}$ is charged, $V_{SSHBC/EN}$ rises and the frequency decreases. The contribution of the soft start function is zero when $V_{SSHBC/EN}$ is above $V_{fmin(SSHBC)}$ (typ. 7.9 V).

$V_{SSHBC/EN}$ is clamped at a maximum of $V_{clamp(SSHBC)}$ (typ. 8.4 V) (frequency is at a minimum) and at a minimum (≈ 3 V). Below $V_{fmax(SSHBC)}$ (maximum frequency), the discharge current is reduced to a maximum-frequency soft start current of typically 5 μA The voltage is clamped at a minimum of $V_{pu(EN)}$ (typ. 3 V). Both clamp levels are just outside the operating area of $V_{fmax(SSHBC)}$ to $V_{fmin(SSHBC)}$. The margins avoid frequency disturbance during normal output voltage regulation, but ensure that overcurrent regulation can respond quickly.

7.8.8.2 Soft start charge and discharge

At initial start-up, the soft start capacitor $C_{ss(HBC)}$ is charged to obtain a decreasing frequency sweep from maximum to operating frequency. As well as being used to softly start up the resonant converter, the soft start functionality is also used for regulation purposes (such as overcurrent regulation). $C_{ss(HBC)}$ can therefore be charged or discharged. In the case of overcurrent regulation, a continuous alternation between charging and discharging takes place. In this way $V_{SSHBC/EN}$ can be regulated, thereby overruling the signal from the feedback input.

The (dis-)charge current can have a high value, $I_{ss(hf)(SSHBC)}$ (typ. 160 μA), resulting in a fast (dis-)charge, or it can have a low value $I_{ss(lf)(SSHBC)}$ (typ. 40 μA), resulting in a slow (dis-)charge. This two-speed soft start sweep allows for a combination of a short start-up time for the resonant converter and stable regulation loops (such as overcurrent regulation).

The fast (dis-)charge speed is used for the upper frequency range where $V_{SSHBC/EN}$ is below $V_{ss(hf-lf)(SSHBC)}$ (typ. 5.6 V). In the upper frequency range, the currents in the converter do not react strongly to frequency variations.

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The slow (dis-)charge speed is used for the lower frequency range where $V_{SSHBC/EN}$ is above $V_{ss(hf-lf)(SSHBC)}$ (typ. 5.6 V). In the lower frequency range, the currents in the converter react strongly to frequency variations.

Section 7.8.10.2 describes how the two-speed soft start function is used for overcurrent regulation.

The soft start capacitor is neither charged nor discharged during non-operation time in Burst mode. The soft start voltage will not change during this time.

7.8.8.3 Soft start reset

The TEA1713LT has a special fast soft start reset feature for the HBC controller that forces $V_{fmax(ss)(RFMAX)}$ on pin RFMAX. Soft start reset is used when the HBC controller is enabled via the SSHBC/EN pin or after a restart to ensure a safe start at maximum frequency. Soft start reset is not used when the operation was stopped in Burst mode.

When a soft start reset function is activated, the oscillator control input is disconnected from the soft start capacitor, $C_{ss(HBC)}$, connected between pin SSHBC/EN and ground and the switching frequency is immediately set to a maximum. Starting the switching at the maximum is a safe starting condition. At the same time, the capacitor is discharged to the maximum frequency level, $V_{fmax(SSHBC)}$. Once $V_{SSHBC/EN}$ has reached this level, the oscillator control input is connected to the pin again and the normal soft start sweep follows. Figure 16 shows the soft start reset and the two-speed frequency sweep downwards.

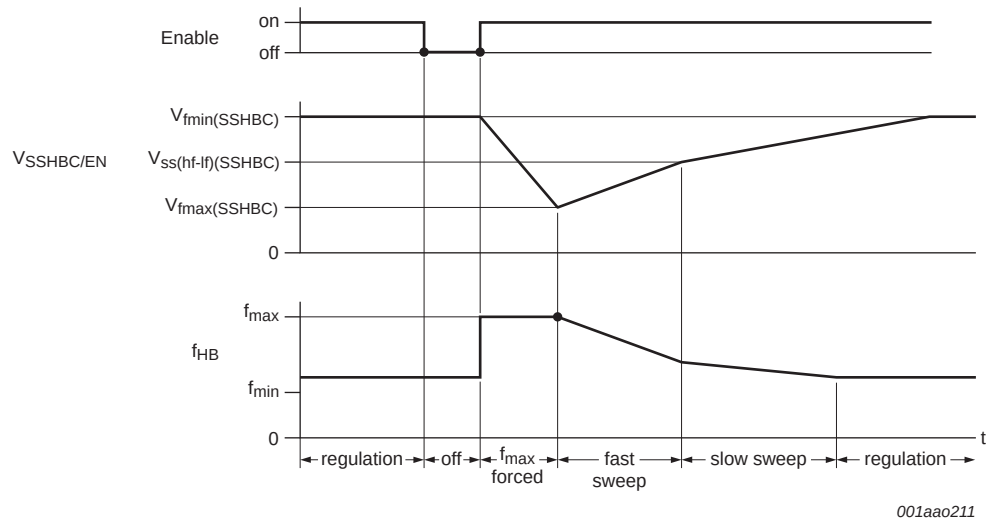

Fig 16. Soft start reset and two-speed soft start

7.8.9 HBC high-frequency protection, HFP-HBC (pin RFMAX)

Normally the converter will not operate continuously at maximum frequency because it will sweep down to much lower values. Certain error conditions, such as a disconnected transformer, could cause the converter to operate continuously at maximum frequency. If zero-voltage switching conditions are no longer present, the MOSFETs can overheat. The TEA1713LT features High-Frequency Protection (HFP) for the HBC controller to protect it from being damaged in such circumstances.

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HFP senses the voltage at pin RFMAX. This voltage indicates the current frequency. When the frequency is higher than 75 % of the soft start frequency range, the protection timer is started. The 75 % level corresponds to an RFMAX voltage of $V_{hfp(RFMAX)}$ (typ. 1.83 V).

7.8.10 HBC overcurrent regulation, OCR (pin SNSCURHBC)

Overcurrent regulation (OCR-HBC), which increases the frequency slowly, protects the HBC controller against overcurrent. The protection timer is also started.

A boost voltage compensation function is included to reduce the variation in the output current protection level.

7.8.10.1 Boost voltage compensation

The primary current, also known as the resonant current, is sensed via pin SNSCURHBC. It senses the momentary voltage across an external current sense resistor $R_{cur(HBC)}$. The use of the momentary current signal allows for fast overcurrent protection and simplifies the stabilizing of overcurrent regulation. The OCR comparators compare $V_{SNSCURHBC}$ with the maximum positive and negative values.

For the same output power, the primary current is higher when the boost voltage is low. A boost compensation is included to reduce the dependency of the protected output current level on the boost voltage. The boost compensation sources and sinks a current from the SNSCURHBC pin. This current creates a voltage drop across the series resistor R_{curcmp}.

The amplitude of the current depends linearly on the boost voltage. At nominal boost voltage the current is zero and the voltage $V_{Cur(HBC)}$ across the current sense resistor is also present at the SNSCURHBC pin. At the UVP-boost start level $V_{uvp(SNSBOOST)}$, the current is at a maximum. The direction of the current, sink or source, depends on the active gate signal. The voltage drop created across R_{curcmp} reduces the amplitude at the pin, resulting in a higher effective current protection level. The amount of compensation is set by the value of R_{curcmp}. Figure 17 shows how the boost compensation works for an artificial current signal. The sinking compensation current only flows when $V_{SNSCURHBC}$ is positive because of the circuit implementation.

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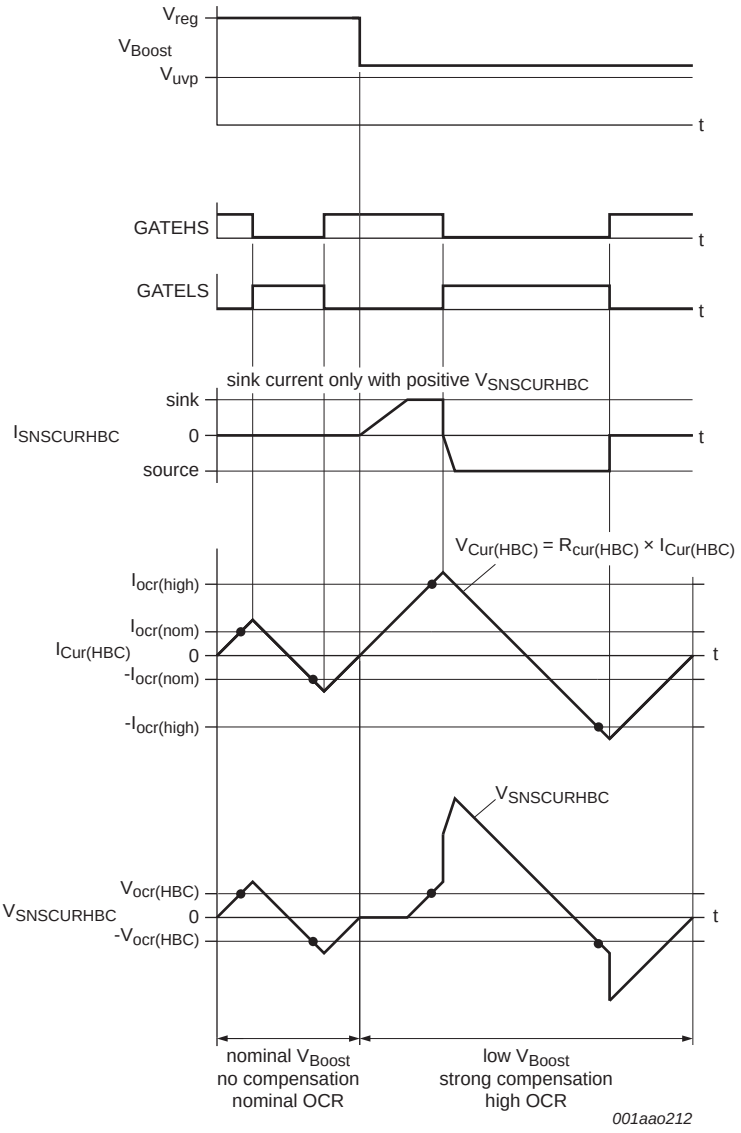

Fig 17. Boost voltage compensation

7.8.10.2 Overcurrent regulation, OCR-HBC

The lowest comparator levels at the SNSCURHBC pin, $V_{ocr(HBC)}$ (typ. −0.5 V and +0.5 V), relate to the overcurrent regulation voltage. There are comparators for both the positive and negative polarities. The positive comparator is active during the high-side on-time and the following high-side to low-side non-overlap time. The negative comparator is active during the remaining time. If either level is exceeded, the frequency will be slowly increased. This is accomplished by discharging the soft start capacitor. Each time the OCR level is exceeded, the event is latched until the next stroke and the soft start discharge current is enabled. When both the positive and negative OCR levels are exceeded, the soft start discharge current will flow continuously.

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Overcurrent regulation is very effective at limiting the output current during start-up. A smaller soft start capacitor can be used to achieve a faster start-up. Using a smaller capacitor may result in an output current that is too high at times, but the OCR function will slow down the frequency sweep when needed to keep the output current within the specified limits. Figure 18 shows the operation of the OCR during output voltage start-up.

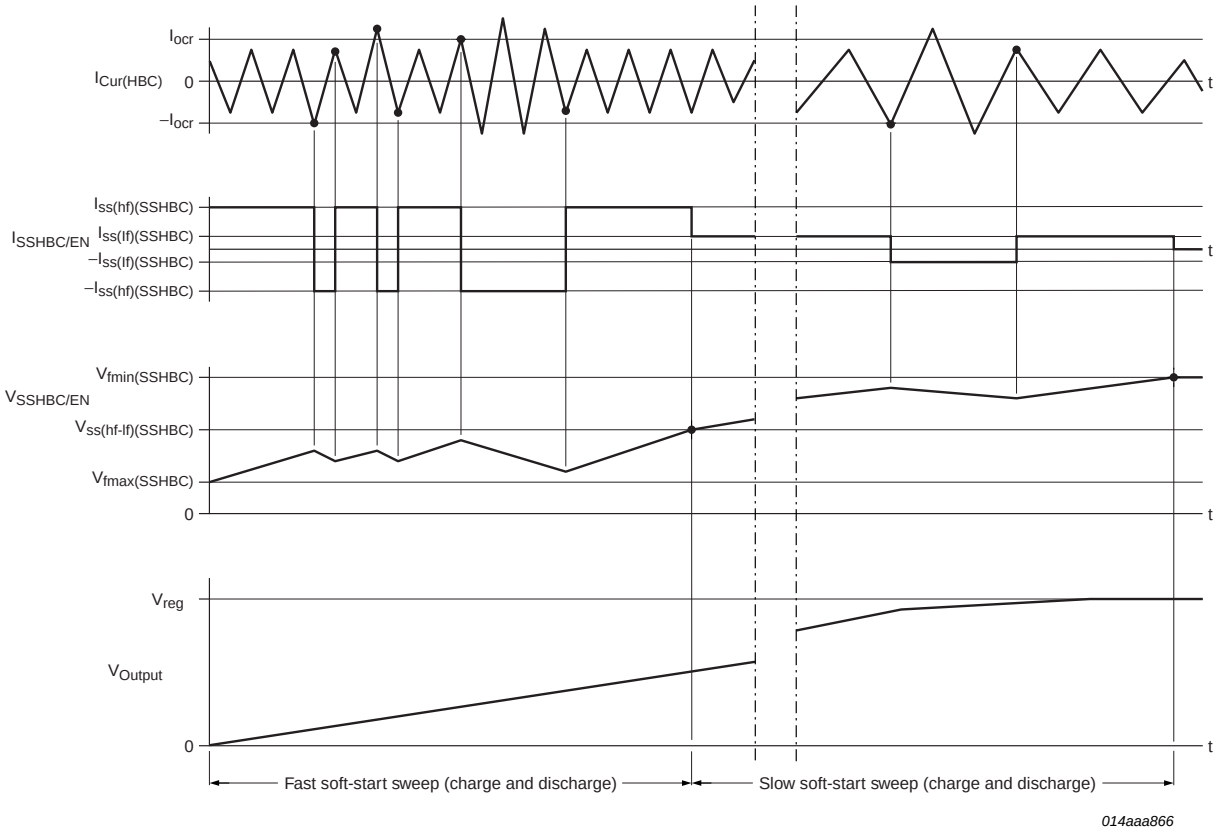

Fig 18. Overcurrent regulation during start-up

The protection timer is also started. The Protection shutdown state is activated when the OCR-HBC condition is still present after the protection time has elapsed.

7.8.11 HBC capacitive mode regulation, CMR (pin HB)

The MOSFETs in the half-bridge drive the resonant circuit. Depending on the output load, the output voltage, and the switching frequency this resonant circuit can have an inductive impedance or a capacitive impedance. Inductive impedance is preferred because it facilitates efficient zero-voltage switching.

Harmful switching in Capacitive mode is prevented by the adaptive non-overlap time function (see Section 7.8.4.2). An extra action is performed which results in Capacitive Mode Regulation (CMR). CMR causes the half-bridge circuit to return to Inductive mode from Capacitive mode.

Capacitive mode is detected when the HB slope does not start within $t_{to(cmr)}$ after the MOSFETs have switched off. Detection of Capacitive mode will increase the switching frequency. This is realized by discharging the soft start capacitor with a relatively high

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current $I_{cmr(hf)(SSHBC)}$ from the instant $t_{to(cmr)}$ has expired until the half-bridge slope has started. The frequency increase regulates the HBC to the border between capacitive and inductive mode.

7.9 Protection overview

Table 4. Overview protections

Protected Part	Symbol	Protection	Affected	Action	Description
IC	UVP-SUPIC	Undervoltage protection SUPIC	IC	disable	Section 7.2.1
IC	UVP-SUPREG	Undervoltage protection SUPREG	IC	disable	Section 7.2.2
IC	UVP-supplies	Undervoltage protection supplies	IC	disable and reset	Section 7.3
IC	SCP-SUPIC	Short circuit protection SUPIC	IC	low HV start-up current	Section 7.2.4
IC	OVP-output	Overvoltage protection output	IC	shutdown	Section 7.5.4
IC	OTP	Overtemperature protection	IC	disable	Section 7.5.5
PFC	OCR-PFC	Overcurrent regulation PFC	PFC	switch off cycle-by-cycle	Section 7.7.7
PFC	UVP-mains	Undervoltage protection mains	PFC	suspend switching	Section 7.7.8
PFC	OVP-boost	Overvoltage protection boost	PFC	suspend switching	Section 7.7.9
PFC	SCP-boost	Short circuit protection boost	IC	restart	Section 7.7.10
PFC	OLP-PFC	Open-loop protection PFC	IC	restart	Section 7.7.10
HBC	UVP-boost	Undervoltage protection boost	HBC	disable	Section 7.8.2
HBC	OLP-HBC	Open-loop protection HBC	IC	shutdown after protection time	Section 7.8.7
HBC	HFP-HBC	High-frequency protection HBC	IC	shutdown after protection time	Section 7.8.9
HBC	OCR-HBC	Overcurrent regulation HBC	HBC IC	increase frequency; shutdown after protection time	Section 7.8.10.2
HBC	CMR	Capacitive mode regulation	HBC	increase frequency	Section 7.8.11
HBC	ANO	Adaptive non-overlap	HBC	prevent hazardous switching	Section 7.8.4

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).; All voltages are measured with respect to pin SGND; Currents are positive when flowing into the IC; The voltage ratings are valid provided other ratings are not violated; Current ratings are valid provided the maximum power rating is not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{SUPHV}	voltage on pin SUPHV	continuous	−0.4	+630	V
V_{SUPHS}	voltage on pin SUPHS	DC	−0.4	+570	V
		t < 0.5 s	−0.4	+630	V
		referenced to pin HB	−0.4	+14	V
V_{SUPIC}	voltage on pin SUPIC		−0.4	+38	V
$V_{SNSAUXPFC}$	voltage on pin SNSAUXPFC		−25	+25	V
V_{SUPREG}	voltage on pin SUPREG		−0.4	+12	V
V_{SNSOUT}	voltage on pin SNSOUT		−0.4	+12	V
V_{RCPROT}	voltage on pin RCPROT		−0.4	+12	V
V_{SNSFB}	voltage on pin SNSFB		−0.4	+12	V
$V_{SSHBC/EN}$	voltage on pin SSHBC/EN		−0.4	+12	V
V_{GATEHS}	voltage on pin GATEHS	t < 10 µs for I > 10 mA	−0.4	V_{SUPHS} + 0.4	V
V_{GATELS}	voltage on pin GATELS	t < 10 µs for I > 10 mA	−0.4	V_{SUPREG} + 0.4	V
$V_{GATEPFC}$	voltage on pin GATEPFC	t < 10 µs for I > 10 mA	−0.4	V_{SUPREG} + 0.4	V
$V_{SNSCURHBC}$	voltage on pin SNSCURHBC		−5	+5	V
$V_{SNSBOOST}$	voltage on pin SNSBOOST		−0.4	+5	V
$V_{SNSMAINS}$	voltage on pin SNSMAINS		−0.4	+5	V
$V_{SNSCURPFC}$	voltage on pin SNSCURPFC	current limited	−0.4	+5	V
$V_{COMPPFC}$	voltage on pin COMPPFC		−0.4	+5	V
V_{CFMIN}	voltage on pin CFMIN		−0.4	+5	V
V_{PGND}	voltage on pin PGND		−1	+1	V
Currents					
$I_{GATEPFC}$	current into pin GATEPFC	duty cycle < 10 %	−0.8	+2	A
$I_{SNSCURPFC}$	current into pin SNSCURPFC		−1	+10	mA
General					
P_{tot}	total power dissipation	T_{amb} < 75 °C	-	0.8	W
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−40	+150	°C

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Table 5. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).; All voltages are measured with respect to pin SGND; Currents are positive when flowing into the IC; The voltage ratings are valid provided other ratings are not violated; Current ratings are valid provided the maximum power rating is not violated.

Symbol	Parameter	Conditions		Min	Max	Unit
ESD						
V_{ESD}	Electrostatic discharge voltage	Human body model				
		Pin 12 (SUPHV)	[1]	-	1500	V
		Pin 13,14,15 (HS driver)	[1]	-	1000	V
		other pins	[1]	-	2000	V
		Machine model				
		All pins	[2]	-	200	V
		Charged device model				
		All pins		-	500	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	In free air; JEDEC single layer test board	90	K/W

10. Characteristics

Table 7. Characteristics

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High-voltage start-up source (pin SUPHV)						
$I_{dism(SUPHV)}$	disable mode current on pin SUPHV	Disabled IC state	-	150	-	μA
$I_{red(SUPHV)}$	reduced current on pin SUPHV	$V_{SUPIC} < V_{scp(SUPIC)}$	-	1.1	-	mA
$I_{nom(SUPHV)}$	nominal current on pin SUPHV	$V_{SUPIC} < V_{start(hvd)(SUPIC)}$	-	5.1	-	mA
$I_{tko(SUPHV)}$	takeover current on pin SUPHV	$V_{SUPIC} > V_{start(hvd)(SUPIC)}$	-	7	-	μA
$V_{det(SUPHV)}$	detection voltage on pin SUPHV		-	-	25	V
$V_{rst(SUPHV)}$	reset voltage on pin SUPHV	$V_{SUPIC} < V_{rst(SUPIC)}$	-	7	-	V
Low-voltage IC supply (pin SUPIC)						
$V_{start(hvd)(SUPIC)}$	start voltage with high voltage detected	$V_{SUPHV} > V_{det(SUPHV)}$	21.0	22.0	23.0	V
$V_{start(nohvd)(SUPIC)}$	start voltage with no high voltage detected	$V_{SUPHV} < V_{det(SUPHV)}$ or open	16.1	17.0	17.9	V
$V_{start(hys)(SUPIC)}$	hysteresis of start voltage on pin SUPIC		-	0.3	-	V

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Table 7. Characteristics *...continued*

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{uvp(SUPIC)}$	undervoltage protection voltage on pin SUPIC			14.2	15.0	15.8	V
$V_{rst(SUPIC)}$	reset voltage on pin SUPIC	$V_{SUPHV} < V_{rst(SUPHV)}$		-	7	-	V
$V_{scp(SUPIC)}$	short-circuit protection voltage on pin SUPIC			0.55	0.65	0.75	V
$I_{ch(red)(SUPIC)}$	reduced charge current on pin SUPIC	$V_{SUPIC} < V_{scp(SUPIC)}$		-	−0.95	-	mA
$I_{ch(nom)(SUPIC)}$	nominal charge current on pin SUPIC			-	−4.8	-	mA
$I_{dism(SUPIC)}$	current on pin SUPIC in disabled mode	Disabled IC state		-	0.25	-	mA
$I_{protm(SUPIC)}$	current on pin SUPIC in protection mode	SUPIC charge, SUPREG charge; Restart or shutdown state		-	0.4	-	mA
$I_{oper(SUPIC)}$	current on pin SUPIC in operating mode	Operational supply state; Driver pins open.		-	3	-	mA
Regulated supply (pin SUPREG)							
$V_{reg(SUPREG)}$	regulation voltage on pin SUPREG	I_{SUPREG} = −40 mA	[1]	10.6	10.9	11.2	V
$V_{start(SUPREG)}$	start voltage on pin SUPREG		[1]	-	10.7	-	V
$V_{uvp(SUPREG)}$	undervoltage protection voltage on pin SUPREG		[1]	-	10.3	-	V
$I_{ch(SUPREG)max}$	maximum charge current on pin SUPREG	$V_{SUPREG} > V_{uvp(SUPREG)}$		−40	−100	-	mA
$I_{ch(red)(SUPREG)}$	reduced charge current on pin SUPREG	$V_{SUPREG} < V_{uvp(SUPREG)}$; T = 25 °C.		-	−5.5	-	mA
		T = 140 °C		−2.5	-	-	mA
Enable input (pin SSHBC/EN)							
$V_{en(PFC)(EN)}$	PFC enable voltage on pin EN	PFC only	[2]	0.8	1.2	1.4	V
$V_{en(IC)(EN)}$	IC enable voltage on pin EN	PFC + HBC	[2]	1.8	2.2	2.4	V
$I_{pu(EN)}$	pull-up current on pin EN	$V_{SSHBC/EN}$ = 2.5 V		-	−42	-	µA
$V_{pu(EN)}$	pull-up voltage on pin EN			-	3.0	-	V
Fast shutdown reset (pin SNSMAINS)							
$V_{rst(SNSMAINS)}$	reset level on pin SNSMAINS		[2]	-	0.8	-	V
Protection and restart timer (pin RCPROT)							
$V_{u(RCPROT)}$	upper voltage on pin RCPROT			3.8	4.0	4.2	V
$V_{l(RCPROT)}$	lower voltage on pin RCPROT			0.4	0.5	0.6	V
$I_{ch(fast)(RCPROT)}$	fast-charge current on pin RCPROT			-	−2.2	-	mA
$I_{ch(slow)(RCPROT)}$	slow-charge current on pin RCPROT			−120	−100	−80	µA

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Table 7. Characteristics *...continued*

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output voltage protection sensing, UVP/OVP output (pin SNSOUT)							
$V_{ovp(SNSOUT)}$	overvoltage protection voltage on pin SNSOUT		[2]	3.40	3.50	3.60	V
Overtemperature protection							
T_{otp}	overtemperature protection trip temperature		[2]	130	150	160	°C
Burst mode activation (pin SNSOUT)							
$V_{burst(HBC)}$	HFC burst mode voltage		[2]	0.9	1.1	1.2	V
$V_{burst(PFC)}$	PFC burst mode voltage		[2]	0.3	0.4	0.5	V
$I_{pu(SNSOUT)}$	pull-up current on pin SNSOUT			-	−100	−80	µA
$V_{pu(SNSOUT)}$	pull-up voltage on pin SNSOUT	R_{SNSOUT} = 25 kΩ to SGND		-	1.5	-	V
PFC driver (pin GATEPFC)							
$I_{source(GATEPFC)}$	source current on pin GATEPFC	$V_{GATEPFC}$ = 2 V		-	−0.5		A
$I_{sink(GATEPFC)}$	sink current on pin GATEPFC	$V_{GATEPFC}$ = 2 V		-	0.7	-	A
		$V_{GATEPFC}$ = 10 V		-	1.2	-	A
PFC on-timer (pin COMPPFC)							
$V_{ton(COMPPFC)zero}$	zero on-time voltage on pin COMPPFC			-	3.5	-	V
$V_{ton(COMPPFC)max}$	maximum on-time voltage on pin COMPPFC			-	1.25	-	V
$f_{max(PFC)}$	PFC maximum frequency			100	125	150	kHz
$t_{off(PFC)min}$	minimum PFC off-time			-	1.4	-	µs
PFC error amplifier (pin SNSBOOST and COMPPFC)							
$V_{reg(SNSBOOST)}$	regulation voltage on pin SNSBOOST pin	$I_{COMPPFC}$ = 0		2.475	2.500	2.525	V
g_m	transconductance	$V_{SNSBOOST}$ to $I_{COMPPFC}$		-	80	-	µA/V
$I_{sink(COMPPFC)}$	sink current on pin COMPPFC	$V_{SNSBOOST}$ = 3.3 V		-	39	-	µA
$I_{source(COMPPFC)}$	compensation source current	$V_{SNSBOOST}$ = 2.0 V		-	−39	-	µA
$V_{clamp(COMPPFC)}$	clamp voltage on pin COMPPFC		[3]	-	3.9	-	V
PFC mains compensation (pin SNSMAINS)							
$t_{on(max)}$	maximum on-time	high mains; $V_{SNSMAINS}$ = 3.3 V		3.5	4.7	5.9	µs
		low mains; $V_{SNSMAINS}$ = 0.97 V		29	44	59	µs
$V_{mvc(SNSMAINS)max}$	maximum mains voltage compensation voltage on pin SNSMAINS			4.0	-	-	V

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Table 7. Characteristics *...continued*

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PFC demagnetization sensing (pin SNSAUXPFC)							
$V_{demag(SNSAUXPFC)}$	demagnetization voltage on pin SNSAUXPFC			−150	−100	−50	mV
$t_{to(mag)}$	magnetization time-out time			40	50	60	µs
$I_{prot(SNSAUXPFC)}$	protection current on pin SNSAUXPFC	$V_{SNSAUXPFC}$ = 50 mV		−75	−33	-	nA
PFC valley sensing (pin SNSAUXPFC)							
$(dV/dt)_{vrec(min)}$	minimum valley recognition rate of voltage change			-	-	1.7	V/µs
$t_{slope(vrec)min}$	minimum valley recognition slope time	$V_{SNSAUXPFC}$ = 1 V_{pp}	[4]	-	-	300	ns
		demagnetization to $\Delta V/\Delta t$ = 0	[5]	-	-	50	ns
$t_{d(val-dem)max}$	maximum valley-to-demag delay time			-	200	-	ns
$t_{to(vrec)}$	valley recognition time-out time			3	4	6	µs
PFC soft start (pin SNSCURPFC)							
$I_{ch(ss)(PFC)}$	PFC soft-start charge current			-	−60	-	µA
$V_{clamp(ss)(PFC)}$	PFC soft-start clamp voltage		[1]	0.46	0.50	0.54	V
$V_{stop(ss)(PFC)}$	PFC soft-start stop voltage		[1]	-	0.45	-	V
$R_{ss(PFC)}$	PFC soft-start resistor			12	-	-	kΩ
PFC overcurrent sensing (pin SNSCURPFC)							
$V_{ocr(PFC)}$	PFC overcurrent regulation voltage	dV/dt = 50 mV/µs		0.49	0.52	0.55	V
		dV/dt = 200 mV/µs		0.51	0.54	0.57	V
$t_{leb(PFC)}$	leading edge blanking time			250	310	370	ns
$I_{prot(SNSCURPFC)}$	protection current on pin SNSCURPFC			−50	−33	-	nA
PFC mains voltage sensing and clamp (pin SNSMAINS)							
$V_{start(SNSMAINS)}$	start voltage on pin SNSMAINS		[1]	1.11	1.15	1.19	V
$V_{uvp(SNSMAINS)}$	undervoltage protection voltage on pin SNSMAINS		[1]	0.84	0.89	0.94	V
$V_{pu(SNSMAINS)}$	pull-up voltage on pin SNSMAINS	UVP-mains active	[1]	-	1.05	-	V
$I_{pu(SNSMAINS)}$	maximum clamp current	UVP-mains active		-	−42	−35	µA
$I_{prot(SNSMAINS)}$	Protection current on pin SNSMAINS	$V_{SNSMAINS}$ > $V_{uvp(SNSMAINS)}$		-	33	100	nA
PFC boost voltage protection sensing, SCP/UVP/OVP boost (pin SNSBOOST)							
$V_{scp(SNSBOOST)}$	short-circuit protection voltage on pin SNSBOOST			0.35	0.40	0.45	V
$V_{start(SNSBOOST)}$	start voltage on pin SNSBOOST			-	2.30	2.40	V
$V_{uvp(SNSBOOST)}$	undervoltage protection voltage on pin SNSBOOST			1.50	1.60	-	V
$V_{ovp(SNSBOOST)}$	overvoltage protection voltage on pin SNSBOOST			2.59	2.63	2.67	V

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Table 7. Characteristics *...continued*

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{prot(SNSBOOST)}$	protection current on pin SNSBOOST	$V_{SNSBOOST}$ = 2.5 V		-	45	100	nA
HBC high-side and low-side driver (pin GATEHS and GATELS)							
$I_{source(GATEHS)}$	source current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 4 V		-	−310	-	mA
$I_{source(GATELS)}$	source current on pin GATELS	$V_{GATELS} - V_{PGND}$ = 4 V		-	−310	-	mA
$I_{sink(GATEHS)}$	sink current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 2 V;		-	560	-	mA
		$V_{GATEHS} - V_{HB}$ = 11 V		-	1.9	-	A
$I_{sink(GATELS)}$	sink current on pin GATELS	$V_{GATELS} - V_{PGND}$ = 2 V		-	560	-	mA
		$V_{GATELS} - V_{PGND}$ = 11 V		-	1.9	-	A
$V_{rst(SUPHS)}$	reset voltage on pin SUPHS			-	4.5	-	V
$I_{q(SUPHS)}$	quiescent current on pin SUPHS	$V_{SUPHS} - V_{HB}$ = 11 V		-	37	-	µA
HBC adaptive non-overlap time (pin HB)							
$(dV/dt)_{ano(min)}$	minimum adaptive non-overlap time rate of voltage change			-	-	120	V/µs
$t_{no(min)}$	minimum non-overlap time			-	-	160	ns
HBC current controlled oscillator (pin CFMIN and RFMAX)							
$f_{min(HB)}$	minimum frequency on pin HB	C_{fmin} = 390 pF; $V_{SSHBC/EN} > V_{fmin(SSHBC)}$ $V_{SNSFB} > V_{fmin(SNSFB)}$		40	44	48	kHz
$I_{osc(min)}$	minimum oscillator current	V_{RFMAX} = 0 V; charge and discharge		-	150	-	µA
$I_{osc(max)}$	maximum oscillator current	R_{fmax} = 15 kΩ; V_{RFMAX}=2.5 V; $V_{SSHBC/EN} < V_{fmax(SSHBC)}$		-	970	-	µA
$I_{osc(red)}$	reduced oscillator current	Slowed-down oscillator		-	−30	-	µA
I_{CFMIN}/I_{RFMAX}	current on pin CFMIN to current on pin RFMAX ratio			-	4.9	-	
$f_{limit(HB)}$	limit frequency on pin HB	C_{fmin} = 20 pF		500	670	-	kHz
$V_{u(CFMIN)}$	upper voltage on pin CFMIN			-	3.0	-	V
$V_{l(CFMIN)}$	lower voltage on pin CFMIN			-	1.0	-	V
$V_{fmin(RFMAX)}$	minimum frequency voltage on pin RFMAX			-	0	-	V
$V_{fmax(ss)(RFMAX)}$	maximum soft start frequency voltage on pin RFMAX	$V_{SSHBC/EN} < V_{fmax(SSHBC)}$		2.40	2.50	2.60	V
$V_{fmax(fb)(RFMAX)}$	maximum feedback frequency voltage on pin RFMAX	$V_{SNSFB} < V_{fmax(SNSFB)}$		1.45	1.55	1.65	V
HBC feedback input (pin SNSFB)							
$V_{pu(SNSFB)}$	pull-up voltage on pin SNSFB			-	8.4	-	V
$R_{O(SNSFB)}$	output resistance on pin SNSFB			-	1.5	-	kΩ
$V_{olp(SNSFB)}$	open-loop protection voltage on pin SNSFB		[2]	7.0	7.7	7.9	V
$I_{olp(SNSFB)}$	open-loop protection current on pin SNSFB		[2]	−0.35	−0.26	−0.10	mA

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Table 7. Characteristics *...continued*

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{fmin(SNSFB)}$	minimum frequency voltage on pin SNSFB			6.1	6.4	6.9	V
$I_{fmin(SNSFB)}$	minimum frequency current on pin SNSFB	$V_{SSHBC/EN} > V_{fmin(SSHBC)}$		−0.86	−0.66	−0.46	mA
$V_{fmax(SNSFB)}$	maximum frequency voltage on pin SNSFB	$V_{SSHBC/EN} > V_{fmin(SSHBC)}$		3.9	4.1	4.3	V
$I_{fmax(SNSFB)}$	maximum frequency current on pin SNSFB	$V_{SSHBC/EN} > V_{fmin(SSHBC)}$		-	−2.2	-	mA
$V_{clamp(SNSFB)}$	clamp voltage on pin SNSFB	maximum frequency; I_{SNSFB} = −4 mA		-	3.2	-	V
$I_{clamp(SNSFB)}$	clamp current on pin SNSFB	maximum frequency; V_{SNSFB} = 0 V		-	−7.3	-	mA
HBC soft-start (pin SSHBC/EN)							
$V_{fmax(SSHBC)}$	maximum frequency voltage on pin SSHBC			-	3.2	-	V
$V_{fmin(SSHBC)}$	minimum frequency voltage on pin SSHBC	$V_{SNSFB} > V_{fmin(SNSFB)}$		7.5	7.9	8.3	V
$V_{clamp(SSHBC)}$	clamp voltage on pin SSHBC			-	8.4	-	V
$V_{ss(hf-lf)(SSHBC)}$	high-low frequency soft-start voltage on pin SSHBC		[2]	-	5.6	-	V
$I_{ss(hf)(SSHBC)}$	high frequency soft-start current on pin SSHBC	$V_{SSHBC} < V_{ss(lf-hf)(SSHBC)}$					
		charge current		-	−160	-	µA
		discharge current		-	160	-	µA
$I_{ss(lf)(SSHBC)}$	low frequency soft-start current on pin SSHBC	$V_{SSHBC} > V_{ss(lf-hf)(SSHBC)}$					
		charge current		-	−40	-	µA
		discharge current		-	40	-	µA
$I_{cmr(hf)(SSHBC)}$	high frequency CMR current on pin SSHBC	$V_{SSHBC} < V_{ss(lf-hf)(SSHBC)}$ discharge only		-	1800	-	µA
$I_{cmr(lf)(SSHBC)}$	low frequency CMR current on pin SSHBC	$V_{SSHBC} > V_{ss(lf-hf)(SSHBC)}$ discharge only		-	440	-	µA
HBC high frequency sensing, HFP - HBC (pin RFMAX)							
$V_{hfp(RFMAX)}$	High-frequency protection voltage on pin RFMAX		[2]	1.70	1.83	2.00	V
HBC overcurrent sensing, OCR - HBC (pin SNSCURHBC)							
$V_{ocr(HBC)}$	HBC overcurrent regulation voltage						
		positive level; HS on + HS-LS non-overlap time		0.45	0.50	0.55	V
		negative level; LS on + LS-HS non-overlap time		−0.55	−0.50	−0.45	V

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Table 7. Characteristics *...continued*

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{bstc(SNSCURHBC)max}$	maximum boost compensation current on pin SNSCURHBC	$V_{SNSBOOST}$ = 1.8 V				
		source current; $V_{SNSCURHBC}$ = –0.5 V	-	–170	-	µA
		sink current; $V_{SNSCURHBC}$ = 0.5 V	-	170	-	µA
HBC Capacitive Mode Protection (CMP) (pin HB)						
$t_{to(cmr)}$	time-out capacitive mode regulation		-	690	-	ns

[1] The marked levels on this pin are correlated. The voltage difference between the levels has much less spread than the absolute value of the levels themselves.

[2] Switching level has some hysteresis. The hysteresis falls within the limits.

[3] For a typical application with a compensation network on pin COMPPFC, like the example in Figure 19.

[4] Minimum required voltage change time for valley recognition on pin SNSAUXPFC.

[5] Minimum time required between demagnetization detection and ΔV/Δt = 0 on pin SNSAUXPFC.

11. Application information

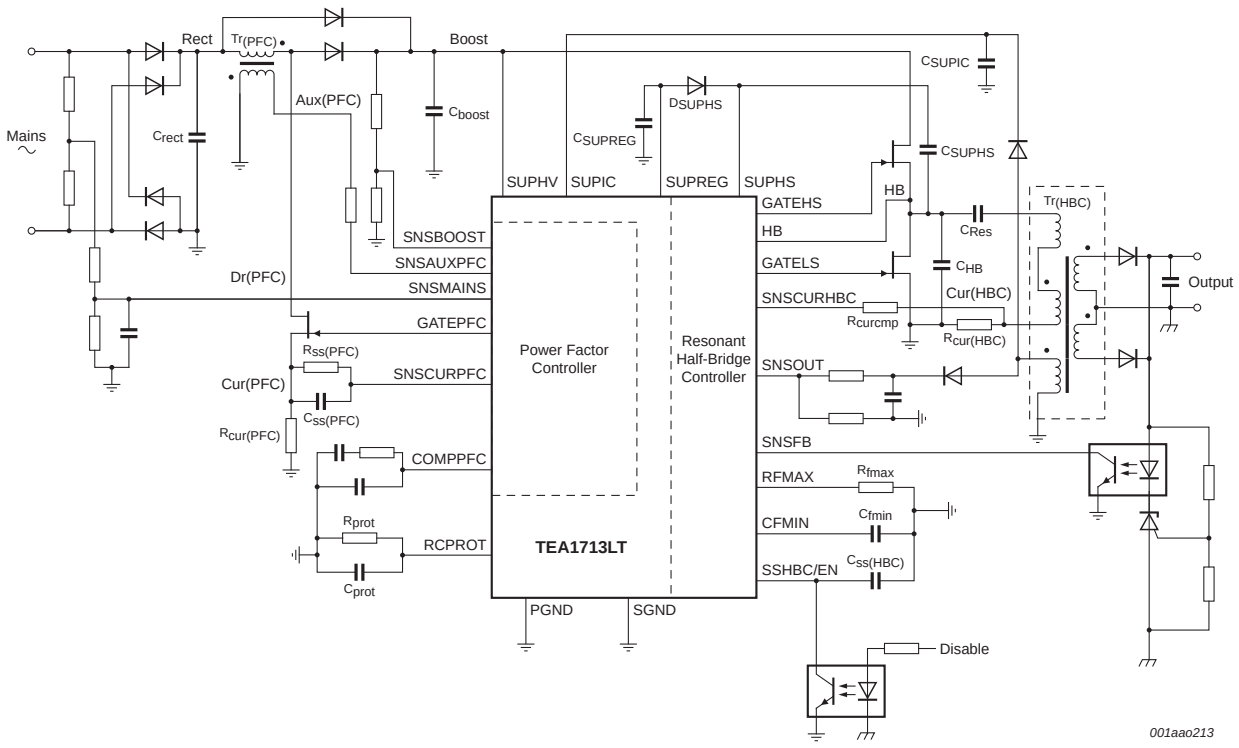

Fig 19. Application diagram of TEA1713LT

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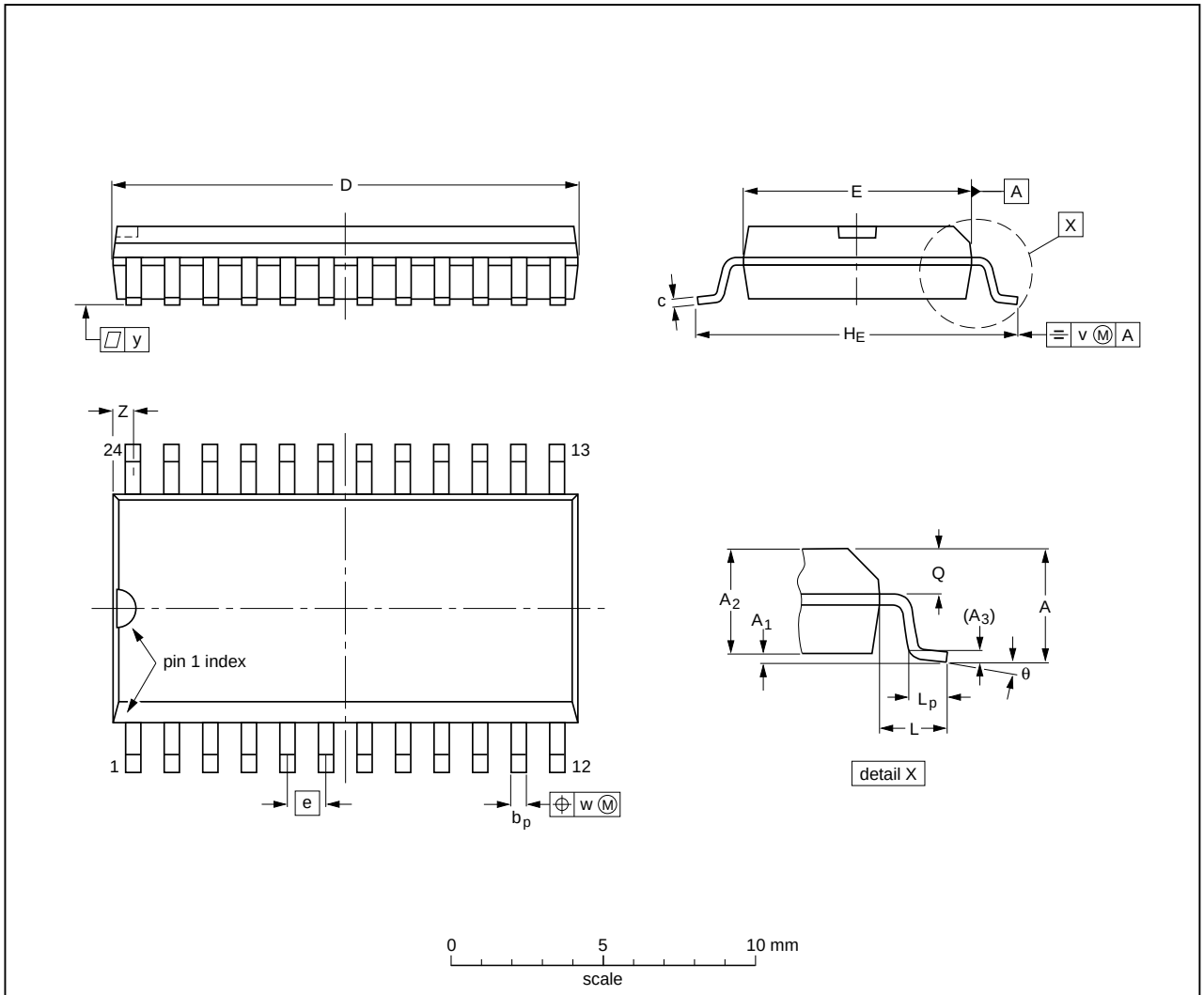
12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 20. Package outline SOT137 (SO24)

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13. Abbreviations

Table 8. Abbreviations

Acronym	Description
ANO	Adaptive Non-Overlap
CMOS	Complementary Metal-Oxide-Semiconductor'
CMR	Capacitive Mode Regulation
DMOS	Double-diffused Metal-Oxide-Semiconductor
EMI	ElectroMagnetic Interference
HBC	Half-Bridge Converter or Controller. Resonant converter which generates the regulated output voltage.
HFP	High-Frequency Protection
HV	High-voltage
OCR	OverCurrent Regulation
OLP	Open-Loop Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PFC	Power Factor Converter or Controller. Converter which performs the power factor correction.
UVP	UnderVoltage Protection
SCP	Short-Circuit Protection

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14. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1713LT v.1	20110624	Product data sheet	-	-

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15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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