

SM2GZ47, SM2GZ47A, SM2JZ47, SM2JZ47A

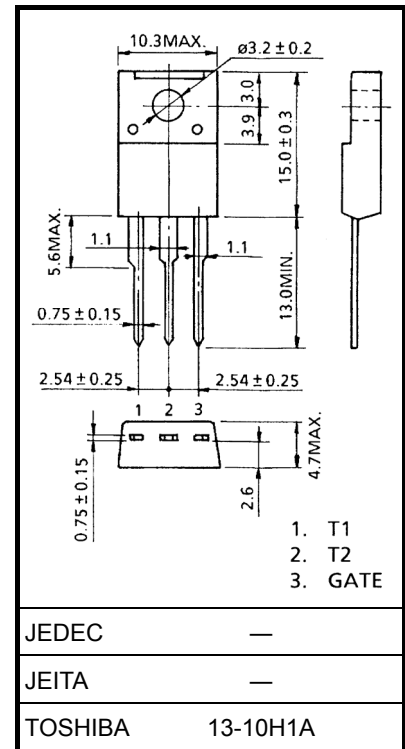
AC POWER CONTROL APPLICATIONS

Unit: mm

- I_T (RMS) = 1A ($T_a = 65^\circ\text{C}$ without radiator)
- Gate Trigger Current: $I_{GT} = 5\text{mA}$ Max. (TYPE "A")
- Repetitive Peak Off-State Voltage: $V_{DRM} = 400\text{V}, 600\text{V}$
- R.M.S On-State Current: I_T (RMS) = 2A ($T_c = 110^\circ\text{C}$)
- Isolation Voltage: $V_{ISOL} = 1500\text{V}$ (AC, $t = 60\text{s}$)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage and Repetitive Peak Reverse Voltage	V_{DRM}	400	V
		600	
R.M.S On-State Current (Full Sine Waveform)	I_T (RMS)	2	A
		1	
Peak One Cycle Surge On-State Current (Non-Repetitive)	I_{TSM}	8 (50Hz)	A
		8.8 (60Hz)	
I2t Limit Value	I_2t	0.32	A2s
Peak Gate Power Dissipation	P_{GM}	3	W
Average Gate Power Dissipation	$P_{G(AV)}$	0.3	W
Peak Gate Voltage	V_{FGM}	10	V
Peak Gate Current	I_{GM}	1.6	A
Junction Temperature	T_j	-40~125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40~125	$^\circ\text{C}$
Isolation Voltage (AC, $t = 1\text{min.}$)	V_{ISOL}	1500	V

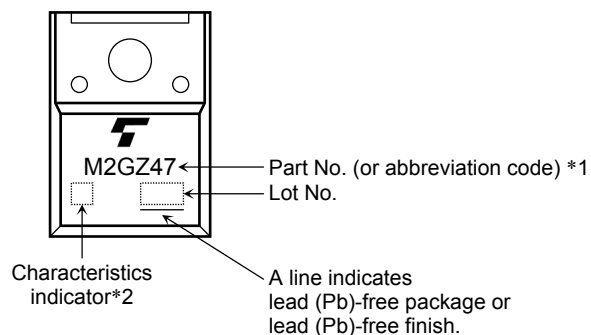


Weight: 1.7 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

MARKING

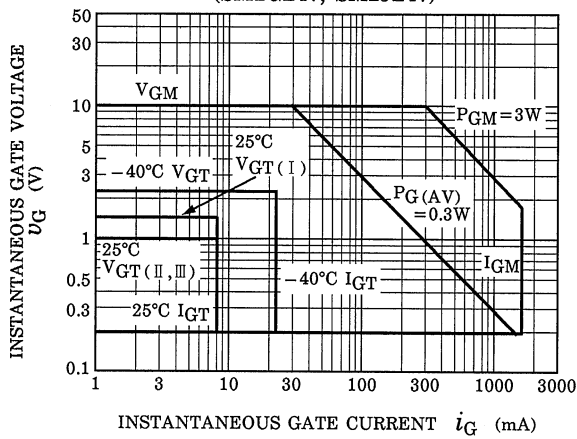


	Part No. (or abbreviation code)	Part No.
*1	M2GZ47	SM2GZ47, SM2GZ47A
	M2JZ47	SM2JZ47, SM2JZ47A
*2	Nothing	SM2GZ47, SM2JZ47
	A	SM2GZ47A, SM2JZ47A

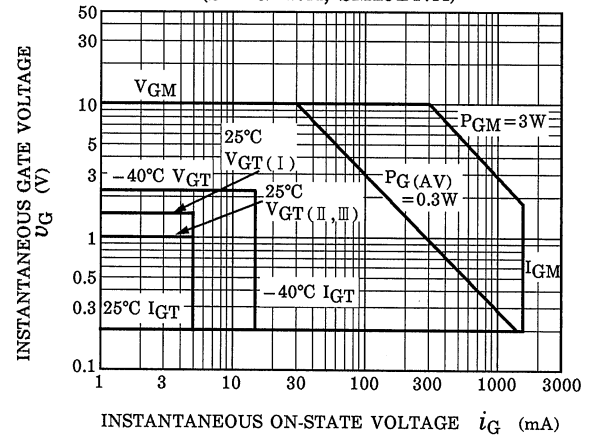
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT
Repetitive Peak Off-State Current		I _{DRM}	V _{DRM} = Rated		—	—	20	μA
Gate Trigger Voltage		I	V _{GT}	T2 (+) , Gate (+)	—	—	1.5	V
		II		T2 (+) , Gate (–)	—	—	1	
		III		T2 (–) , Gate (–)	—	—	1	
		IV		T2 (–) , Gate (+)	—	—	—	
Gate Trigger Current	SM2GZ47 SM2JZ47	I	I _{GT}	T2 (+) , Gate (+)	—	—	8	mA
		II		T2 (+) , Gate (–)	—	—	8	
		III		T2 (–) , Gate (–)	—	—	8	
		IV		T2 (–) , Gate (+)	—	—	—	
	SM2GZ47A SM2JZ47A	I		T2 (+) , Gate (+)	—	—	5	
		II		T2 (+) , Gate (–)	—	—	5	
		III		T2 (–) , Gate (–)	—	—	5	
		IV		T2 (–) , Gate (+)	—	—	—	
Peak On-State Voltage		V _{TM}	I _{TM} = 3A		—	—	1.7	V
Gate Non-Trigger Voltage		V _{GD}	V _D = Rated, T _c = 125°C		0.2	—	—	V
Holding Current		I _H	R _L = 100Ω		—	—	10	mA
Thermal Resistance		R _{th (j-a)}	Junction to Ambient, AC		—	—	55	°C / W

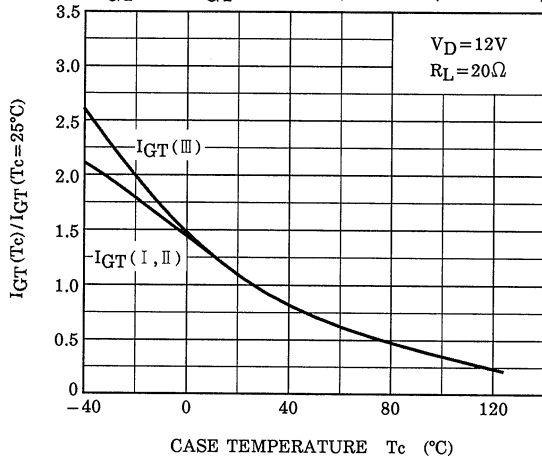
GATE TRIGGER CHARACTERISTIC
(SM2GZ47, SM2JZ47)



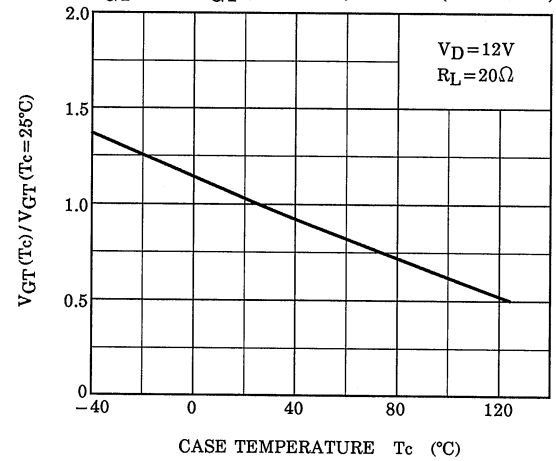
GATE TRIGGER CHARACTERISTIC
(SM2GZ47A, SM2JZ47A)



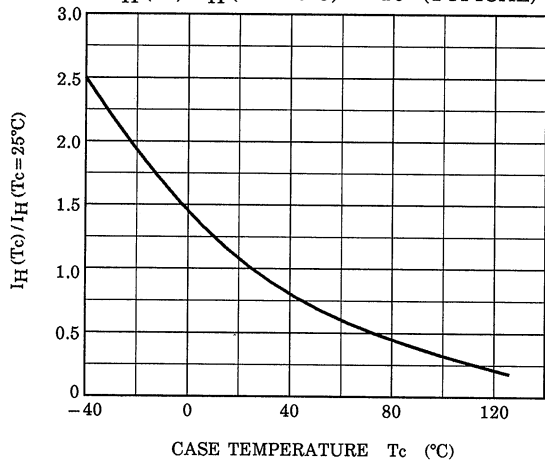
$I_{GT}(T_c)/I_{GT}(T_c=25^\circ\text{C}) - T_c$ (TYPICAL)



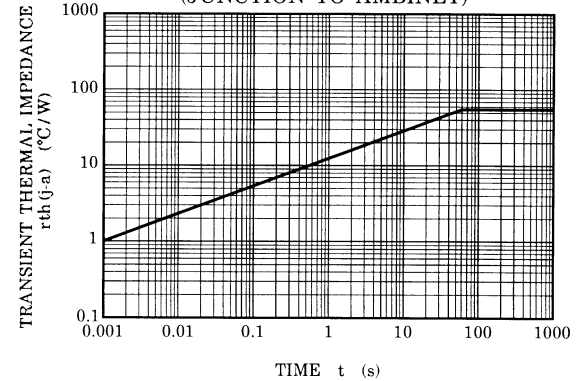
$V_{GT}(T_c)/V_{GT}(T_c=25^\circ\text{C}) - T_c$ (TYPICAL)

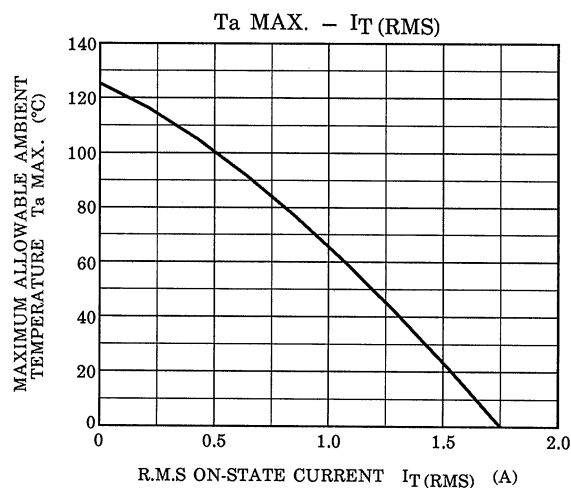
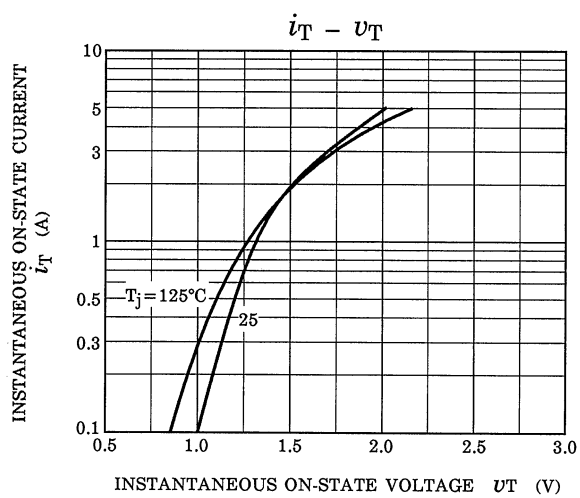


$I_H(T_c)/I_H(T_c=25^\circ\text{C}) - T_c$ (TYPICAL)



TRANSIENT THERMAL IMPEDANCE
(JUNCTION TO AMBIENT)





<CONDITION>

- ◆ NO HEAT SINK
- ◆ LEAD FORMING : LB182
- ◆ PRINT BOARD

$\left(\begin{array}{l} t=1.6\text{mm} \\ \text{SOLDER LAND : } 2\text{mm}\phi \end{array} \right)$

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20070701-EN

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