

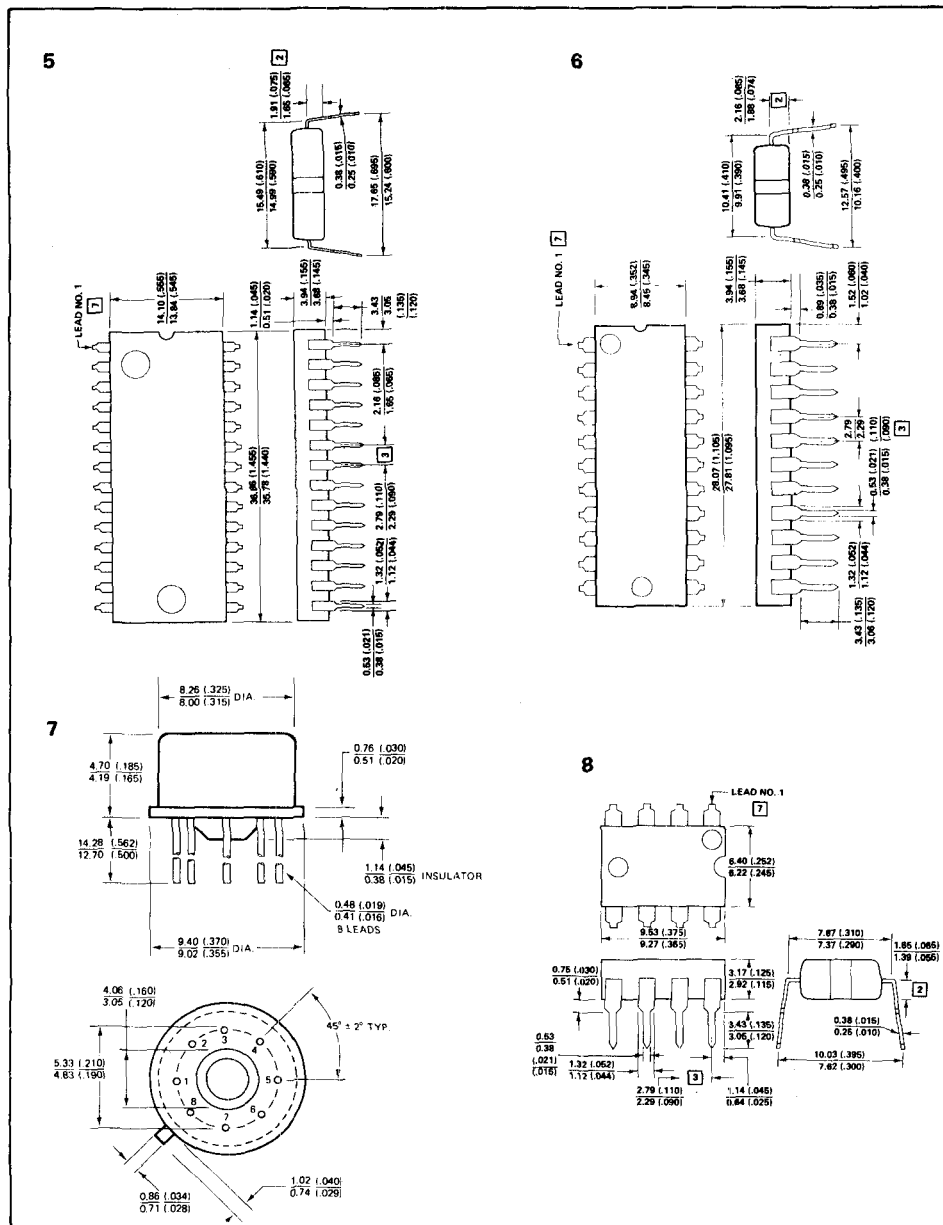
REFERENCE TABLE

TYPE NO.	DESCRIPTION	STOCK NO.	OUTLINE DRWG. NO.	CONNECTION DIAG. NO.
N74LS51N	Dual 2-Wide 2-Input AOI Gate	55673H	1	B39
N74LS54N	4-Wide 2-Input AOI Gate	55674F	1	B42
N74LS55N	2-Wide 4-Input AOI Gate	55675D	1	B218
N74LS73N	Dual J-K Master-Slave F/F	55676B	1	B52
N74LS74N	Dual D-Type Edge-Triggered F/F	55677X	1	B53
N74LS75N	Quad Bistable Latch	55678R	2	B54
N74LS76N	Dual J-K Master-Slave F/F	55679G	2	B55
N74LS78N	Dual J-K Negative Edge-Triggered F/F	55680X	2	B219
N74LS83AN	4-Bit Binary Full Adder	55681H	2	B58
N74LS85N	4-Bit Magnitude Comparator	55682F	2	B59
N74LS86N	Quad 2-Input Exclusive OR Gate	55683D	1	B60
N74LS90N	Decade Counter	55684B	1	B61
N74LS92N	Divide-By-Twelve Counter	55685X	1	B63
N74LS93N	4-Bit Binary Counter	55686R	1	B64
N74LS95BN	4-Bit Left-Right Shift Register	55687G	1	B66
N74LS96N	5-Bit Shift Register	55688E	2	B67
N74LS107N	Dual J-K Master-Slave F/F	55689C	1	B69
N74LS109N	Dual J-K Positive Edge Triggered F/F	55690F	2	B70
N74LS112N	Dual J-K Negative Edge Triggered F/F	55691D	2	B180
N74LS113N	Dual J-K Negative Edge Triggered F/F	55692B	1	B181
N74LS114N	Dual J-K Negative Edge Triggered F/F	55693X	1	B182
N74LS123N	Retriggerable Monostable Multivibrator	55694R	2	B74
N74LS125N	Quad Bus Buffer Gate w/Tri-state outputs	55695S	1	B75
N74LS126N	Quad Bus Buffer Gate w/Tri-state outputs	55696E	1	B76
N74LS132N	Quad Schmitt Trigger	55697C	1	B78
N74LS136N	Quad Exclusive OR O/C	55698A	1	B223
N74LS138N	3 to 1 of 8 Line Decoder/Demux	55699X	2	B186
N74LS139N	Dual 2 to 10 of 4 line Decoder/Demux	55700A	2	B187
N74LS145N	BCD-Decimal Decoder/Driver with o/c	55701X	2	B79
N74LS151N	8-Line to 1-Line Mux	55702H	2	B83
N74LS153N	Dual 4-Line to 1-Line Mux	55703F	2	B84
N74LS155N	Dual 2-Line to 4-Line Decoder/Demux	55704D	2	B86
N74LS157N	Quad 2-Input Data Selector (non-inv.)	55705B	2	B88
N74LS158N	Quad 2-Input Data Selector (inv.)	55706X	2	B89
N74LS160N	Synchronous 4-Bit Decade Counter	55707R	2	B90
N74LS161N	Synchronous 4-Bit Binary Counter	55708G	2	B91
N74LS162N	Synchronous 4-Bit Decade Counter	55709E	2	B92
N74LS163N	Synchronous 4-Bit Binary Counter	55710H	2	B93
N74LS164N	8-Bit Parallel Out Serial Shift Register	55711F	1	B94
N74LS170N	4 x 4 Register File	55712D	2	B97
N74LS173N	Quad D-Type F/F (Tri-State) (8T10)	55713B	2	B98
N74LS174N	Hex D-Type F/F with Clear	55714X	2	B99
N74LS175N	Quad D-Type Edge-Triggered F/F	55715R	2	B100
N74LS181N	4-Bit A/U	55716G	3	B106
N74LS190N	Synchronous UP/Down Counter (BCD)	55717E	2	B108
N74LS191N	Synchronous Up/Down Counter (Binary)	55718C	2	B109
N74LS192N	Synchronous Decade Up/Down Counter	55719A	2	B110
N74LS193N	Synchronous 4-Bit Binary Up/Down Counter	55720D	2	B111
N74LS194N	4-Bit Bidirectional Universal Shift Reg.	55721B	2	B112
N74LS195AN	4-Bit Parallel-Access Shift Reg.	55722X	2	B113
N74LS196N	Presetable Decade Counter/Latch (8290)	55723R	1	B114
N74LS197N	Presetable Binary Counter/Latch (8291)	55724G	1	B115
N74LS221N	Dual Monostable Multivibrator	55725E	2	B118
N74LS240N	Octal Inverter—3 State	55726C	2	B226
N74LS241N	Octal Buffer—2 State	55727A	2	B227
N74LS242N		55728X	1	B228
N74LS243N		55729H	2	B229
N74LS244N		55730X	4	B230
N74LS251N	Data Selector/Mux with 3-State outputs	55731R	2	B193
N74LS253N	Dual 4-Line to 1-Line Data Selector/Mux	55732G	2	B194
N74LS257N	Quad 2-Line to 1-Line Data Selector/Mux	55733E	2	B195
N74LS258N	Quad 2-Line to 1-Line Data Selector/Mux	55734C	2	B196

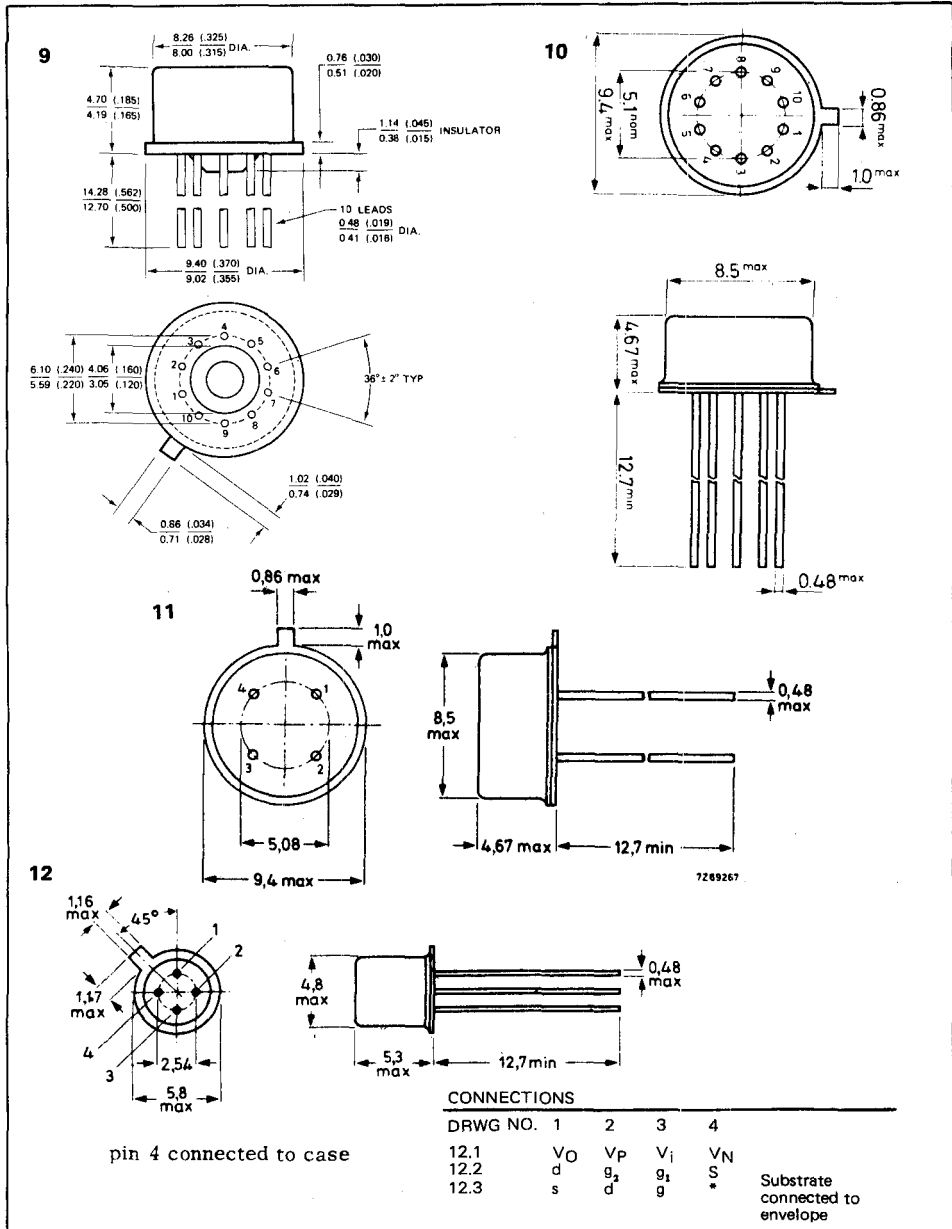
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Outline Drawings

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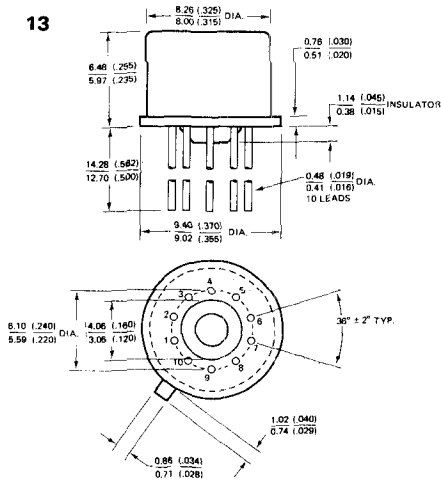
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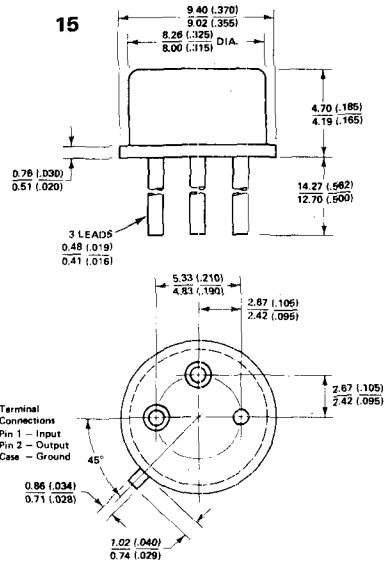
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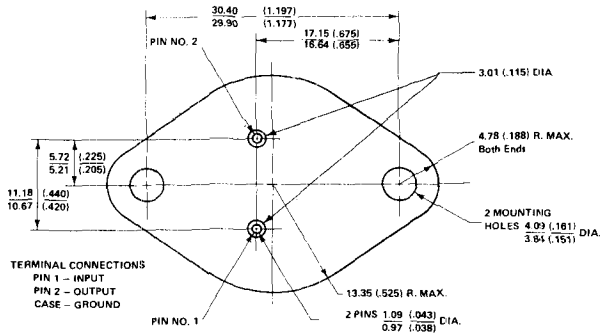
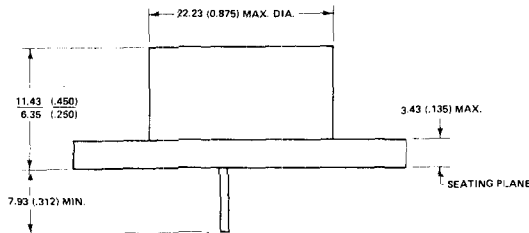
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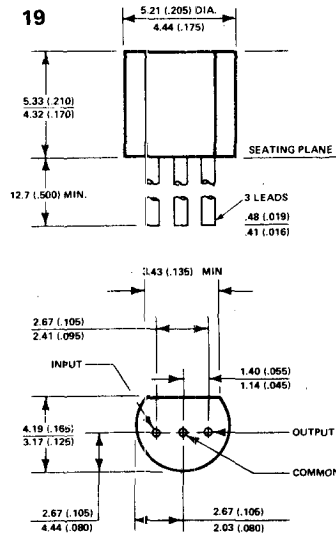
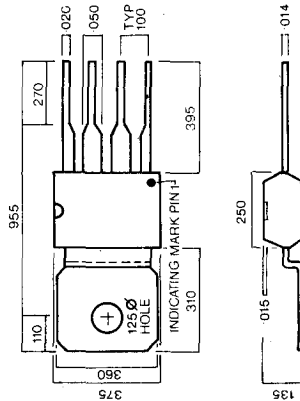
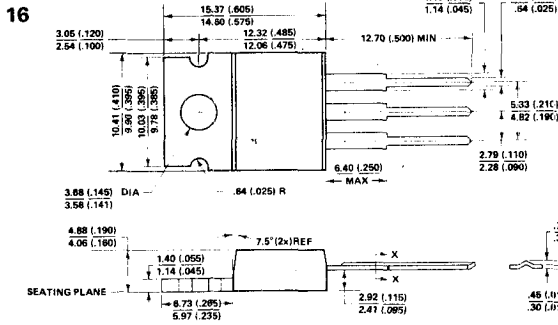


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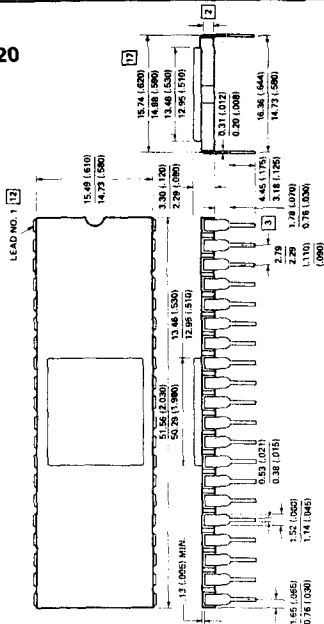
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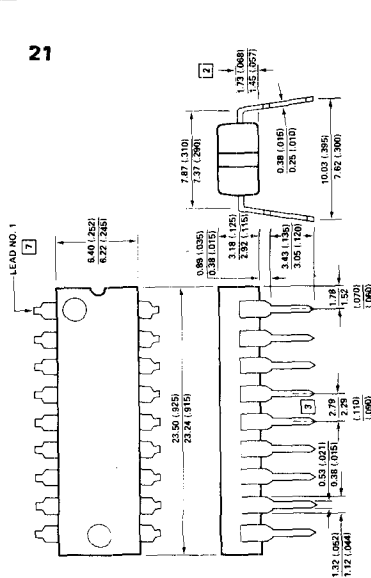
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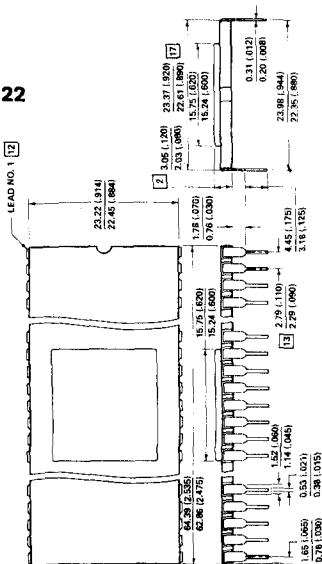
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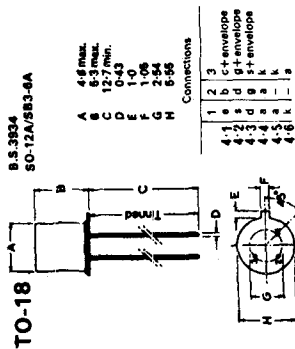
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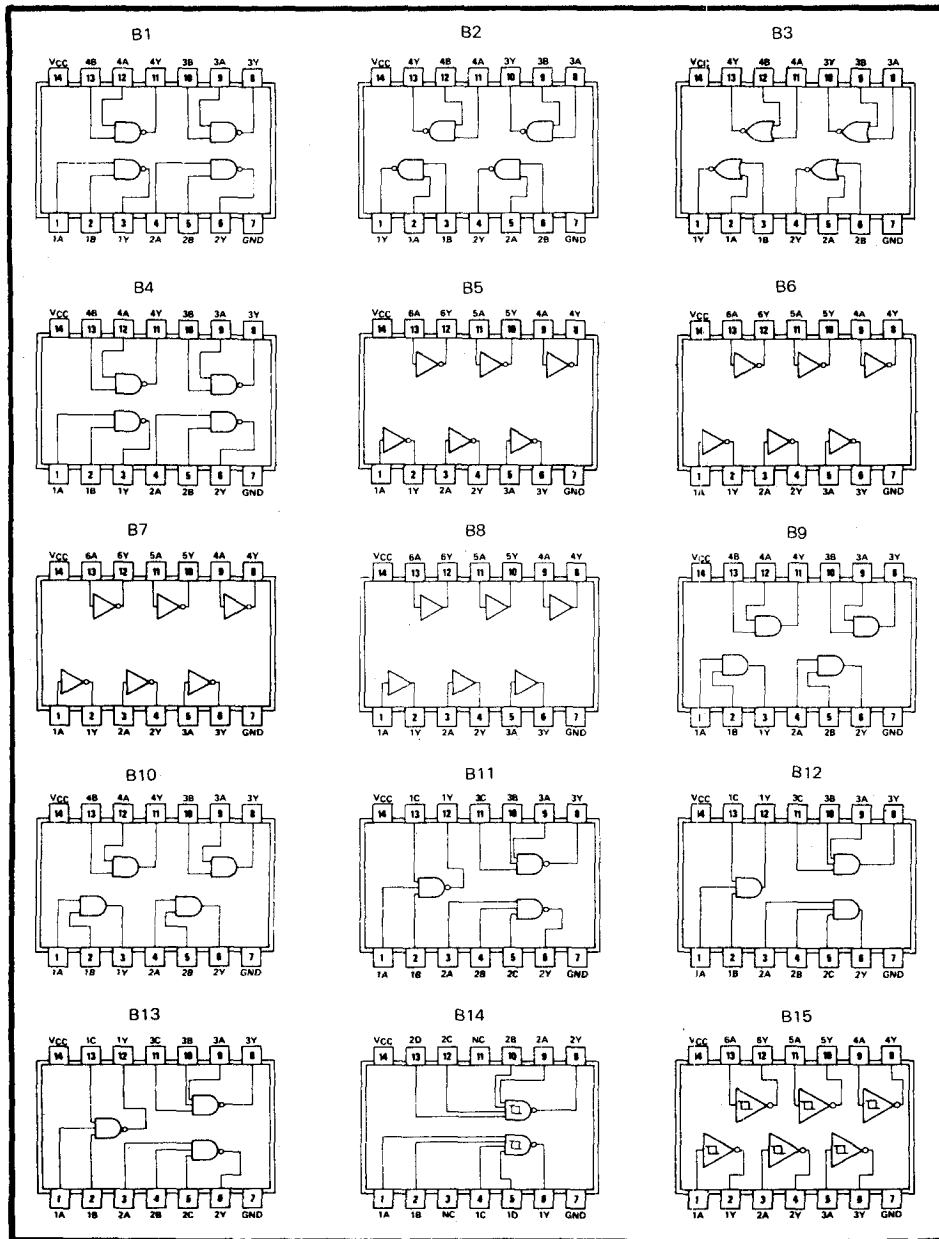


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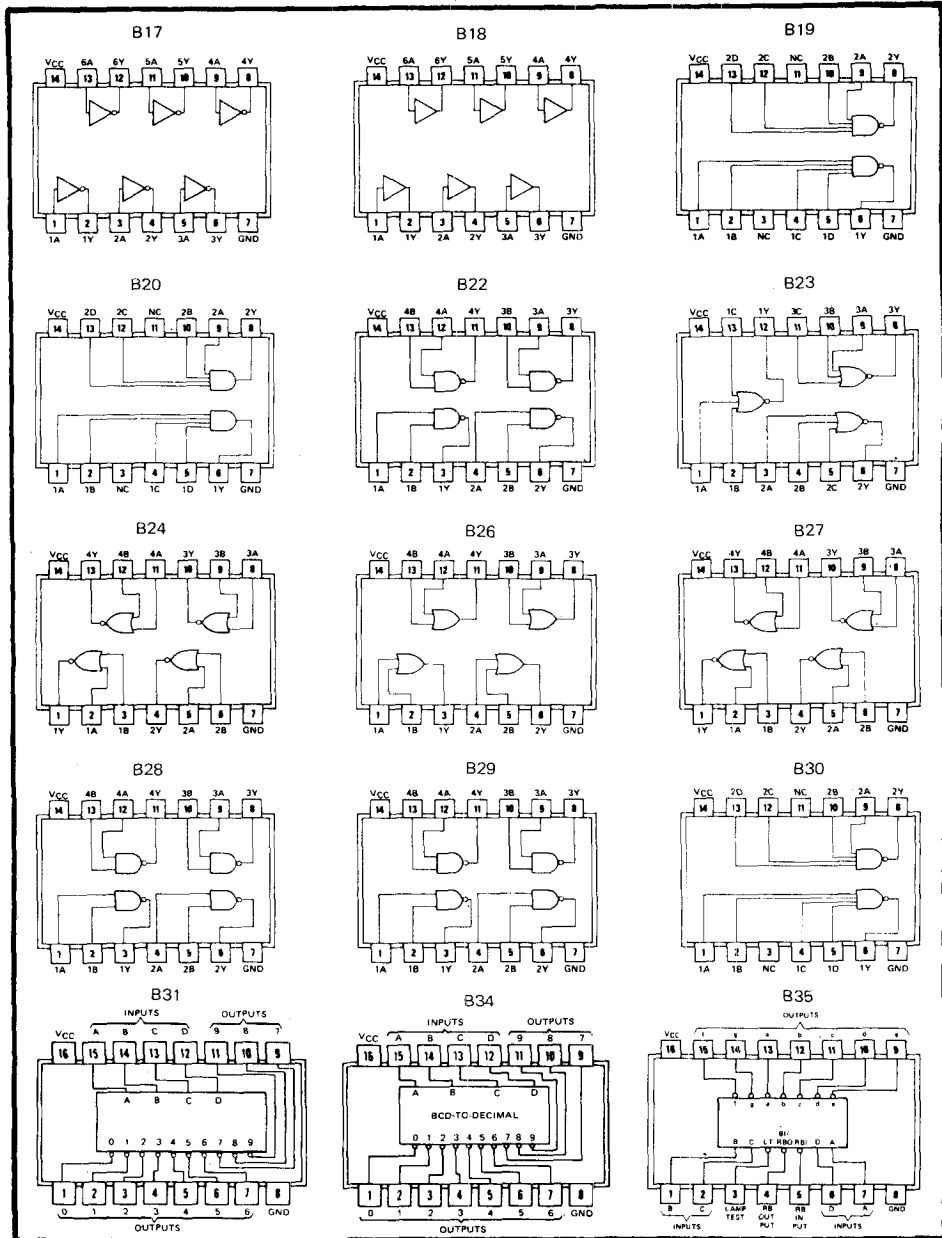


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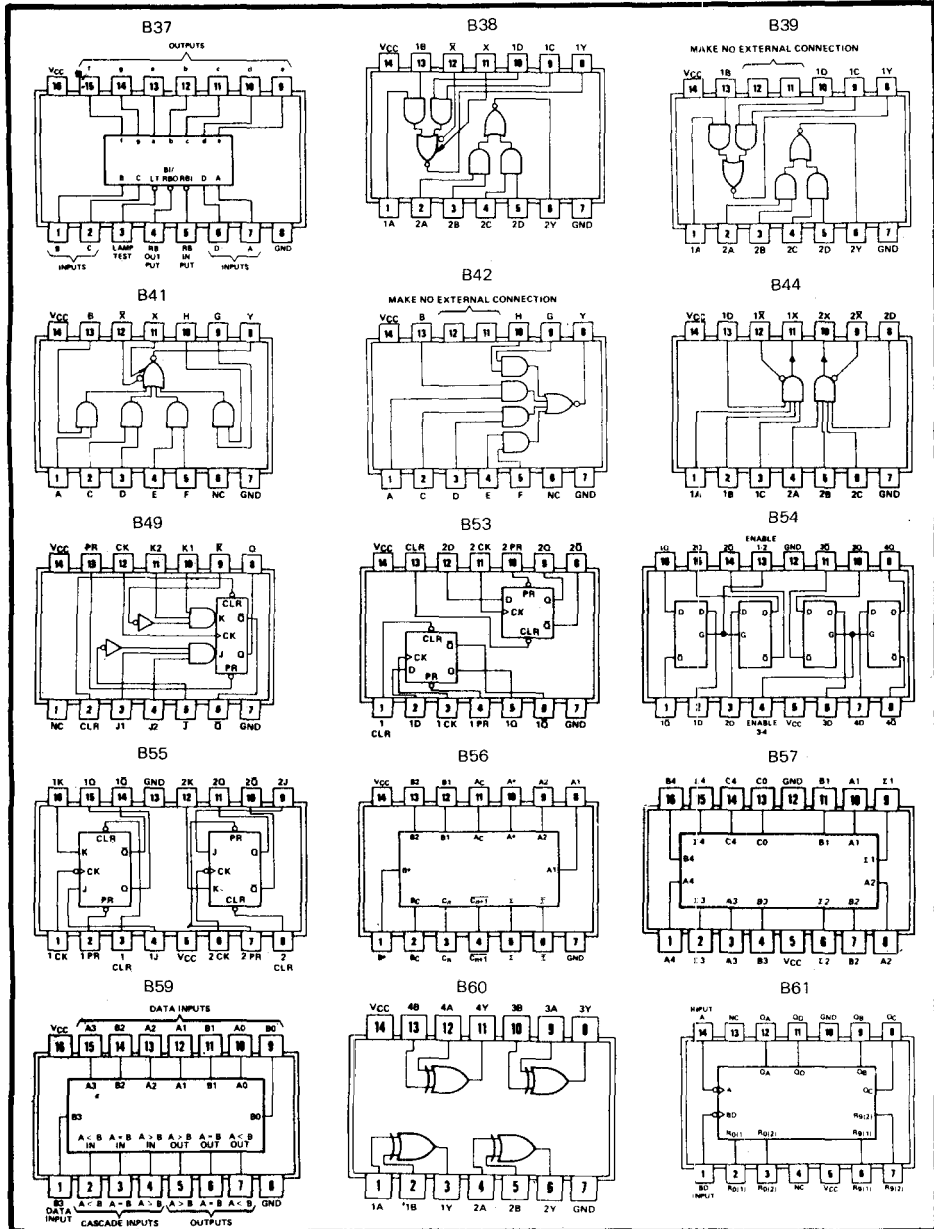
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Connection Diagram



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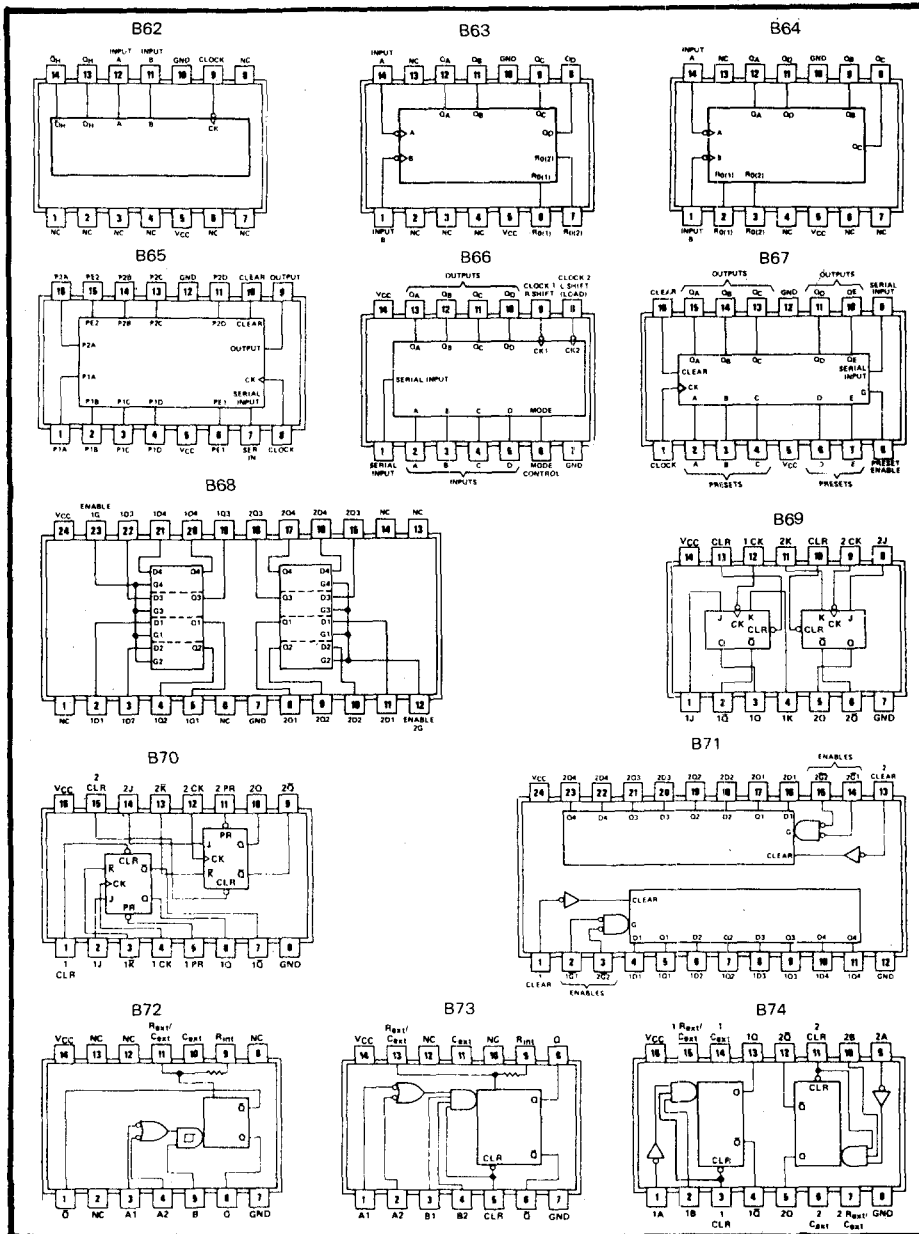


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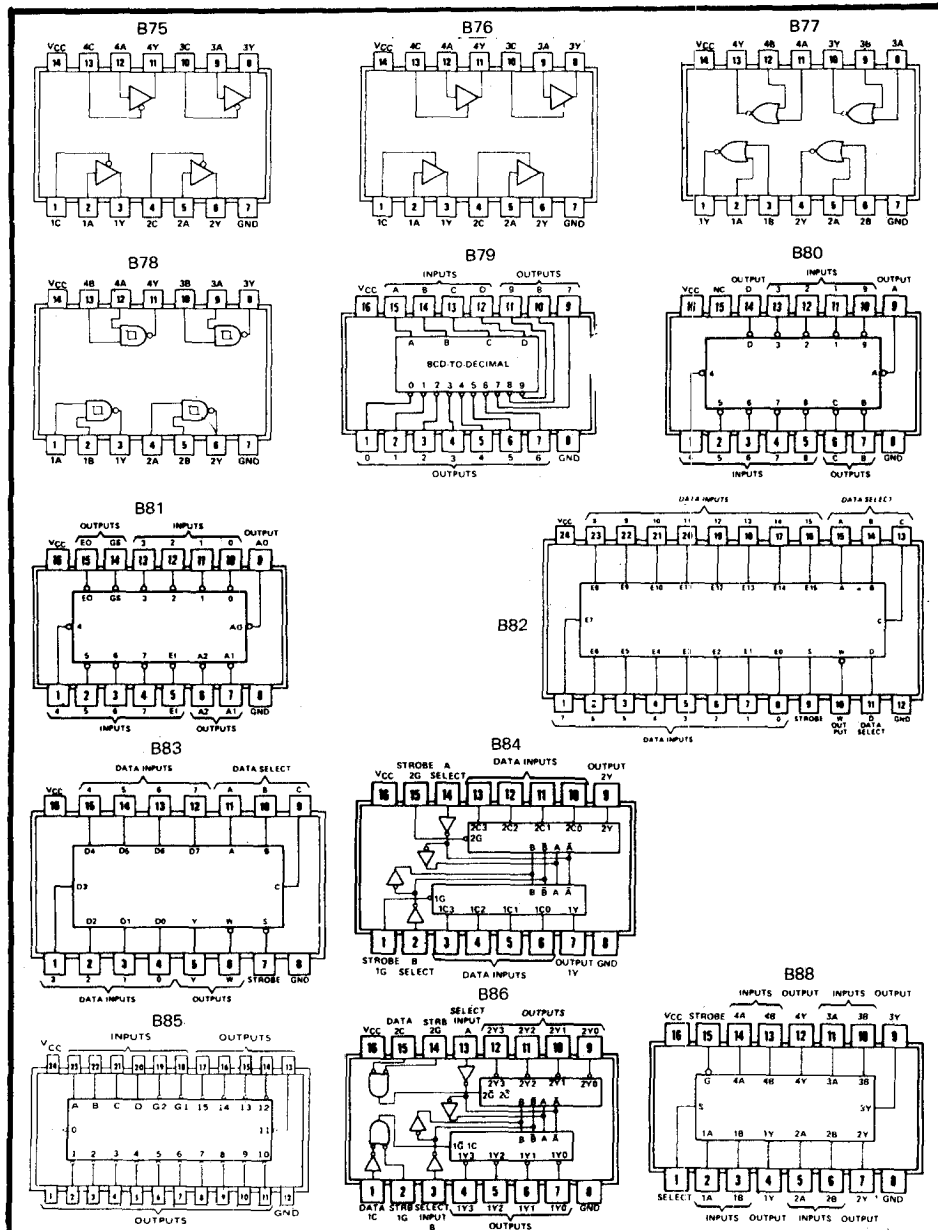


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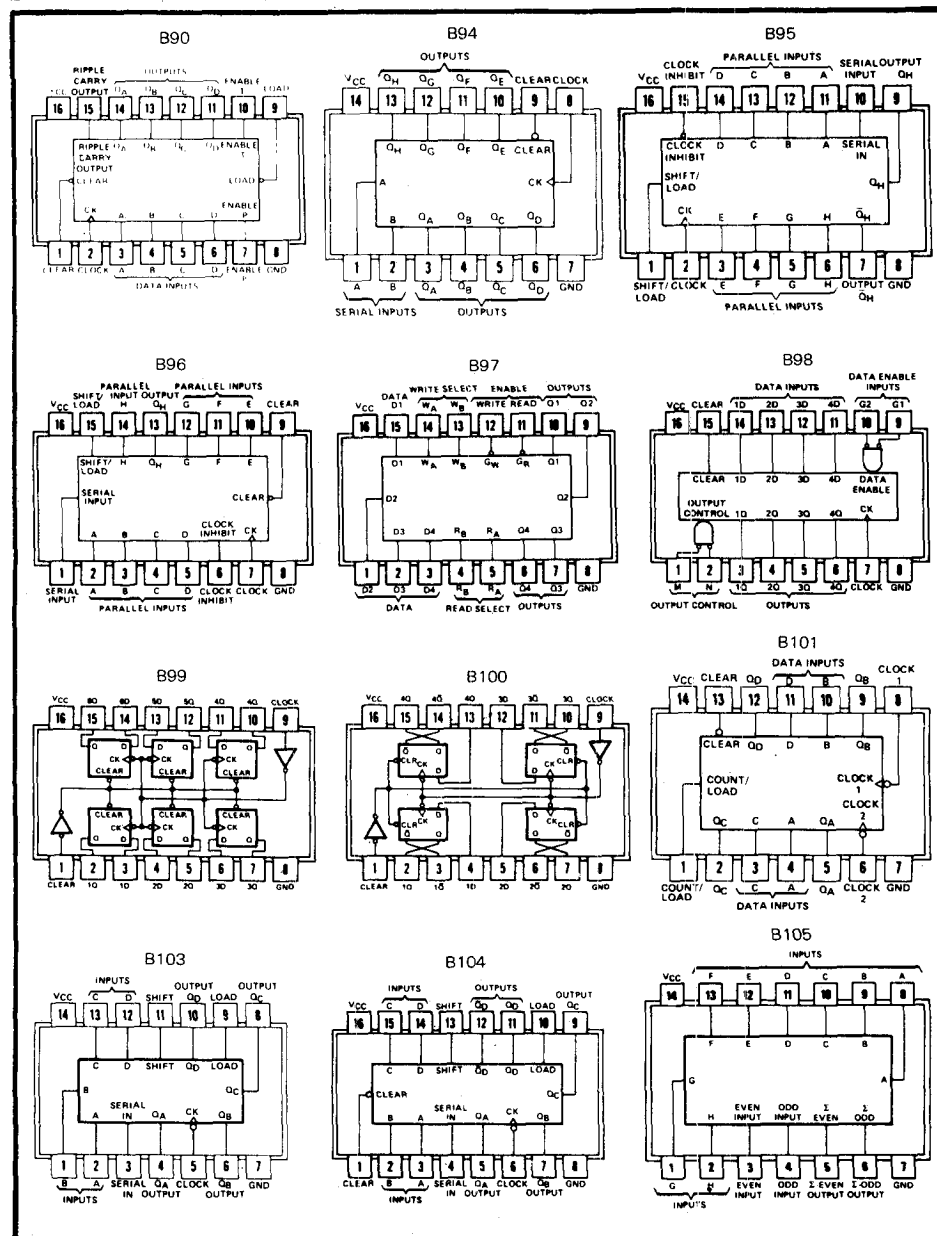
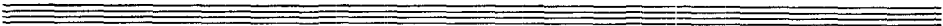
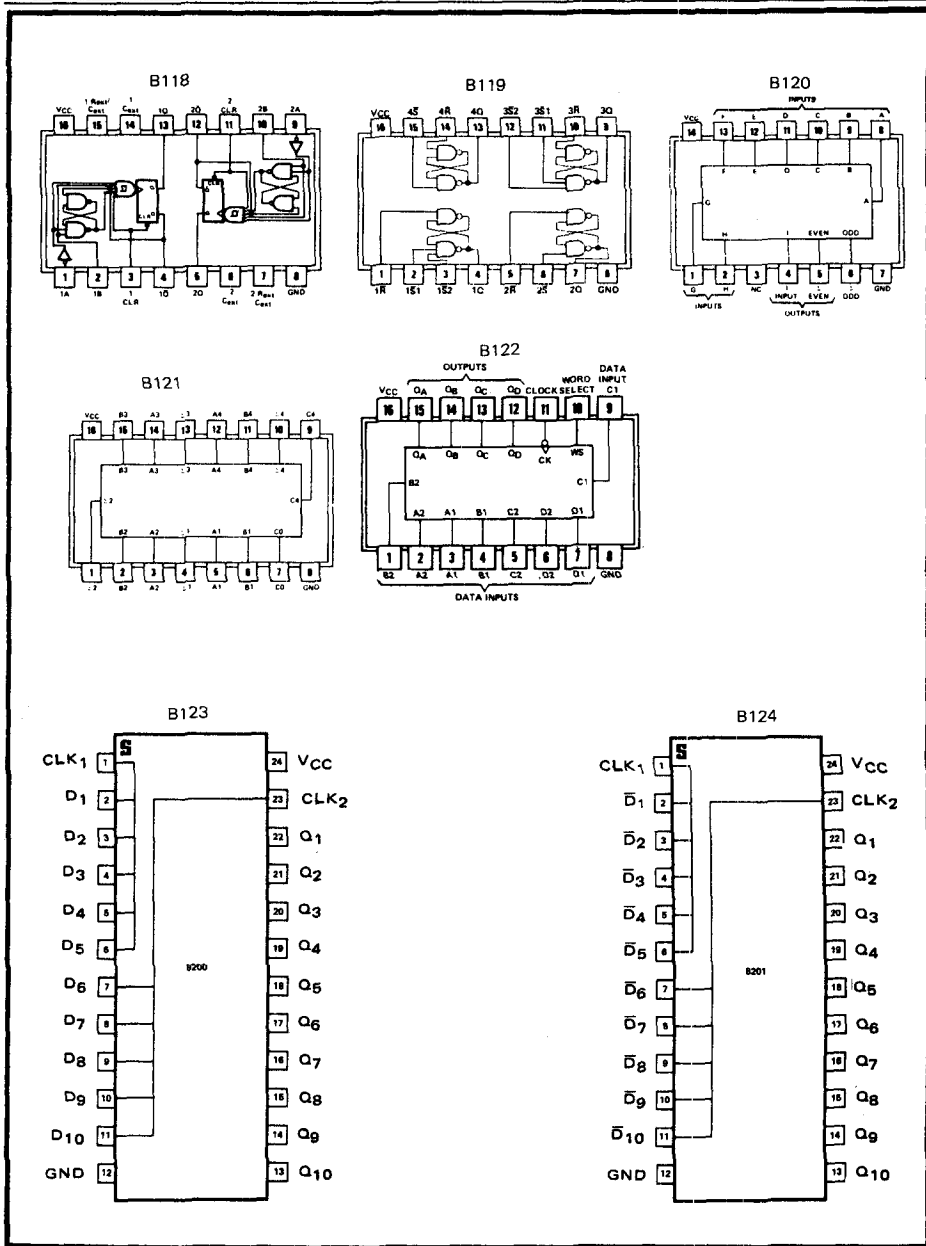


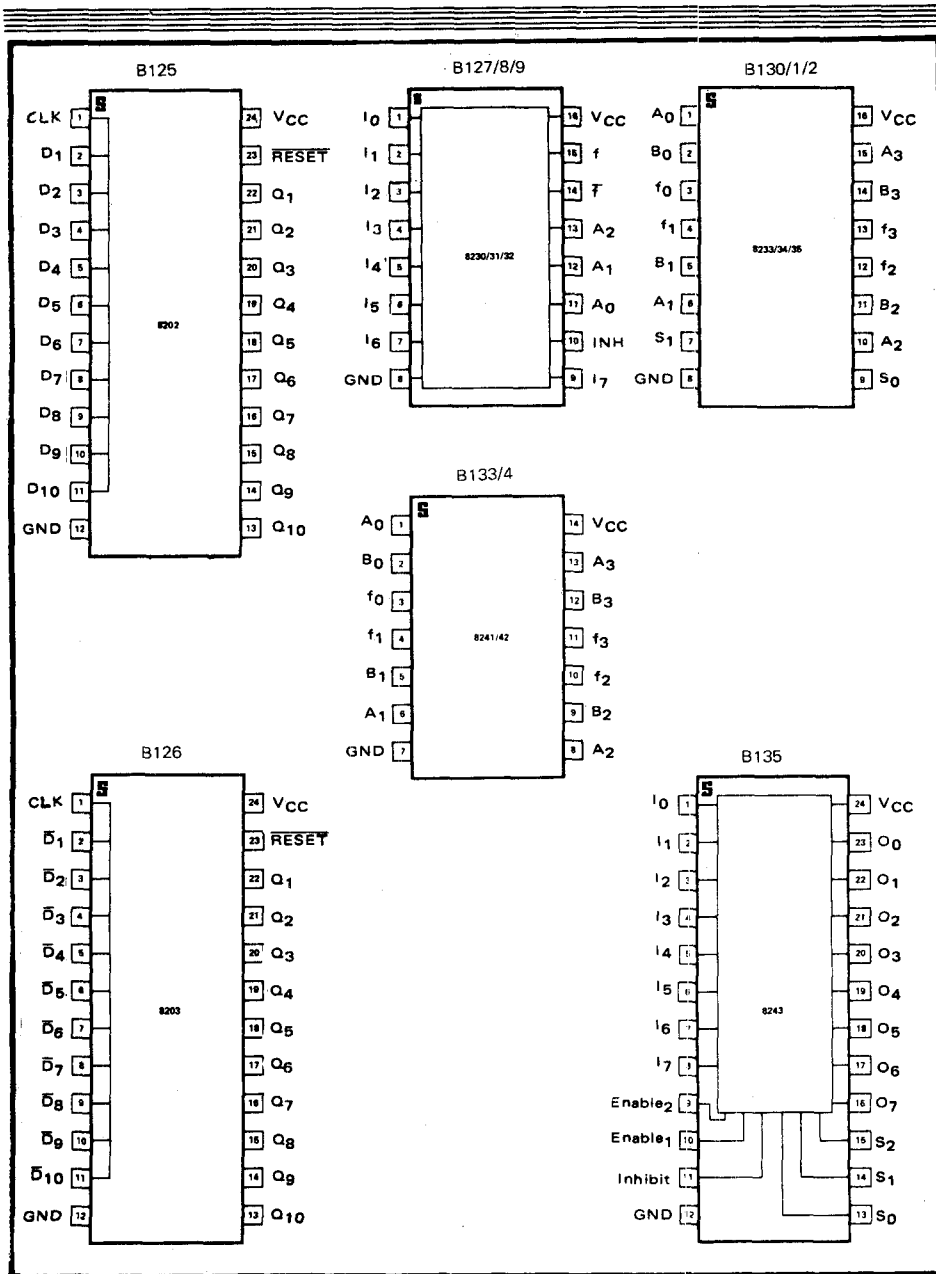
Figure 1: Schematic representation of the experimental design. The figure shows a timeline of the experiment. It starts with a 'Pretest' phase, followed by a 'Main Experiment' phase. The Main Experiment is divided into two parts: 'Part 1' and 'Part 2'. Part 1 involves a 'Pretest' and a 'Main Experiment' with 'Condition 1' and 'Condition 2'. Part 2 involves a 'Pretest' and a 'Main Experiment' with 'Condition 1' and 'Condition 2'. The timeline ends with a 'Posttest' phase.

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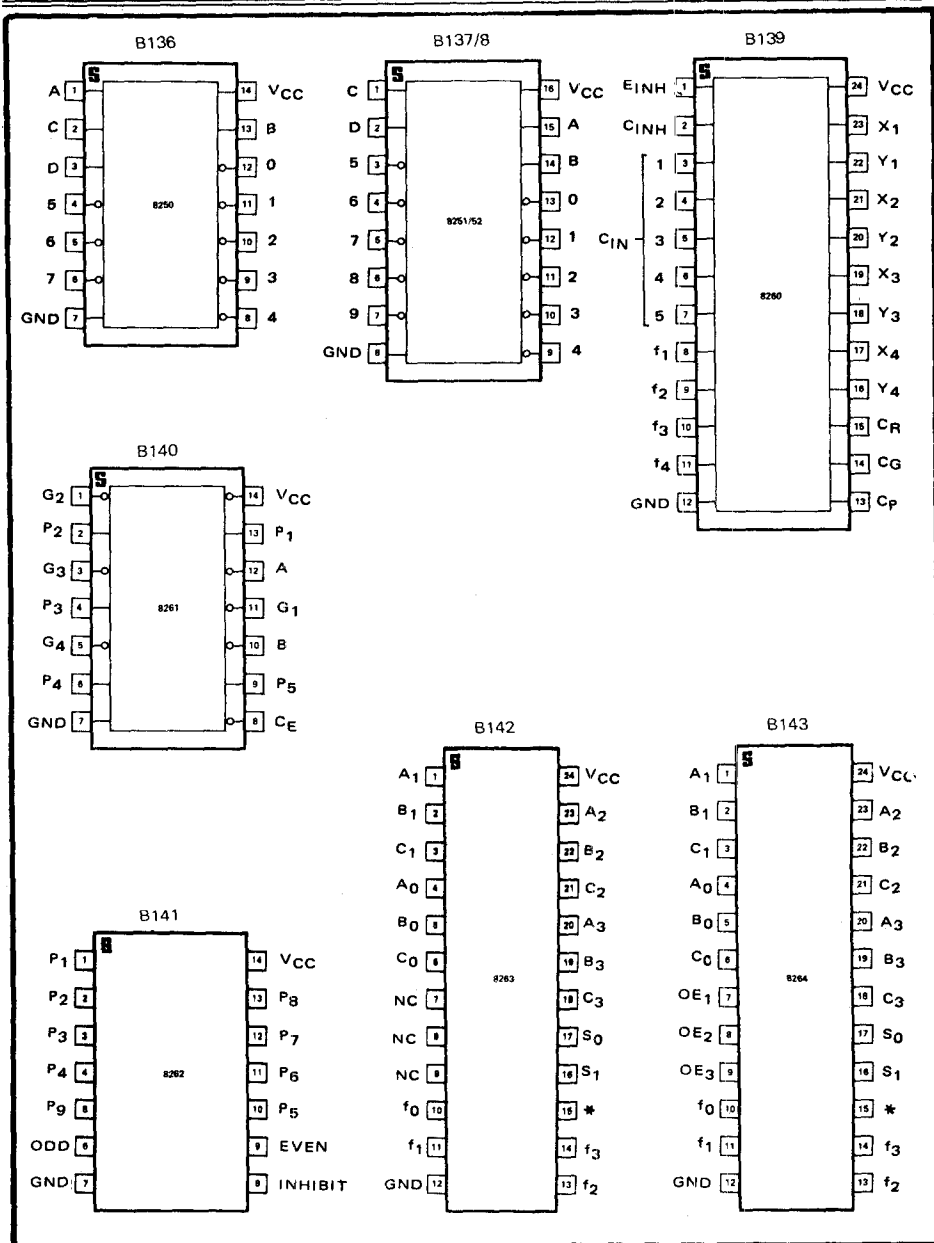
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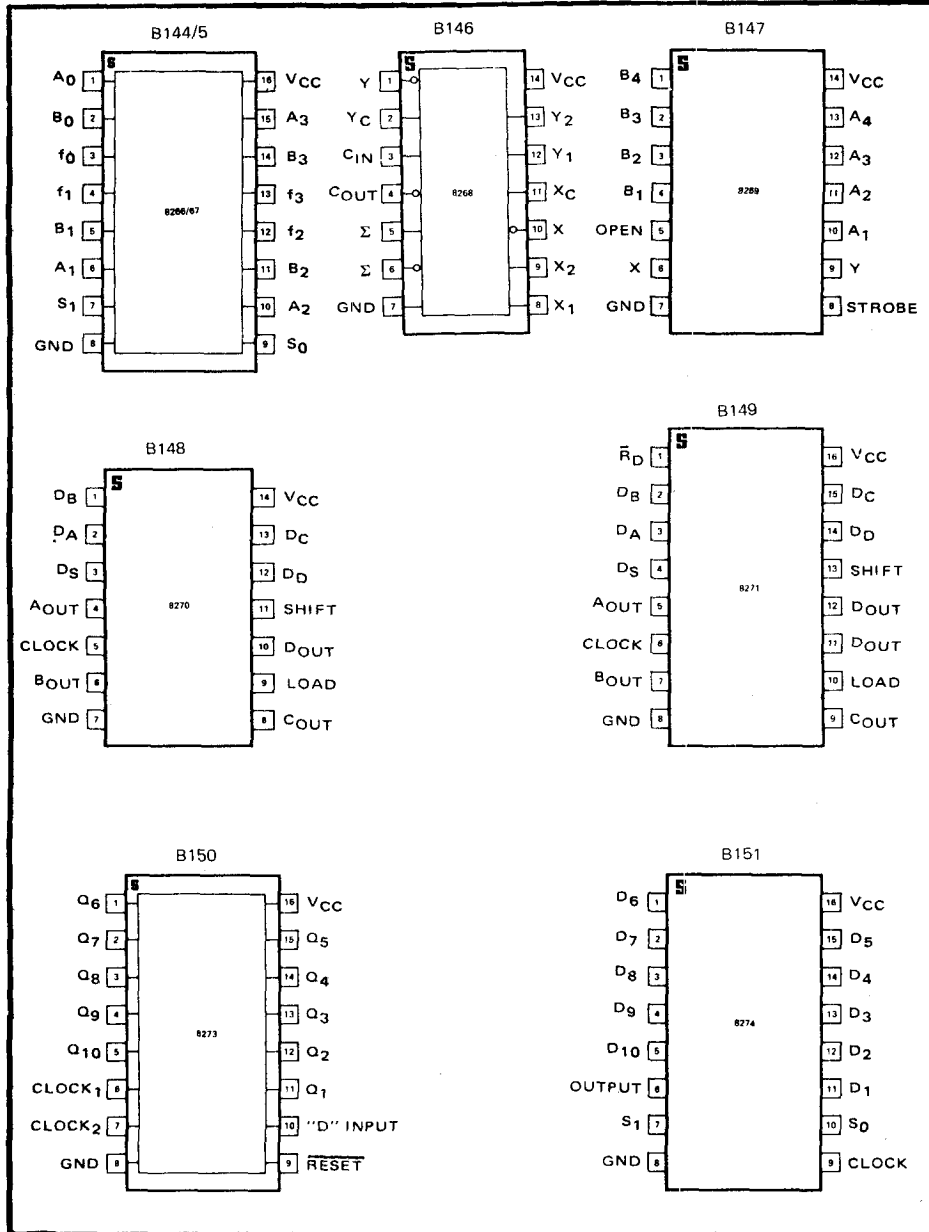
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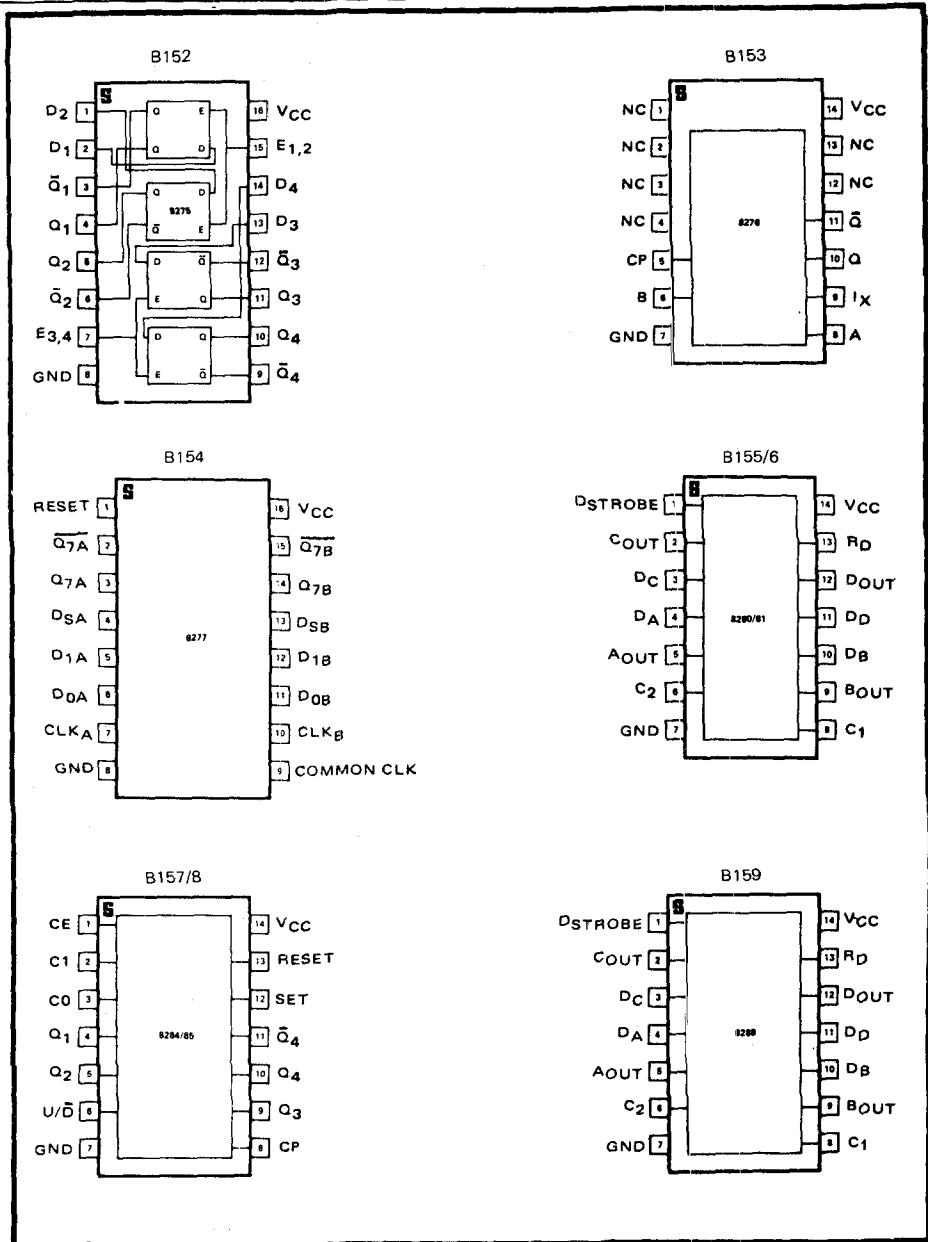
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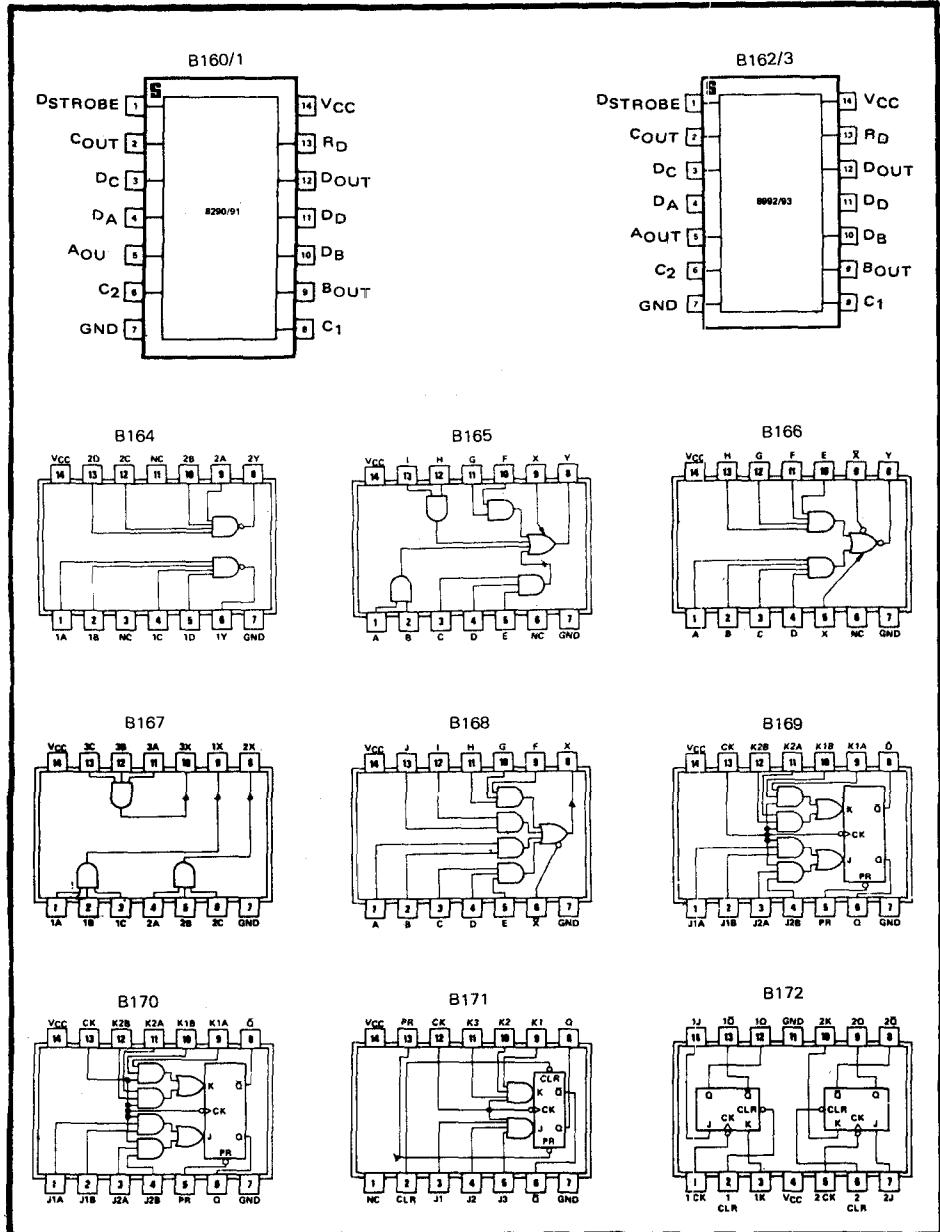
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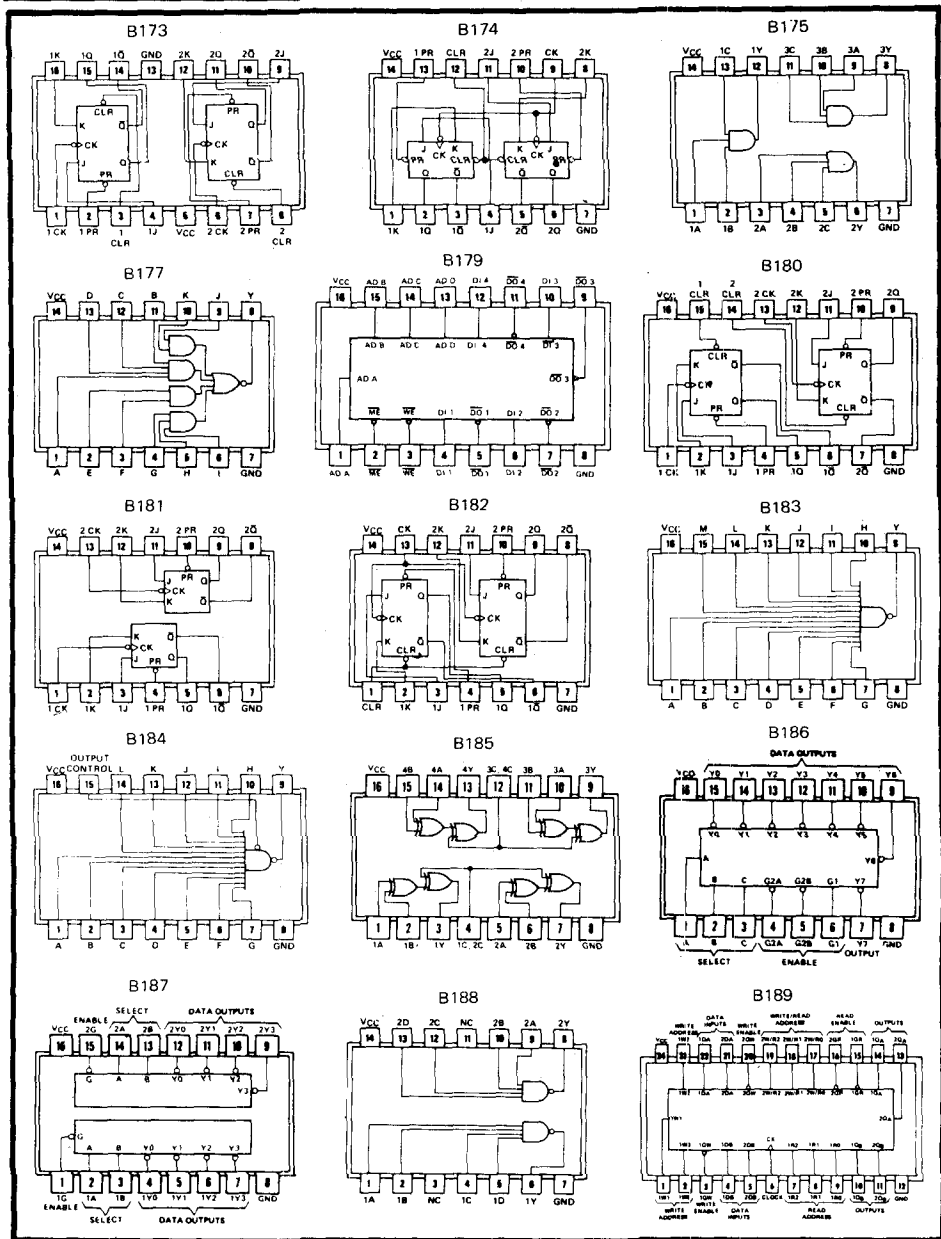


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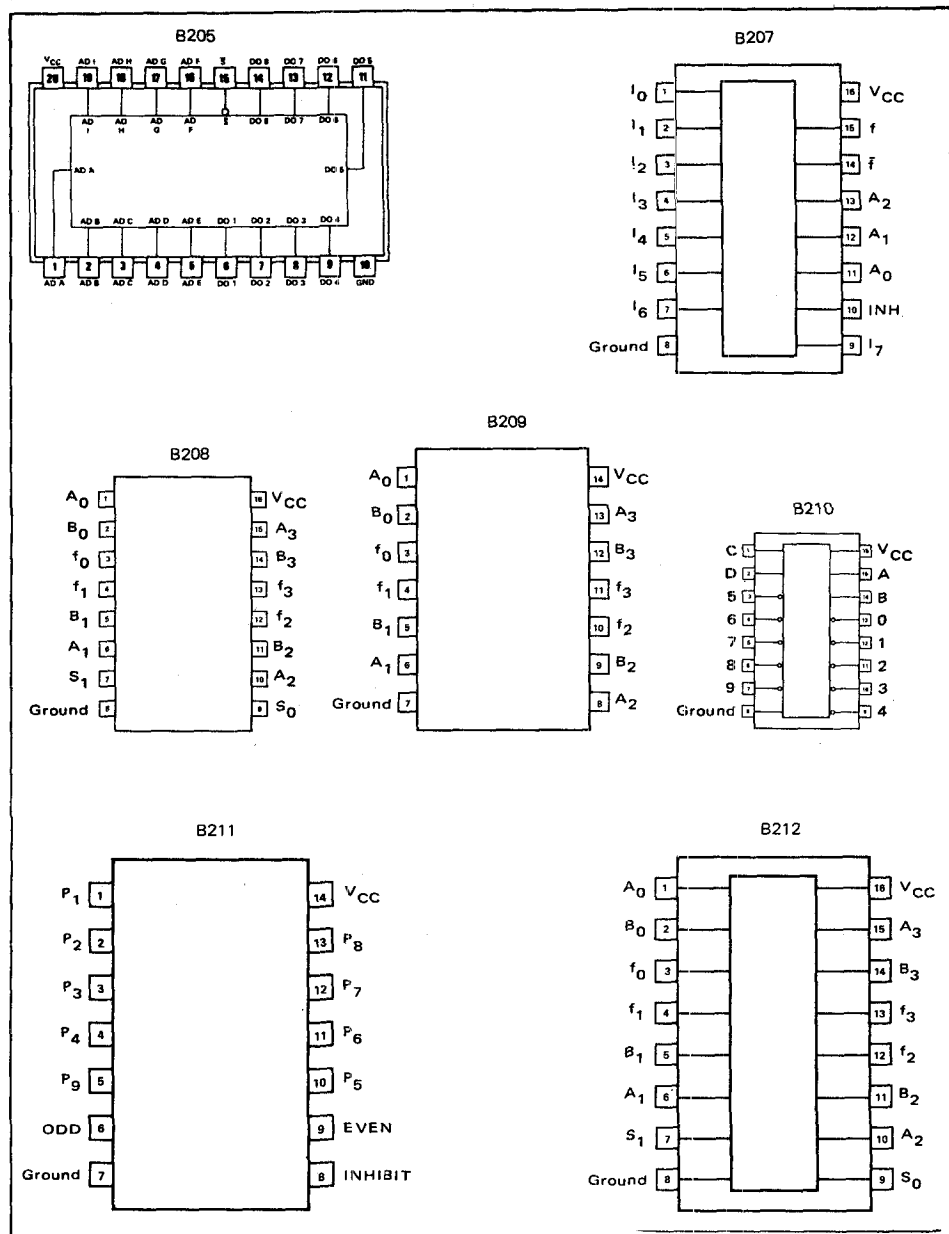


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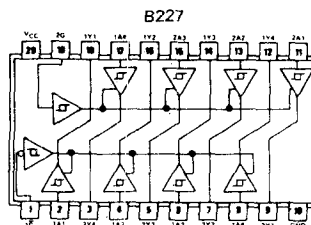
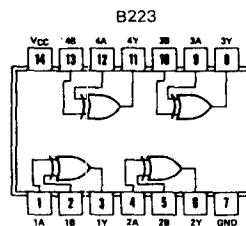
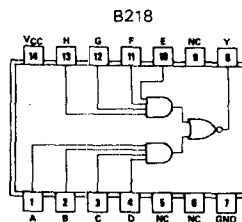
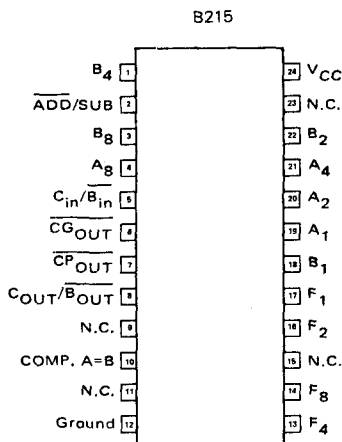
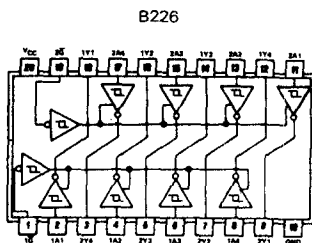
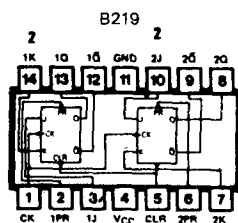
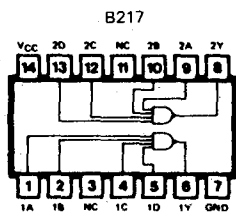
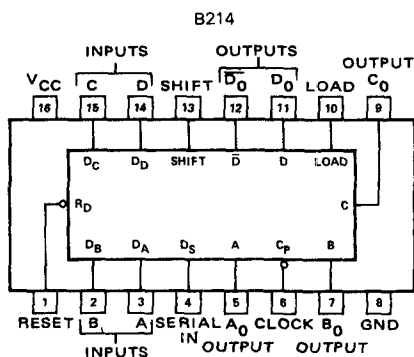
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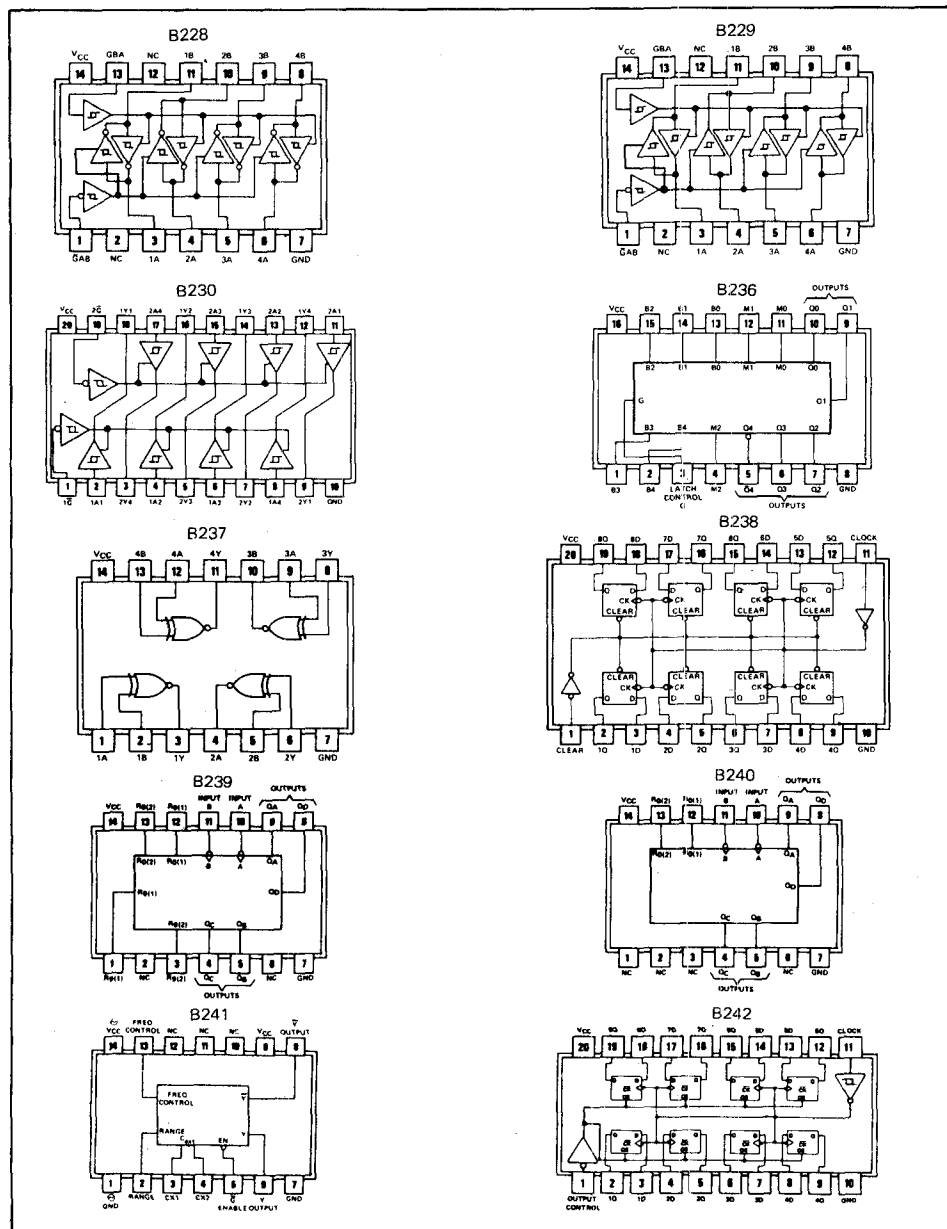
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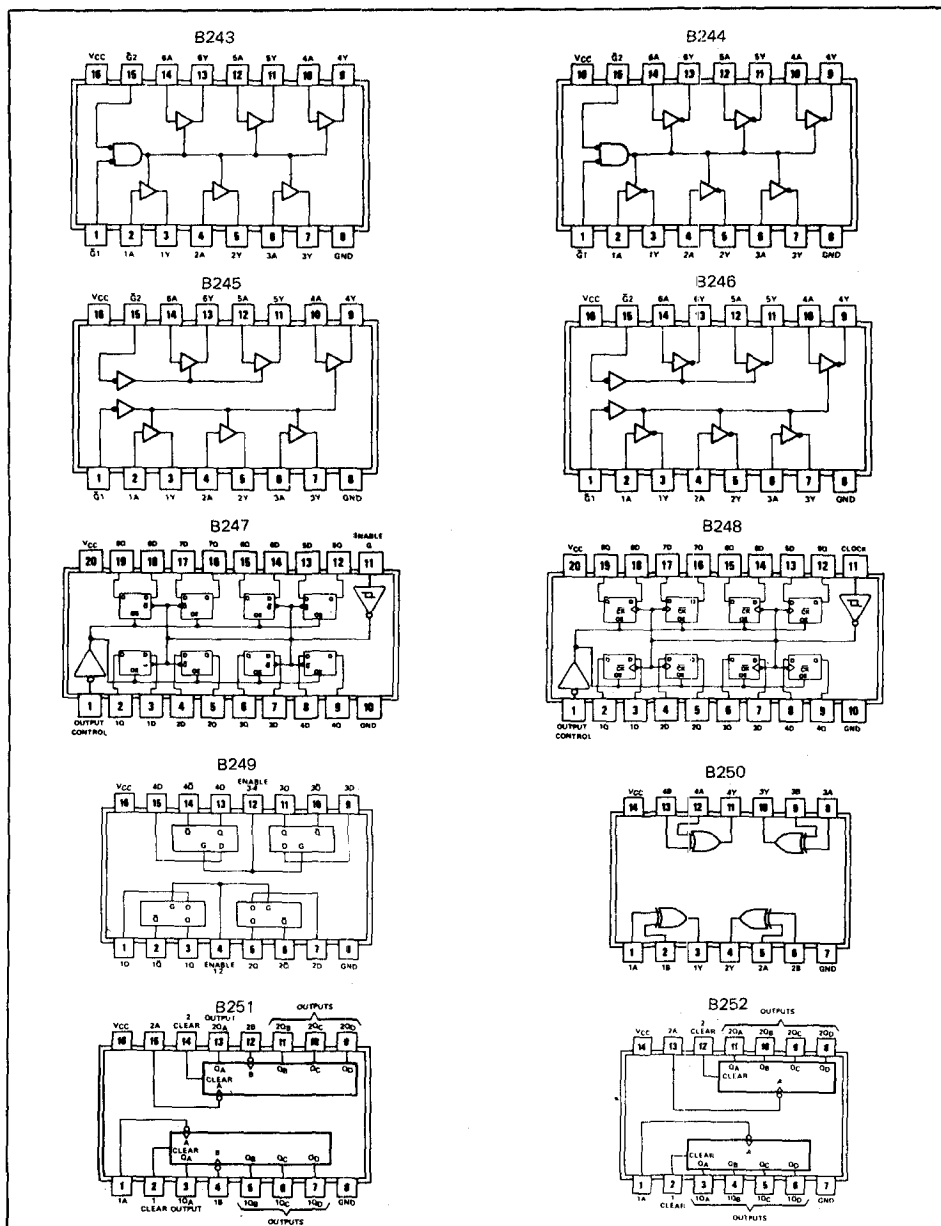
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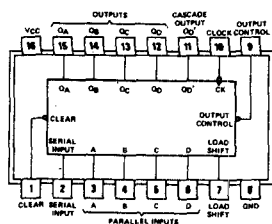
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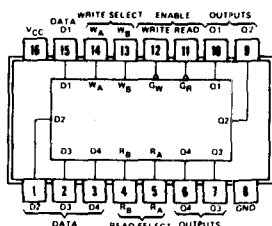
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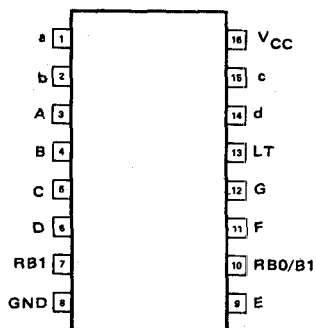
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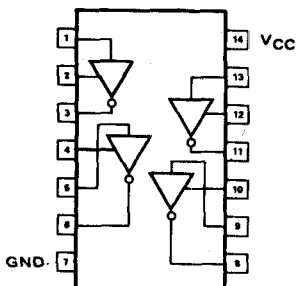
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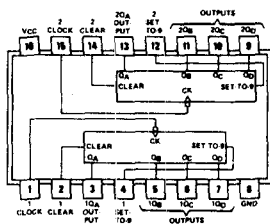
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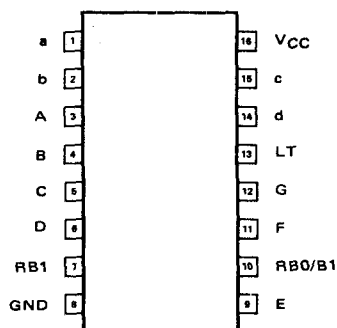
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