

**TOSHIBA**

TOSHIBA Original CMOS 16-Bit Microcontroller

**TLCS-900/L1 Series**

**TMP91C630**

**TOSHIBA CORPORATION**

Semiconductor Company

## Preface

Thank you very much for making use of Toshiba microcomputer LSIs.  
Before use this LSI, refer the section, "Points of Note and Restrictions".  
Especially, take care below cautions.

## CMOS 16-Bit Microcontrollers

### TMP91C630F

## 1. Outline and Features

TMP91C630 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment. With 2 Kbytes of boot ROM included, it allows your programs to be erased and rewritten on board.

TMP91C630 comes in a 100-pin flat package. Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)

- Instruction mnemonics are upward-compatible with TLCS-90/900
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: Four-channels (444 ns/2 bytes at 36 MHz)

(2) Minimum instruction execution time: 111 ns (at 36 MHz)

(3) Built-in RAM: 6 Kbytes

Built-in ROM: None

Built-in Boot ROM: 2 Kbytes

## RESTRICTIONS ON PRODUCT USE

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

- (4) External memory expansion
  - Expandable up to 16 Mbytes (shared program/data area)
  - Can simultaneously support 8-/16-bit width external data bus
    - ... Dynamic data bus sizing
- (5) 8-bit timers: 6 channels
  - Event counter :2 channels
- (6) 16-bit timer/event counter: 1 channel
- (7) Serial bus interface: 2 channels
- (8) 10-bit AD converter: 8 channels
- (9) Watchdog timer
- (10) Chip Select/Wait controller: 4 blocks
- (11) Interrupts: 35 interrupts
  - 9 CPU interrupts: Software interrupt instruction and illegal instruction
  - 19 internal interrupts: 7 priority levels are selectable.
  - 7 external interrupts: 7 priority levels are selectable.  
(Level mode, rising edge mode and falling edge mode are selectable.)
- (12) Input/output ports: 53 pins
- (13) Standby function
  - Three halt modes: Idle2 (programmable), Idle1, Stop
- (14) Operating voltage
  - VCC = 2.7 V to 3.6 V (fc max = 36 MHz)
- (15) Package
  - 100-pin QFP: P-LQFP100-1414-0.50F

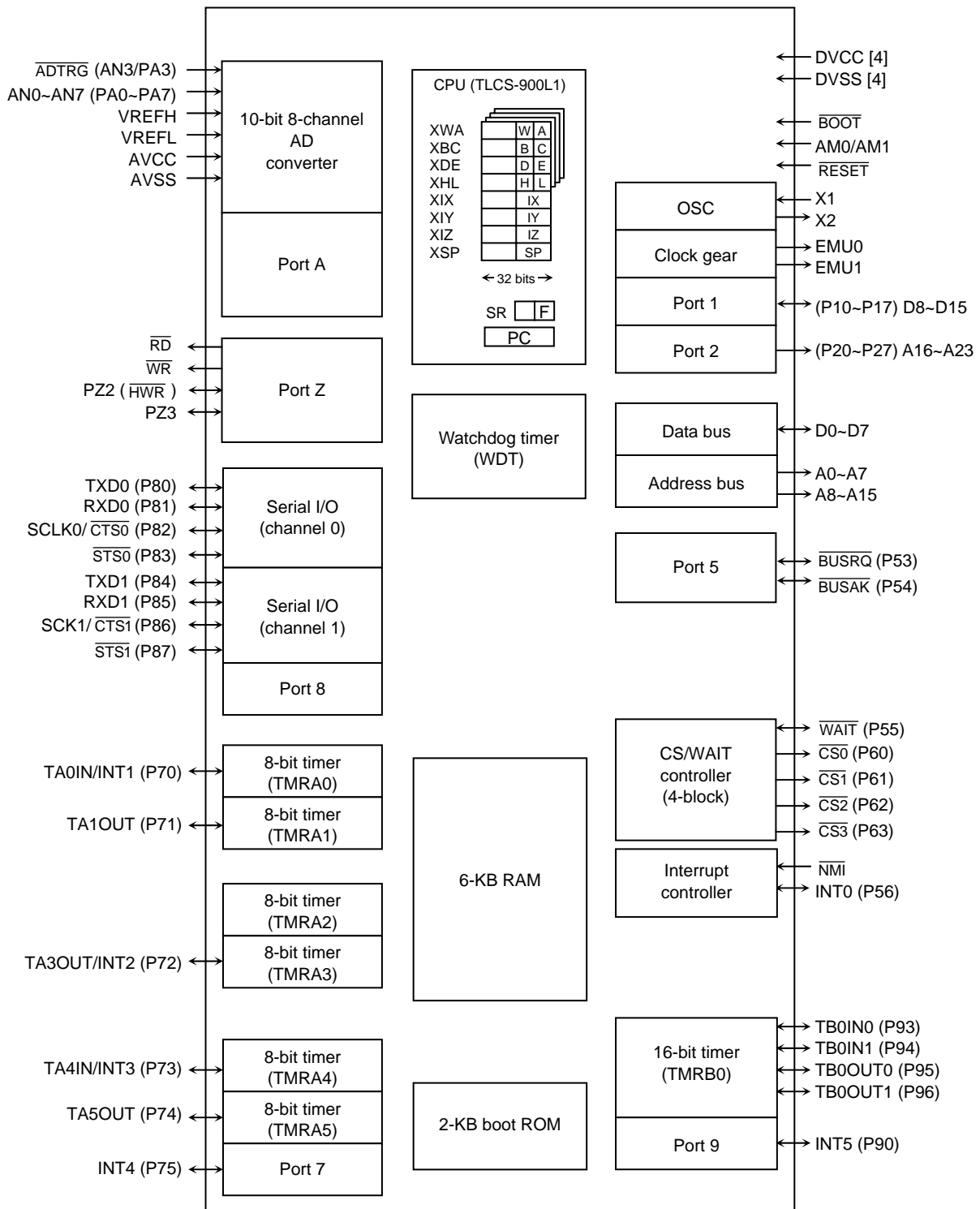


Figure 1.1 TMP91C630 Block Diagram

## 2. Pin Assignment and Pin Functions

The Pin Assignment and Pin Functions of the TMP91C630F are showed in Figure 2.1.1.

### 2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the TMP91C630F.

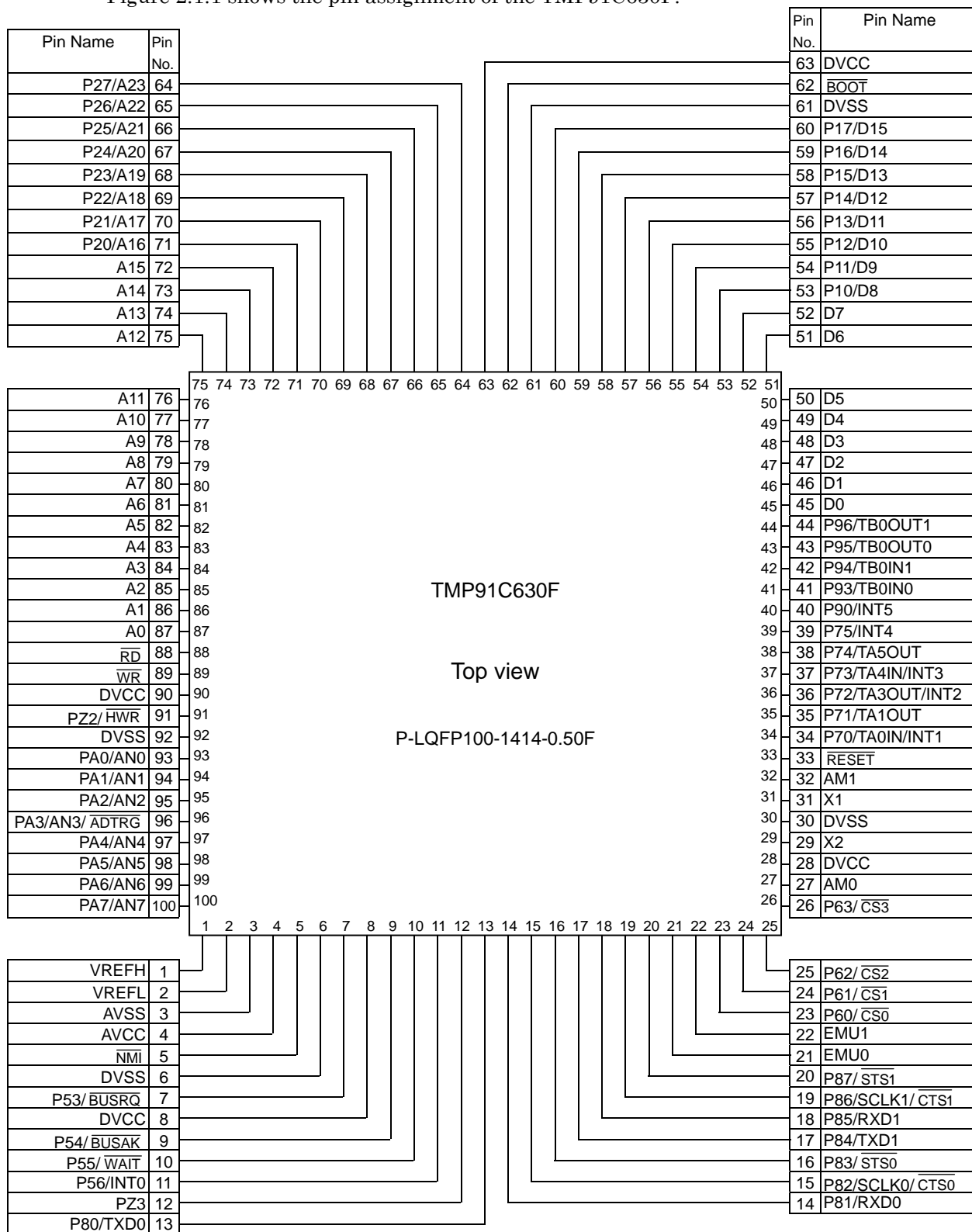


Figure 2.1.1 Pin Assignment Diagram (100-Pin LQFP)

## 2.2 Pin Names and Functions

The names of the Input/Output pins and their functions are described below.

Table 2.2.1 to Table 2.2.3 show Pin name and functions.

Table 2.2.1 Pin Names and Functions (1/3)

| Pin Names          | Number of Pins | I/O    | Functions   |
|--------------------|----------------|--------|---|
| D0 to D7           | 8              | I/O    | Data (lower): Bits 0 to 7 of data bus   |
| P10 to P17         | 8              | I/O    | Port 1: I/O port that allows I/O to be selected at the bit level<br>(When used to the external 8-bit bus) |
| D8 to D15          |                | I/O    | Data (upper): Bits 8 to 15 of data bus  |
| P20 to P27         | 8              | Output | Port 2: Output port   |
| A16 to A23         |                | Output | Address: Bits 16 to 23 of address bus   |
| A8 to A15          | 8              | Output | Address: Bits 8 to 15 of address bus  |
| A0 to A7           | 8              | Output | Address: Bits 0 to 7 of address bus   |
| $\overline{RD}$    | 1              | Output | Read: Strobe signal for reading external memory   |
| $\overline{WR}$    | 1              | Output | Write: Strobe signal for writing data to pins D0 to D7  |
| P53                | 1              | I/O    | Port 53: I/O port (with pull-up resistor)   |
| $\overline{BUSRQ}$ |                | Input  | Bus request: Signal used to request bus release (high-impedance).   |
| P54                | 1              | I/O    | Port 54: I/O port (with pull-up resistor)   |
| $\overline{BUSAk}$ |                | Output | Bus acknowledge: Signal used to acknowledge bus release (high-impedance).                                 |
| P55                | 1              | I/O    | Port 55: I/O port (with pull-up resistor)   |
| $\overline{WAIT}$  |                | Input  | Wait: Pin used to request CPU bus wait. ((1 + N) waits mode)  |
| P56                | 1              | I/O    | Port 56: I/O port (with pull-up resistor)   |
| INT0               |                | Input  | Interrupt request pin0: Interrupt request pin with programmable level/rising edge/falling edge            |
| P60                | 1              | Output | Port 60: Output port  |
| $\overline{CS0}$   |                | Output | Chip select 0: Outputs 0 when address is within specified address area.                                   |
| P61                | 1              | Output | Port 61: Output port  |
| $\overline{CS1}$   |                | Output | Chip select 1: Outputs 0 when address is within specified address area.                                   |
| P62                | 1              | Output | Port 62: Output port  |
| $\overline{CS2}$   |                | Output | Chip select 2: Outputs 0 when address is within specified address area.                                   |
| P63                | 1              | Output | Port 63: Output port  |
| $\overline{CS3}$   |                | Output | Chip select 3: Outputs 0 when address is within specified address area.                                   |
| P70                | 1              | I/O    | Port 70: I/O port   |
| TA0IN              |                | Input  | 8-bit TMRA0 input   |
| INT1               |                | Input  | Interrupt request pin 2: Interrupt request pin with programmable level/rising edge/falling edge           |
| P71                | 1              | I/O    | Port 71: I/O port   |
| TA1OUT             |                | Output | 8-bit TMRA0 or 8-bit TMRA1 output   |
| P72                | 1              | I/O    | Port 72: I/O port   |
| TA3OUT             |                | Output | 8-bit TMRA2 or 8-bit TMRA3 output   |
| INT2               |                | Input  | Interrupt request pin 2: Interrupt request pin with programmable level/rising edge/falling edge           |

Table 2.2.2 Pin Names and Functions (2/3)

| Pin Names   | Number of Pins | I/O                     | Functions   |
|---|----------------|-------------------------|---|
| P73<br>TA4IN<br>INT3                                  | 1              | I/O<br>Input<br>Input   | Port 73: I/O port<br>8-bit TMRA4 input<br>Interrupt request pin 3: Interrupt request pin with programmable level/rising edge/falling edge.                |
| P74<br>TA5OUT   | 1              | I/O<br>Output           | Port 74: I/O port<br>8-bit TMRA4 or 8-bit TMRA5 output  |
| P75<br>INT4   | 1              | I/O<br>Input            | Port 75: I/O port<br>Interrupt request pin 4: Interrupt request pin with programmable   |
| P80<br>TXD0   | 1              | I/O<br>Output           | Port 80: I/O port (with pull-up resistor)<br>Serial send data 0: Programmable open-drain output pin   |
| P81<br>RXD0   | 1              | I/O<br>Input            | Port 81: I/O port (with pull-up resistor)<br>Serial receive data 0  |
| P82<br>SCLK0<br>$\overline{\text{CTS0}}$              | 1              | I/O<br>Input<br>I/O     | Port 82: I/O port (with pull-up resistor)<br>Serial clock I/O 0<br>Serial data send enable 0 (Clear to send)  |
| P83<br>$\overline{\text{STS0}}$                       | 1              | I/O                     | Port 83: I/O port (with pull-up resistor)<br>Serial data request signal 0   |
| P84<br>TXD1   | 1              | I/O<br>Output           | Port 84: I/O port (with pull-up resistor)<br>Serial send data 0: Programmable open-drain output pin   |
| P85<br>RXD1   | 1              | I/O<br>Input            | Port 85: I/O port (with pull-up resistor)<br>Serial receive data 1  |
| P86<br>SCLK1<br>$\overline{\text{CTS1}}$              | 1              | I/O<br>Input<br>I/O     | Port 86: I/O port (with pull-up resistor)<br>Serial clock I/O 1<br>Serial data send enable 1 (Clear to send)  |
| P87<br>$\overline{\text{STS1}}$                       | 1              | I/O                     | Port 87: I/O port (with pull-up resistor)<br>Serial data request signal 1   |
| P90<br>INT5   | 1              | I/O<br>Input            | Port 90: I/O port<br>Interrupt request pin 5: Interrupt request pin with programmable level/rising edge/falling edge                                      |
| P93<br>TB0IN0   | 1              | I/O<br>Input            | Port 93: I/O port<br>Timer B0 input 0   |
| P94<br>TB0IN1   | 1              | I/O<br>Input            | Port 94: I/O port<br>Timer B0 input 1   |
| P95<br>TB0OUT0  | 1              | I/O<br>Output           | Port 95: I/O port<br>Timer B0 output 0  |
| P96<br>TB0OUT1  | 1              | I/O<br>Output           | Port 96: I/O port<br>Timer B0 output 1  |
| PA0 to PA7<br>AN0 to AN7<br>$\overline{\text{ADTRG}}$ | 8              | Input<br>Input<br>Input | Port A0 to A7: Pins used to input port.<br>Analog input 0 to 7: Pins used to input to AD converter.<br>AD trigger: Signal used to request AD start (PA3). |
| PZ2<br>$\overline{\text{HWR}}$                        | 1              | I/O<br>Output           | Port Z2: I/O port (with pull-up resistor)<br>High write: Strobe signal for writing data to pins D8 to D15   |
| PZ3   | 1              | I/O                     | Port Z3: I/O port (with pull-up resistor)   |



Table 2.2.3 Pin Names and Functions (3/3)

| Pin Names  | Number of Pins | I/O    | Functions   |
|------------|----------------|--------|---|
| BOOT       | 1              | Input  | This pin sets boot mode (with pull-up resistor)   |
| NMI        | 1              | Input  | Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge level or with both edge levels programmable                                |
| AM0 to AM1 | 2              | Input  | Operation mode:<br>AM1 = 0 and AM0 = 1: External 16-bit bus is fixed<br>or external 8-/16-bit buses are mixed.<br>AM1 = 0 and AM0 = 0: External 8-bit bus is fixed. |
| RESET      | 1              | Input  | Reset: Initializes TMP91C630F (with pull-up resistor)   |
| VREFH      | 1              | Input  | Pin for reference voltage input to AD converter (H)   |
| VREFL      | 1              | Input  | Pin for reference voltage input to AD converter (L)   |
| AVCC       | 1              | I/O    | Power supply pin for AD converter   |
| AVSS       | 1              |        | GND supply pin for AD converter   |
| X1/X2      | 2              |        | Oscillator connection pins  |
| DVCC       | 4              |        | Power supply pins   |
| DVSS       | 4              |        | GND pins (0 V)  |
| EMU0       | 1              | Output | Open pin  |
| EMU1       | 1              | Output | Open pin  |

Note 1: An external DMA controller cannot access the device's built-in memory or built-in I/O devices using the  $\overline{\text{BUSRQ}}$  and  $\overline{\text{BUSAk}}$  signals.

### 3. Operation

This section describes the basic components, functions and operation of the TMP91C630.

Notes and restrictions which apply to the various items described here are outlined in section 7. Precautions and restrictions at the end of this databook.

#### 3.1 CPU

The TMP91C630 incorporates a high-performance 16-bit CPU (the 900/L1 CPU). For a description of this CPU's operation, please refer to the section of this databook which describes the TLCS-900/L1 CPU.

The following sub-sections describe functions peculiar to the CPU used in the TMP91C630; these functions are not covered in the section devoted to the TLCS-900/L1 CPU.

##### 3.1.1 Reset

When resetting the TMP91C630 microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then set the  $\overline{\text{RESET}}$  input to Low level at least for 10 system clocks (8.89  $\mu\text{s}$  at 36 MHz).

Thus, when turn on the switch, be set to the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the  $\overline{\text{RESET}}$  input to Low level at least for 10 system clocks.

Clock gear is initialized 1/16 mode by Reset operation. It means that the system clock mode  $f_{\text{SYS}}$  is set to  $f_c/32$  ( $= f_c/16 \times 1/2$ ).

When the reset has been accepted, the CPU performs the following:

- Sets the program counter (PC) as follows in accordance with the reset vector stored at address FFFF00H to FFFF02H:  
 $\text{PC}\langle 0:7 \rangle \leftarrow \text{Data in location FFFF00H}$   
 $\text{PC}\langle 8:15 \rangle \leftarrow \text{Data in location FFFF01H}$   
 $\text{PC}\langle 16:23 \rangle \leftarrow \text{Data in location FFFF02H}$
- Sets the stack pointer (XSP) to 100H.
- Sets bits  $\langle \text{IFF0:IFF2} \rangle$  of the status register (SR) to 111 (thereby setting the interrupt level mask register to level 7).
- Sets the  $\langle \text{MAX} \rangle$  bit of the status register to 1 (MAX mode).  
 (Note: As this product does not support MIN mode, do not program a 0 to the  $\langle \text{MAX} \rangle$  bit.)
- Clears bits  $\langle \text{RFP0:RFP2} \rangle$  of the status register to 000 (thereby selecting register bank 0).

When the reset is cleared, the CPU starts executing instructions according to the program counter settings. CPU internal registers not mentioned above do not change when the reset is cleared.

When the reset is accepted, the CPU sets internal I/O, ports and other pins as follows.

- Initializes the internal I/O registers.
- Sets the port pins, including the pins that also act as internal I/O, to general-purpose input or output port mode.

Note: The CPU internal register (except to PC, SR and XSP) and internal RAM data do not change by resetting.

Figure 3.1.1 shows the timing of a reset for the TMP91C630.

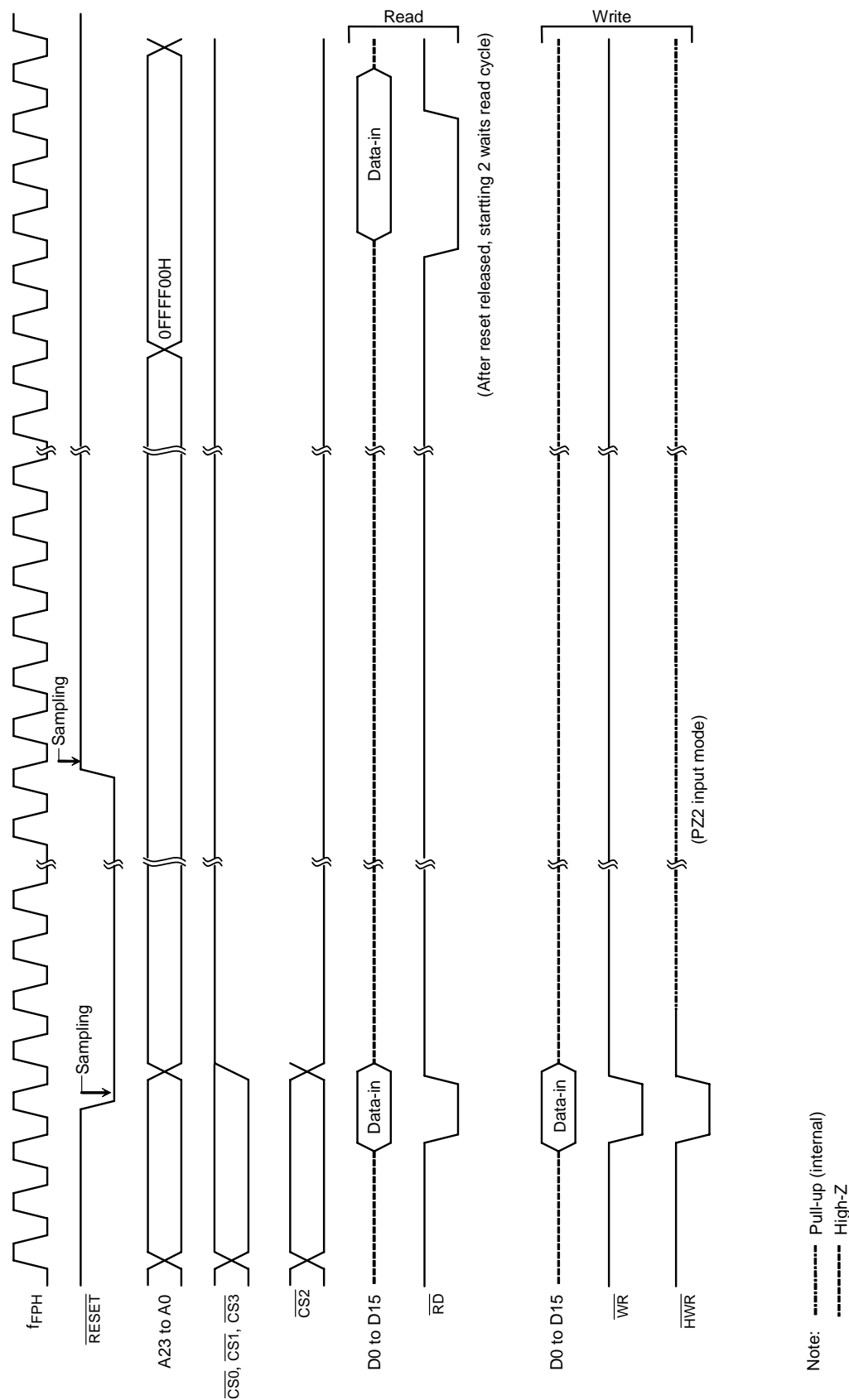


Figure 3.1.1 TMP91C630 Reset Timing Example

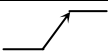
### 3.2 Outline of Operation Modes

There are multi-chip and multi-boot modes. Which mode is selected depends on the device's pin state after a reset.

- Multi-chip mode: The device normally operations in this mode. After a reset, the device starts executing the external memory program.
- Multi-boot mode: This mode is used to rewrite the external flash memory by serial transfer (UART).

After a reset, internal boot program starts up, executing an on-board rewrite program.

Table 3.2.1 Operation Mode Setup Table

| Operation Mode  | Mode Setup Input Pin  |                          |
|-----------------|---|--------------------------|
|                 | $\overline{\text{RESET}}$   | $\overline{\text{BOOT}}$ |
| Multi-chip mode |  | H                        |
| Multi-boot mode |   | L                        |

3.3 Memory Map

Figure 3.3.1 is a memory map of the TMP91C630.

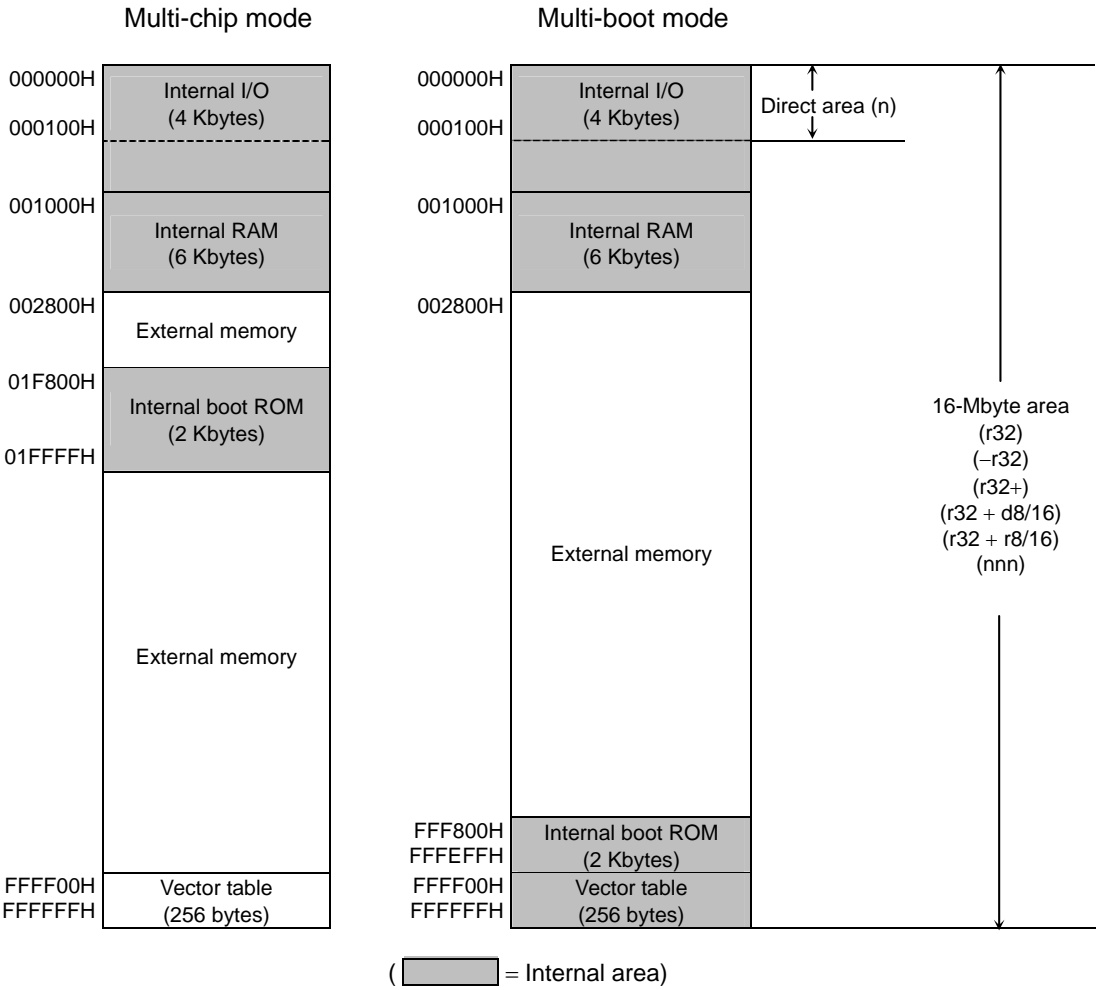


Figure 3.3.1 TMP91C630 Memory Map

## 4. Electrical Characteristics

### 4.1 Maximum Ratings

| Parameter                                 | Symbol           | Rating                        | Unit |
|---|------------------|-------------------------------|------|
| Power supply voltage                      | V <sub>CC</sub>  | −0.5 to 4.0                   | V    |
| Input voltage                             | V <sub>IN</sub>  | −0.5 to V <sub>CC</sub> + 0.5 | V    |
| Output current (per pin)                  | I <sub>OL</sub>  | 2                             | mA   |
| Output current (per pin)                  | I <sub>OH</sub>  | −2                            | mA   |
| Output current (total)                    | ΣI <sub>OL</sub> | 80                            | mA   |
| Output current (total)                    | ΣI <sub>OH</sub> | −80                           | mA   |
| Power dissipation (T <sub>a</sub> = 85°C) | PD               | 600                           | mW   |
| Soldering temperature (10 s)              | TSOLDER          | 260                           | °C   |
| Storage temperature                       | TSTG             | −65 to 150                    | °C   |
| Operating temperature                     | TOPR             | −40 to 85                     | °C   |

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

### 4.2 DC Characteristics (1/2)

| Parameter  |  | Symbol           | Condition                         | Min                   | Typ. (Note) | Max                   | Unit |
|--|--|------------------|-----------------------------------|-----------------------|-------------|-----------------------|------|
| Power supply voltage<br>(AVCC = DVCC)<br>(AVSS = DVSS = 0 V) |  | V <sub>CC</sub>  | f <sub>c</sub> = 10 MHz to 36 MHz | 2.7                   |             | 3.6                   | V    |
| Input Low Voltage  | D0 to D7, P10 to P17 (D8 to D15)   | V <sub>IL</sub>  | V <sub>CC</sub> = 2.7 V to 3.6 V  | −0.3                  |             | 0.6                   | V    |
|  | The other ports  | V <sub>IL1</sub> | V <sub>CC</sub> = 2.7 V to 3.6 V  |                       |             | 0.3 V <sub>CC</sub>   |      |
|  | RESET, NMI, BOOT<br>P56 (INT0), P70 (INT1)<br>P72 (INT2), P73 (INT3)<br>P75 (INT4), P90 (INT5) | V <sub>IL2</sub> | V <sub>CC</sub> = 2.7 V to 3.6 V  |                       |             | 0.25 V <sub>CC</sub>  |      |
|  | AM0, 1   | V <sub>IL3</sub> | V <sub>CC</sub> = 2.7 V to 3.6 V  |                       |             | 0.3                   |      |
|  | X1   | V <sub>IL4</sub> | V <sub>CC</sub> = 2.7 V to 3.6 V  |                       |             | 0.2 V <sub>CC</sub>   |      |
|  |  |                  |                                   |                       |             |                       |      |
| Input High Voltage   | D0 to D7, P10 to P17 (D8 to D15)   | V <sub>IH</sub>  | V <sub>CC</sub> = 2.7 V to 3.6 V  | 2.0                   |             | V <sub>CC</sub> + 0.3 | V    |
|  | The other ports  | V <sub>IH1</sub> | V <sub>CC</sub> = 2.7 V to 3.6 V  | 0.7 V <sub>CC</sub>   |             |                       |      |
|  | RESET, NMI, BOOT<br>P56 (INT0), P70 (INT1)<br>P72 (INT2), P73 (INT3)<br>P75 (INT4), P90 (INT5) | V <sub>IH2</sub> | V <sub>CC</sub> = 2.7 V to 3.6 V  | 0.75 V <sub>CC</sub>  |             |                       |      |
|  | AM0, 1   | V <sub>IH3</sub> | V <sub>CC</sub> = 2.7 V to 3.6 V  | V <sub>CC</sub> − 0.3 |             |                       |      |
|  | X1   | V <sub>IH4</sub> | V <sub>CC</sub> = 2.7 V to 3.6 V  | 0.8 V <sub>CC</sub>   |             |                       |      |
|  |  |                  |                                   |                       |             |                       |      |
| Output low voltage   |  | V <sub>OL</sub>  | I <sub>OL</sub> = 1.6 mA          |                       |             | 0.45                  | V    |
| Output high voltage  |  | V <sub>OH</sub>  | I <sub>OH</sub> = −400 μA         | 2.4                   |             |                       |      |

Note: Typical measurement Condition is T<sub>a</sub> = 25°C, V<sub>CC</sub> = 3.0 V unless otherwise noted.

## DC Characteristics (2/2)

| Parameter   | Symbol | Min | Typ.<br>(Note 1) | Max | Condition  | Unit |
|---|--------|-----|------------------|-----|--|------|
| Input leakage current   | ILI    |     | 0.02             | ±5  | $0.0 \leq V_{IN} \leq V_{CC}$  | μA   |
| Output leakage current  | ILO    |     | 0.05             | ±10 | $0.2 \leq V_{IN} \leq V_{CC} - 0.2$                                  |      |
| Power down voltage<br>(at STOP, RAM back-up)  | VSTOP  | 2.0 |                  | 3.6 | $V_{IL2} = 0.2 V_{CC}$ ,<br>$V_{IH2} = 0.8 V_{CC}$                   | V    |
| $\overline{\text{RESET}}$ pull-up resistor  | RRST   | 80  |                  | 400 | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$                           | kΩ   |
| $\overline{\text{BOOT}}$ pull-up resistor   | RBT    | 80  |                  | 400 | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$                           | kΩ   |
| Pin capacitance   | CIO    |     |                  | 10  | $f_c = 1 \text{ MHz}$  | pF   |
| Schmitt width<br>$\overline{\text{RESET}}$ , $\overline{\text{NMI}}$ , $\overline{\text{BOOT}}$ , INT0 to 5 | VTH    | 0.4 | 1.0              |     | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$                           | V    |
| Programmable<br>pull-up resistor  | RKH    | 80  |                  | 400 | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$                           | kΩ   |
| NORMAL (Note 2): (Note 3)   | Icc    |     | 17               | 25  | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$<br>$f_c = 36 \text{ MHz}$ | mA   |
| IDLE2 (Note 3)  |        |     | 4                | 8   |  |      |
| IDLE1 (Note 3)  |        |     | 1.5              | 3.5 |  |      |
| STOP  |        |     | 0.1              | 10  | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$                           | μA   |

Note 1: Typical measurement condition is  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 3.0 \text{ V}$  unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL):

All functions operate; output pins are open and input pins are fixed.

Note 3: Power supply current from AVCC pin is included in power supply current (Icc) of DVCC pin.

### 4.3 AC Characteristics

(1)  $V_{CC} = 2.7$  to  $3.6$  V

| No. | Parameter   | Symbol     | Variable      |             | $f_{FPH} = 36$ MHz |       | Unit |
|-----|---|------------|---------------|-------------|--------------------|-------|------|
|     |   |            | Min           | Max         | Min                | Max   |      |
| 1   | $f_{FPH}$ period (= x)  | $t_{FPH}$  | 27.6          | 100         | 27.6               |       | ns   |
| 2   | A0 to A23 valid $\rightarrow \overline{RD} / \overline{WR}$ fall          | $t_{AC}$   | $x - 26$      |             | 1.6                |       | ns   |
| 3   | $\overline{RD}$ rise $\rightarrow$ A0 to A23 hold                         | $t_{CAR}$  | $0.5x - 13.8$ |             | 0.0                |       | ns   |
| 4   | $\overline{WR}$ rise $\rightarrow$ A0 to A23 hold                         | $t_{CAW}$  | $x - 13$      |             | 14.6               |       | ns   |
| 5   | A0 to A23 valid $\rightarrow$ D0 to D15 input                             | $t_{AD}$   |               | $3.5x - 40$ |                    | 56.6  | ns   |
| 6   | $\overline{RD}$ fall $\rightarrow$ D0 to D15 input                        | $t_{RD}$   |               | $2.5x - 34$ |                    | 35.0  | ns   |
| 7   | $\overline{RD}$ low width   | $t_{RR}$   | $2.5x - 25$   |             | 44.0               |       | ns   |
| 8   | $\overline{RD}$ rise $\rightarrow$ D0 to D15 hold                         | $t_{HR}$   | 0             |             | 0                  |       | ns   |
| 9   | $\overline{WR}$ low width   | $t_{WW}$   | $2.0x - 25$   |             | 30.2               |       | ns   |
| 10  | D0 to D15 valid $\rightarrow \overline{WR}$ rise                          | $t_{DW}$   | $1.5x - 35$   |             | 6.4                |       | ns   |
| 11  | $\overline{WR}$ rise $\rightarrow$ D0 to D15 hold<br>(1 + N) waits mode   | $t_{WD}$   | $x - 25$      |             | 2.6                |       | ns   |
| 12  | A0 to A23 valid $\rightarrow \overline{WAIT}$ input<br>(1 + N) waits mode | $t_{AW}$   |               | $3.5x - 60$ |                    | 36.6  | ns   |
| 13  | $\overline{RD} / \overline{WR}$ fall $\rightarrow \overline{WAIT}$ hold   | $t_{CW}$   | $2.5x + 0$    |             | 69.0               |       | ns   |
| 14  | A0 to A23 valid $\rightarrow$ PORT input                                  | $t_{APH}$  |               | $3.5x - 76$ |                    | 20.6  | ns   |
| 15  | A0 to A23 valid $\rightarrow$ PORT hold                                   | $t_{APH2}$ | $3.5x$        |             | 96.6               |       | ns   |
| 16  | A0 to A23 valid $\rightarrow$ PORT valid                                  | $t_{APO}$  |               | $3.5x + 60$ |                    | 156.6 | ns   |

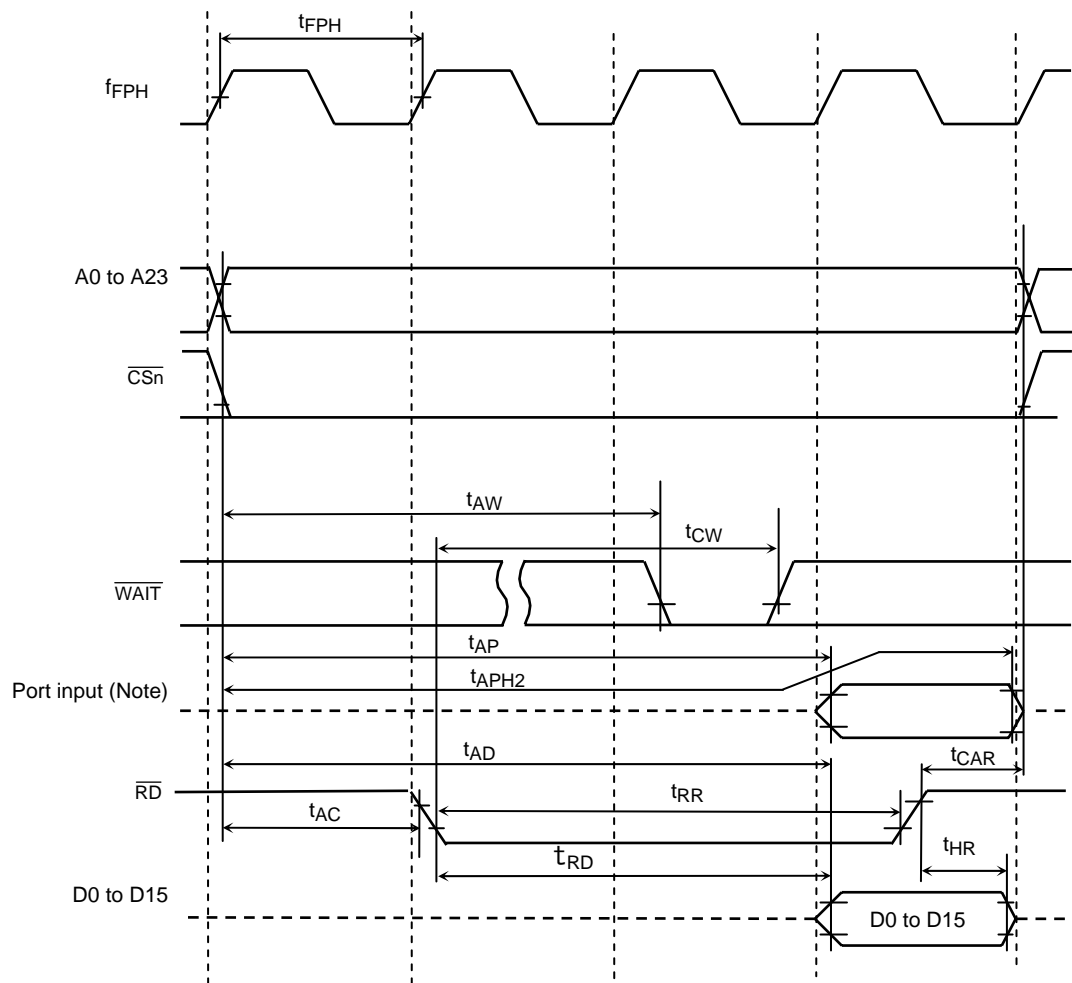
#### AC Measuring Conditions

- Output Level : High = 0.7 V<sub>CC</sub>, Low = 0.3 V<sub>CC</sub>, C<sub>L</sub> = 50 pF
- Input Level : High = 0.9 V<sub>CC</sub>, Low = 0.1V<sub>CC</sub>

Note: Symbol x in the above table means the period of clock  $f_{FPH}$ , it's half period of the system clock  $f_{SYS}$  for CPU core. The period of  $f_{FPH}$  depends on the clock gear setting.

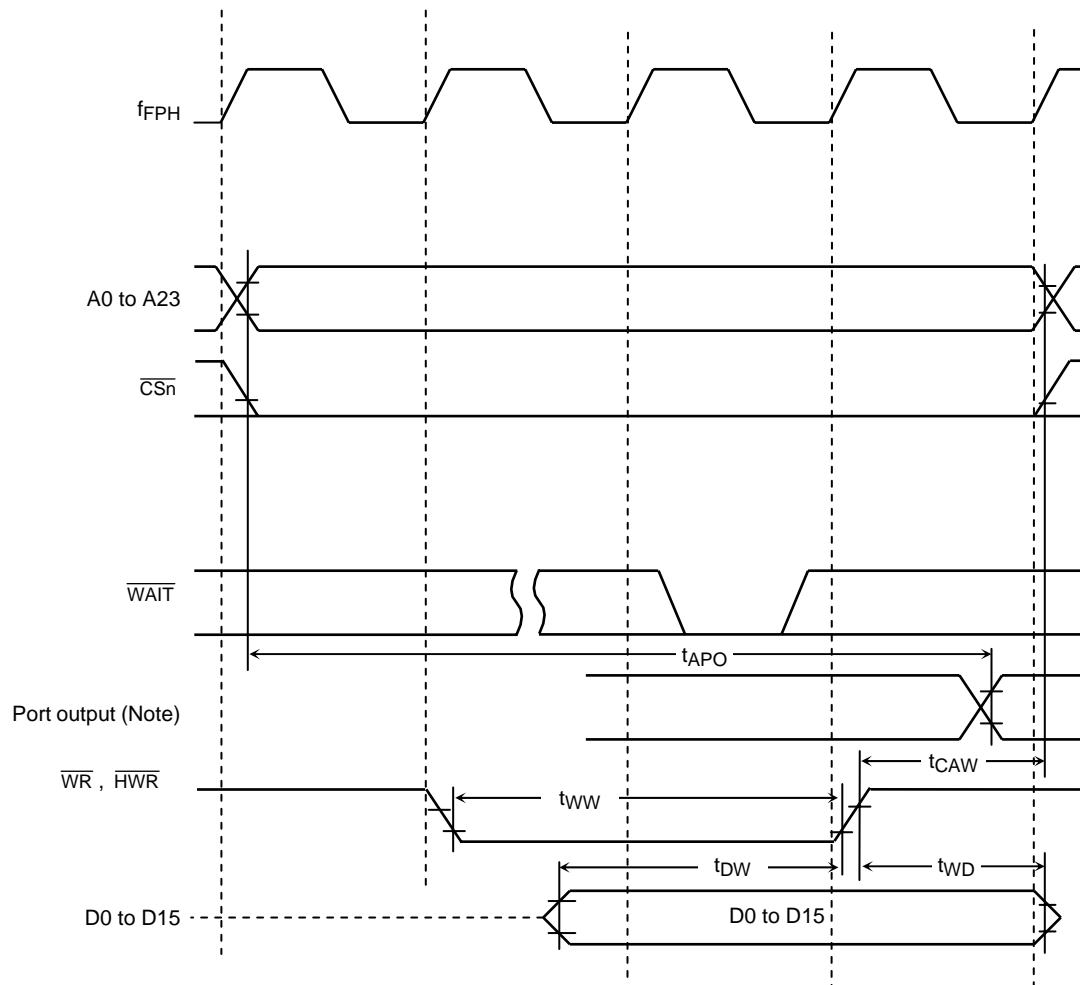


## (2) Read cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as  $\overline{RD}$  and  $\overline{CS}$  are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

## (3) Write cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as  $\overline{WR}$  and  $\overline{CS}$  are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

## 4.4 AD Conversion Characteristics

AVCC = DVCC, AVSS = DVSS

| Parameter   | Symbol               | Min                     | Typ.      | Max                     | Unit          |
|---|----------------------|-------------------------|-----------|-------------------------|---------------|
| Analog reference voltage (+)                                | VREFH                | $V_{CC} - 0.2\text{ V}$ | $V_{CC}$  | $V_{CC}$                | V             |
| Analog reference voltage (-)                                | VREFL                | $V_{SS}$                | $V_{SS}$  | $V_{SS} + 0.2\text{ V}$ |               |
| Analog input voltage range                                  | VAIN                 | $V_{REFL}$              |           | $V_{REFH}$              |               |
| Analog current for analog Reference voltage<br><VREFON> = 1 | IREF<br>(VREFL = 0V) |                         | 0.94      | 1.35                    | mA            |
| <VREFON> = 0  |                      |                         | 0.02      | 5.0                     | $\mu\text{A}$ |
| Error<br>(not including quantizing errors)                  | —                    |                         | $\pm 1.0$ | $\pm 4.0$               | LSB           |

Note 1:  $1\text{ LSB} = (V_{REFH} - V_{REFL})/1024\text{ [V]}$ Note 2: The value of  $I_{CC}$  includes the current which flows through the AVCC pin.

## 4.5 Serial Channel Timing (I/O Internal Mode)

Note: Symbol x in the below table means the period of clock  $f_{FPH}$ , it's half period of the system clock  $f_{SYS}$  for CPU core. The period of  $f_{FPH}$  depends on the clock gear setting.

### (1) SCLK input mode

| Parameter                                    | Symbol    | Variable              |               | 36 MHz (Note) |     | Unit    |
|--|-----------|-----------------------|---------------|---------------|-----|---------|
|  |           | Min                   | Max           | Min           | Max |         |
| SCLK period                                  | $t_{SCY}$ | 16X                   |               | 0.44          |     | $\mu s$ |
| Output data → SCLK rising/falling edge*      | $t_{OSS}$ | $t_{SCY}/2 - 4X - 85$ |               | 25            |     | ns      |
| SCLK rising/falling edge* → Output data hold | $t_{OHS}$ | $t_{SCY}/2 + 2X + 0$  |               | 276           |     | ns      |
| SCLK rising/falling edge* → Input data hold  | $t_{HSR}$ | $3X + 10$             |               | 92            |     | ns      |
| SCLK rising/falling edge* → Valid data input | $t_{SRD}$ |                       | $t_{SCY} - 0$ |               | 440 | ns      |
| Valid data input → SCLK rising/falling edge* | $t_{RDS}$ | 0                     |               | 0             |     | ns      |

\*) SCLK rising/falling edge: The rising edge is used in SCLK rising mode.  
The falling edge is used in SCLK falling mode.

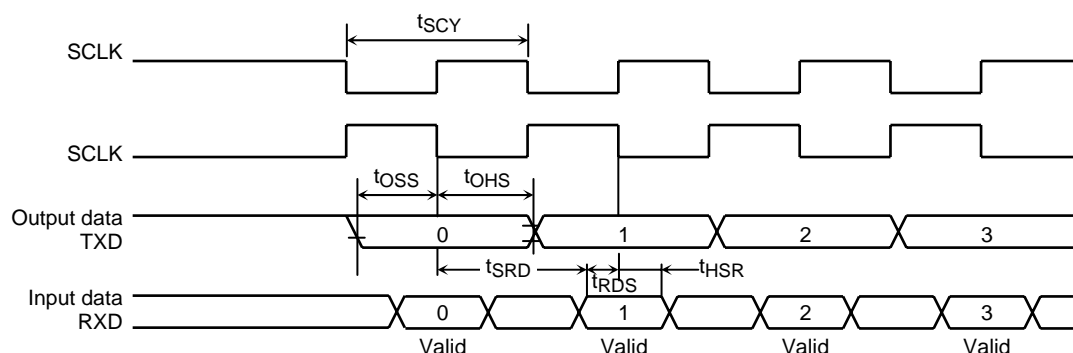
Note: at  $t_{SCY} = 16X$

### (2) SCLK output mode

| Parameter                                    | Symbol    | Variable         |                     | 36 MHz (Note) |     | Unit    |
|--|-----------|------------------|---------------------|---------------|-----|---------|
|  |           | Min              | Max                 | Min           | Max |         |
| SCLK period (programmable)                   | $t_{SCY}$ | 16X              | 8192X               | 0.44          |     | $\mu s$ |
| Output data → SCLK rising/falling edge*      | $t_{OSS}$ | $t_{SCY}/2 - 40$ |                     | 180           |     | ns      |
| SCLK rising/falling edge* → Output data hold | $t_{OHS}$ | $t_{SCY}/2 - 40$ |                     | 180           |     | ns      |
| SCLK rising/falling edge* → Input data hold  | $t_{HSR}$ | 0                |                     | 0             |     | ns      |
| SCLK rising/falling edge* → Valid data input | $t_{SRD}$ |                  | $t_{SCY} - 1X - 90$ |               | 324 | ns      |
| Valid data input → SCLK rising/falling edge* | $t_{RDS}$ | $1X + 90$        |                     | 117           |     | ns      |

\*) SCLK rising/falling edge: The rising edge is used in SCLK rising mode.  
The falling edge is used in SCLK falling mode.

Note: at  $t_{SCY} = 16X$



## 4.6 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1)

| Parameter              | Symbol            | Variable |     | 36 MHz |     | Unit |
|------------------------|-------------------|----------|-----|--------|-----|------|
|                        |                   | Min      | Max | Min    | Max |      |
| Clock period           | t <sub>VCK</sub>  | 8X + 100 |     | 320    |     | ns   |
| Clock low level width  | t <sub>VCKL</sub> | 4X + 40  |     | 150    |     | ns   |
| Clock high level width | t <sub>VCKH</sub> | 4X + 40  |     | 150    |     | ns   |

Note: Symbol x in the above table means the period of clock f<sub>FPH</sub>, it's half period of the system clock f<sub>SYS</sub> for CPU core. The period of f<sub>FPH</sub> depends on the clock gear setting.

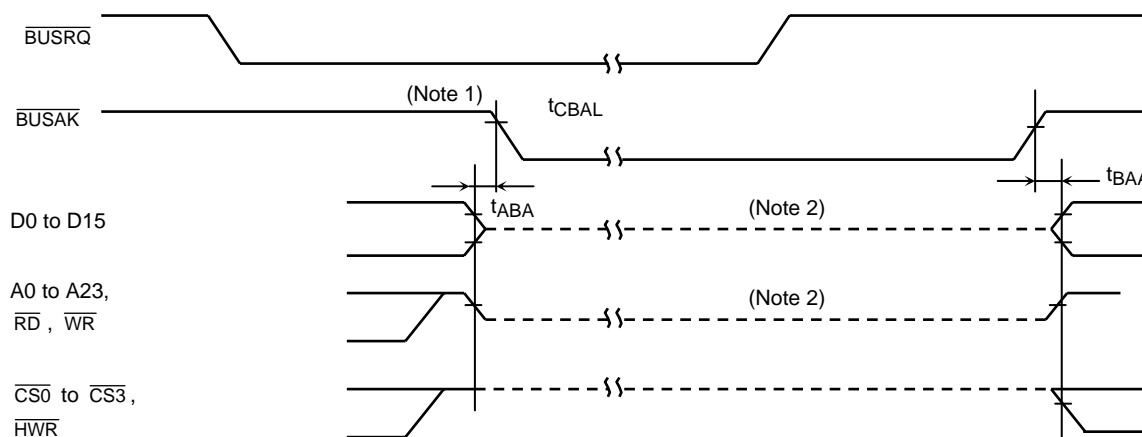
## 4.7 Interrupts

Note: Symbol x in the above table means the period of clock f<sub>FPH</sub>, it's half period of the system clock f<sub>SYS</sub> for CPU core. The period of f<sub>FPH</sub> depends on the clock gear setting.

(1)  $\overline{\text{NMI}}$ , INT0 to INT5 interrupts

| Parameter   | Symbol             | Variable |     | 36 MHz |     | Unit |
|---|--------------------|----------|-----|--------|-----|------|
|   |                    | Min      | Max | Min    | Max |      |
| $\overline{\text{NMI}}$ , INT0 to INT5 low level width  | t <sub>INTAL</sub> | 4X + 40  |     | 150    |     | ns   |
| $\overline{\text{NMI}}$ , INT0 to INT5 high level width | t <sub>INTAH</sub> | 4X + 40  |     | 150    |     | ns   |

## 4.8 Bus Request/Bus Acknowledge



| Parameter  | Symbol           | Variable |     | $f_{\text{FPH}} = 36 \text{ MHz}$ |     | Unit |
|--|------------------|----------|-----|-----------------------------------|-----|------|
|  |                  | Min      | Max | Min                               | Max |      |
| Output buffer to $\overline{\text{BUSAK}}$ low     | $t_{\text{ABA}}$ | 0        | 80  | 0                                 | 80  | ns   |
| $\overline{\text{BUSAK}}$ high to output buffer on | $t_{\text{BAA}}$ | 0        | 80  | 0                                 | 80  | ns   |

Note 1: Even if the  $\overline{\text{BUSRQ}}$  signal goes Low, the bus will not be released while the  $\overline{\text{WAIT}}$  signal is Low. The bus will only be released when  $\overline{\text{BUSRQ}}$  goes Low while  $\overline{\text{WAIT}}$  is High.

Note 2: This line shows only that the output buffer is in the Off state.

It does not indicate that the signal level is fixed.

Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary, since fixing of the level is delayed.

The internal programmable pull-up/pull-down resistor is switched between the Active and Non-Active states by the internal signal.