

**TYPES TIC226B, TIC226D
SILICON BIDIRECTIONAL TRIODE THYRISTORS**

8 A RMS • 200 V and 400 V

TRIACS

for

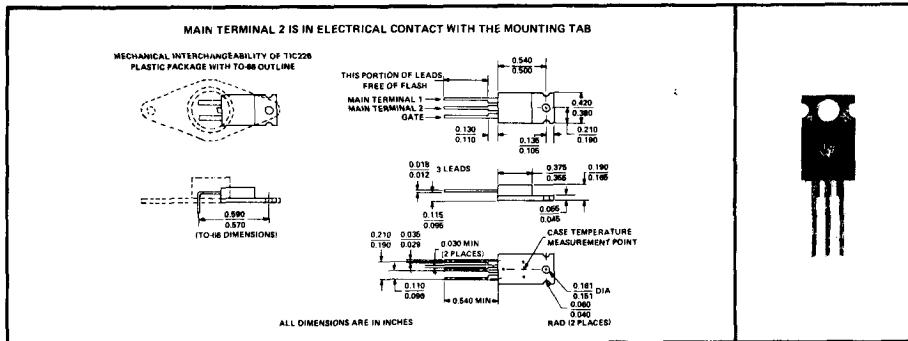
HIGH-TEMPERATURE, HIGH-CURRENT, and HIGH-VOLTAGE APPLICATIONS

- Typ dv/dt of 500 V/ μ s at 25°C

description

These devices are bidirectional triode thyristors (triacs) which may be triggered from the off-state to the on-state by either polarity of gate signal with Main Terminal 2 at either polarity.

mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted)¹

| | | | UNIT |
|---|---------|------------|------|
| Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1) | TIC226B | 200 | V |
| | TIC226D | 400 | |
| Full-Cycle RMS On-State Current at (or below) 85°C Case Temperature, $I_T(RMS)$ (See Note 2) | | 8 | A |
| Peak On-State Surge Current, Full-Sine-Wave, I_{TSM} (See Note 3) | | 70 | A |
| Peak On-State Surge Current, Half-Sine-Wave, I_{TSM} (See Note 4) | | 80 | A |
| Peak Gate Current, I_{GM} | | 1 | A |
| Peak Gate Power Dissipation, PGM , at (or below) 85°C Case Temperature (Pulse Width $\leq 200 \mu s$) | | 2.2 | W |
| Average Gate Power Dissipation, $PG(av)$, at (or below) 85°C Case Temperature (See Note 5) | | 0.9 | W |
| Operating Case Temperature Range | | -40 to 110 | °C |
| Storage Temperature Range | | -40 to 125 | °C |
| Lead Temperature 1/16 inch from Case for 10 Seconds | | 230 | °C |

NOTES: 1. These values apply bidirectionally for any value of resistance between the gate and Main Terminal 1.

2. This value applies for 50-Hz to 60-Hz full-sine-wave operation with resistive load. Above 85°C derate according to Figure 2.

3. This value applies for one 60-Hz full sine wave when the device is operating at (or below) the rated value of on-state current. Surge may be repeated after the device has returned to original thermal equilibrium. During the surge, gate control may be lost.

4. This value applies for one 60-Hz half sine wave when the device is operating at (or below) the rated value of on-state current. Surge may be repeated after the device has returned to original thermal equilibrium. During the surge, gate control may be lost.

5. This value applies for a maximum averaging time of 16.6 ms.

[†]All voltage values are with respect to Main Terminal 1.

TYPES TIC226B, TIC226D

SILICON BIDIRECTIONAL TRIODE THYRISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)[†]

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|--|------|---------|-----------|------------|
| I_{DRM} | Repetitive Peak Off-State Current | V_{DRM} = Rated V_{DRM} , $I_G = 0$ $T_C = 110^\circ C$ | | ± 2 | | mA |
| I_{GTM} Peak Gate Trigger Current | $V_{supply} = +12 V_T$, $R_L = 10 \Omega$, $t_{p(g)} \geq 20 \mu s$ | | 15 | 50 | | mA |
| | $V_{supply} = +12 V_T$, $R_L = 10 \Omega$, $t_{p(g)} \geq 20 \mu s$ | | -25 | -50 | | |
| | $V_{supply} = -12 V_T$, $R_L = 10 \Omega$, $t_{p(g)} \geq 20 \mu s$ | | -30 | -50 | | |
| | $V_{supply} = -12 V_T$, $R_L = 10 \Omega$, $t_{p(g)} \geq 20 \mu s$ | | 75 | | | |
| V_{GTM} Peak Gate Trigger Voltage | $V_{supply} = +12 V_T$, $R_L = 10 \Omega$, $t_{p(g)} \geq 20 \mu s$ | | 0.9 | 2.5 | | V |
| | $V_{supply} = +12 V_T$, $R_L = 10 \Omega$, $t_{p(g)} \geq 20 \mu s$ | | -1.2 | -2.5 | | |
| | $V_{supply} = -12 V_T$, $R_L = 10 \Omega$, $t_{p(g)} \geq 20 \mu s$ | | -1.2 | -2.5 | | |
| | $V_{supply} = -12 V_T$, $R_L = 10 \Omega$, $t_{p(g)} \geq 20 \mu s$ | | 1.2 | | | |
| V_{TM} | Peak On-State Voltage | $I_{TM} = \pm 12 A$, $I_G = 100 mA$, See Note 6 | | | ± 2.1 | V |
| I_H Holding Current | $V_{supply} = +12 V_T$, $I_G = 0$, Initiating $I_{TM} = 500 mA$ | | 20 | 60 | | mA |
| | $V_{supply} = -12 V_T$, $I_G = 0$, Initiating $I_{TM} = -500 mA$ | | -30 | -60 | | |
| I_L Latching Current | $V_{supply} = +12 V_T$, See Note 7 | | 30 | 70 | | mA |
| | $V_{supply} = -12 V_T$, See Note 7 | | -40 | -70 | | |
| dv/dt | Critical Rate of Rise of Off-State Voltage | V_{DRM} = Rated V_{DRM} , $I_G = 0$, $T_C = 110^\circ C$ | | 500 | | V/ μs |
| dv/dt | Critical Rate of Rise of Commutation Voltage | V_{DRM} = Rated V_{DRM} , $I_{TRM} = \pm 12 A$, $T_C = 85^\circ C$, See Figure 3 | | 5 | | V/ μs |

[†]All voltage values are with respect to Main Terminal 1.

NOTES: 6. This parameter must be measured using pulse techniques. $t_W \leq 1 \text{ ms}$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

7. The triacs are triggered by a 15-V (open-circuit amplitude) pulse supplied by a generator with the following characteristics: $R_G = 100 \Omega$, $t_W = 20 \mu s$, $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $f = 1 \text{ kHz}$.

thermal characteristics

| PARAMETER | MAX | UNIT |
|---|------|------|
| $R_{\theta JC}$ Junction-to-Case Thermal Resistance | 1.8 | °C/W |
| $R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance | 62.5 | °C/W |

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PARAMETER MEASUREMENT INFORMATION

The rate of rise of commutation voltage is defined as the slope of the line connecting the 10% and 63% test voltage points.

The critical rate of rise of commutation voltage is the rate above which the device will not sustain the off-state following conduction but will conduct current in the opposite direction in the absence of a gate-trigger signal. While this failure to switch to the off-state is not detrimental to the thyristor, it does result in loss of control of power to the load.

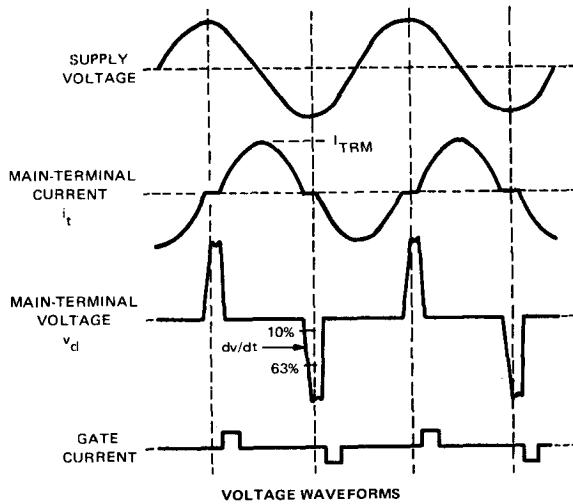
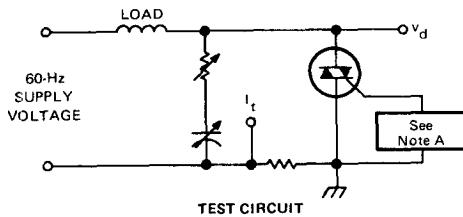


FIGURE 1-COMMUTATING dv/dt

NOTE A: The gate-current pulse is furnished by a trigger circuit which presents essentially an open circuit between pulses. The pulse is timed so that the off-state-voltage duration is approximately 800 μ s.

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THERMAL INFORMATION

MAXIMUM RMS ON-STATE CURRENT VS CASE TEMPERATURE

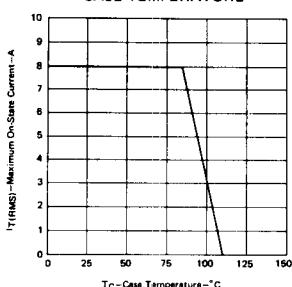


FIGURE 2
SURGE ON-STATE CURRENT
VS
CYCLES OF CURRENT DURATION

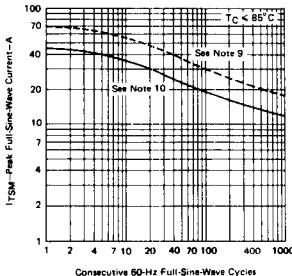


FIGURE 4

MAXIMUM AVERAGE POWER DISSIPATED VS RMS ON-STATE CURRENT

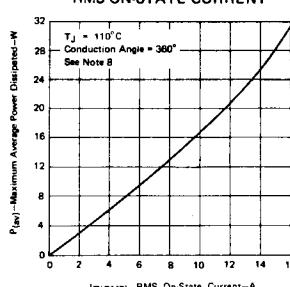


FIGURE 3

NOTES: 8. For operation at current greater than 8 amperes rms, see Figure 4.

9. The dashed curve shows the maximum number of cycles of surge current recommended for safe operation provided the device is initially operating at, or below, the rated value of on-state current; however, during the surge period, gate control of the device may be lost.
10. The solid curve shows the maximum number of cycles of surge current for which gate control is guaranteed provided the device is initially at nonoperating thermal equilibrium.

PEAK GATE TRIGGER CURRENT VS CASE TEMPERATURE

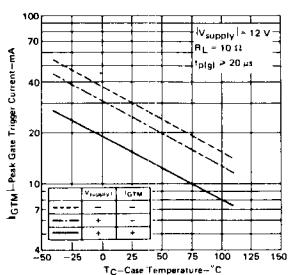


FIGURE 5

[†]The supply voltage is called positive when it causes Main Terminal 2 to be positive with respect to Main Terminal 1.

PEAK GATE TRIGGER VOLTAGE VS CASE TEMPERATURE

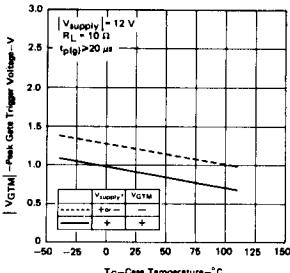


FIGURE 6

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| Typ | I_T (RMS) | V_{DRM} | I_{TSM} | I_{GT} max I, II, III mA | I_{GT} typ. IV mA |
|-----------|-------------|-----------|-----------|----------------------------------|---------------------------|
| type | A | V | A | | |
| TIC 226 B | 8 | 200 | 70 | 50 | 75 |
| TIC 226 D | 8 | 400 | 70 | 50 | 75 |

| V_{GT} max I, II, III V | V_{GT} max IV V | V_{TM} max V | @ | I_{TM} A | I_H max mA | Gehäuse package |
|---------------------------------|-------------------------|----------------------|---|---------------|--------------------|--------------------|
| 2,5 | | 2,1 | | 12 | 60 | TO-66P |
| 2,5 | | 2,1 | | 12 | 60 | TO-66P |