Technical Data
Advance Information

MSC8101/D
Rev. 9, 7/2003

Networking Digital Signal Processor

(mask sets 2K42A and 1K87M)

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The Motorola MSC8101 16-bit Digital Signal Processor (DSP) is the first member of the family of DSPs based on the StarCore SC140 DSP core. The MSC8101 is offered in three core speed levels: 250, 275, and 300 MHz.

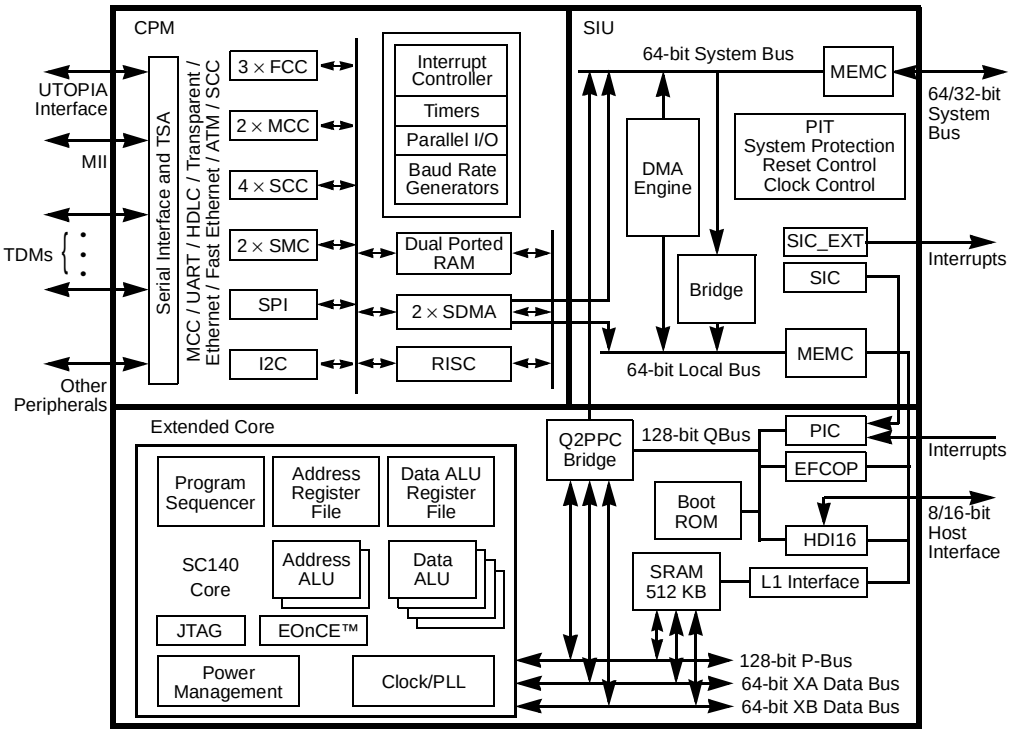

Figure 1. MSC8101 Block Diagram

What's New?

Rev. 9 includes the following changes:

- **Table 2A-16** and **Table 2B-16** note 1.
- **Table 2A-18** and **Table 2B-18**.
- Timing 510 in **Table 2A-21** and **Table 2B-21**.
- **Table 2B-2** for 300 MHz.
- **Table 2B-15** timings 12, 13, 15a, and 15b.
- **Table 3-1** several FCC1 signal designations

The Motorola MSC8101 DSP is a very versatile device that integrates the high-performance SC140 four-ALU (Arithmetic Logic Unit) DSP core along with 512 KB of on-chip memory, a Communications Processor Module (CPM), a 64-bit bus, a very flexible System Integration Unit (SIU), and a 16-channel DMA engine on a single device. With its four-ALU core, the MSC8101 can execute up to four multiply-accumulate (MAC) operations in a single clock cycle. The MSC8101 CPM is a 32-bit RISC-based communications protocol engine that can network to Time-Division Multiplexed (TDM) highways, Ethernet, and Asynchronous Transfer mode (ATM) backbones. The MSC8101 60x-compatible bus interface facilitates its connection to multi-master system architectures. The very large on-chip memory, 512 KB, reduces the need for off-chip program and data memories. The MSC8101 offers 1500 DSP MMACS (1200 core and 300 EFCOP) performance using an internal 300 MHz clock with a 1.6 V core and independent 3.3 V input/output (I/O). **Figure 1** shows a block diagram of the MSC8101 processor.

Note: This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Data Sheet Conventions

pin and pin-out	Although the device package does not have pins, the term pins and pin-out are used for convenience and indicate specific signal locations within the ball-grid array.
OVERBAR	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
“asserted”	Means that a high true (active high) signal is high or that a low true (active low) signal is low
“deasserted”	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

MSC8101 Features

- SC140 Core
  - Architecture optimized for efficient C/C++ code compilation
  - Four 16-bit ALUs and two 32-bit AGUs
  - 1200 DSP MMACS running at 300 MHz
  - Very low power dissipation—less than 0.25 W for the core running full speed at 1.6 V
  - Variable-Length Execution Set (VLES) execution model
  - JTAG/Enhanced OnCE debug port
- Communications Processor Module (CPM)
  - Programmable protocol machine using a 32-bit RISC engine
  - 155 Mbps ATM interface (including AAL 0/1/2/5)
  - 10/100 Mbit Ethernet interface
  - Up to four E1/T1 interfaces or one E3/T3 interface and one E1/T1 interface
  - HDLC support up to T3 rates, or 256 channels
- 64- or 32-bit Wide Bus Interface
  - Support for bursts for high efficiency
  - Glueless interface to 60x-compatible bus systems
  - Multi-master support
- Enhanced Filter Coprocessor (EFCOP)
  - Independently and concurrently executes long filters (such as echo cancellation)
  - Runs at 250/275/300 MHz and provides 250/275/300 MMACS performance
- Programmable Memory Controller
  - Control for up to eight banks of external memory
  - User-programmable machines (UPM) allowing glueless interface to various memory types (SRAM, DRAM, EPROM, and Flash memory) and other user-definable peripherals
  - Dedicated pipelined SDRAM memory interface
- Large On-Chip SRAM
  - 256K 16-bit words (512 KB)
  - Unified program and data space configurable by the application
  - Word and byte addressable
- DMA Controller
  - 16 DMA channels, FIFO based, with burst capabilities
  - Sophisticated addressing capabilities
- Small Foot Print Package
  - 17 mm × 17 mm lidded FC-PBGA package
- Very Low Power Consumption
  - Separate power supply for internal logic (1.6 V) and for I/O (3.3 V)
- Enhanced 16-bit Parallel Host Interface (HDI16)
  - Supports a variety of microcontroller, microprocessor, and DSP bus interfaces
- Phase-Lock Loops (PLLs)
  - System PLL
  - CPM DPLLs (SCC and SCM)
- Process Technology
  - Uses 0.13 micron copper interconnect process technology

Target Applications

The MSC8101 targets applications requiring very high performance, very large amounts of on-chip memory, and such networking capabilities as:

- Third-generation wideband wireless infrastructure systems
- Packet Telephony systems
- Multi-channel modem banks
- Multi-channel xDSL

Product Documentation

The documents listed in **Table 1** are required for a complete description of the MSC8101 and are necessary to design properly with the part. Documentation is available from the following sources (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

Table 1. MSC8101 Documentation

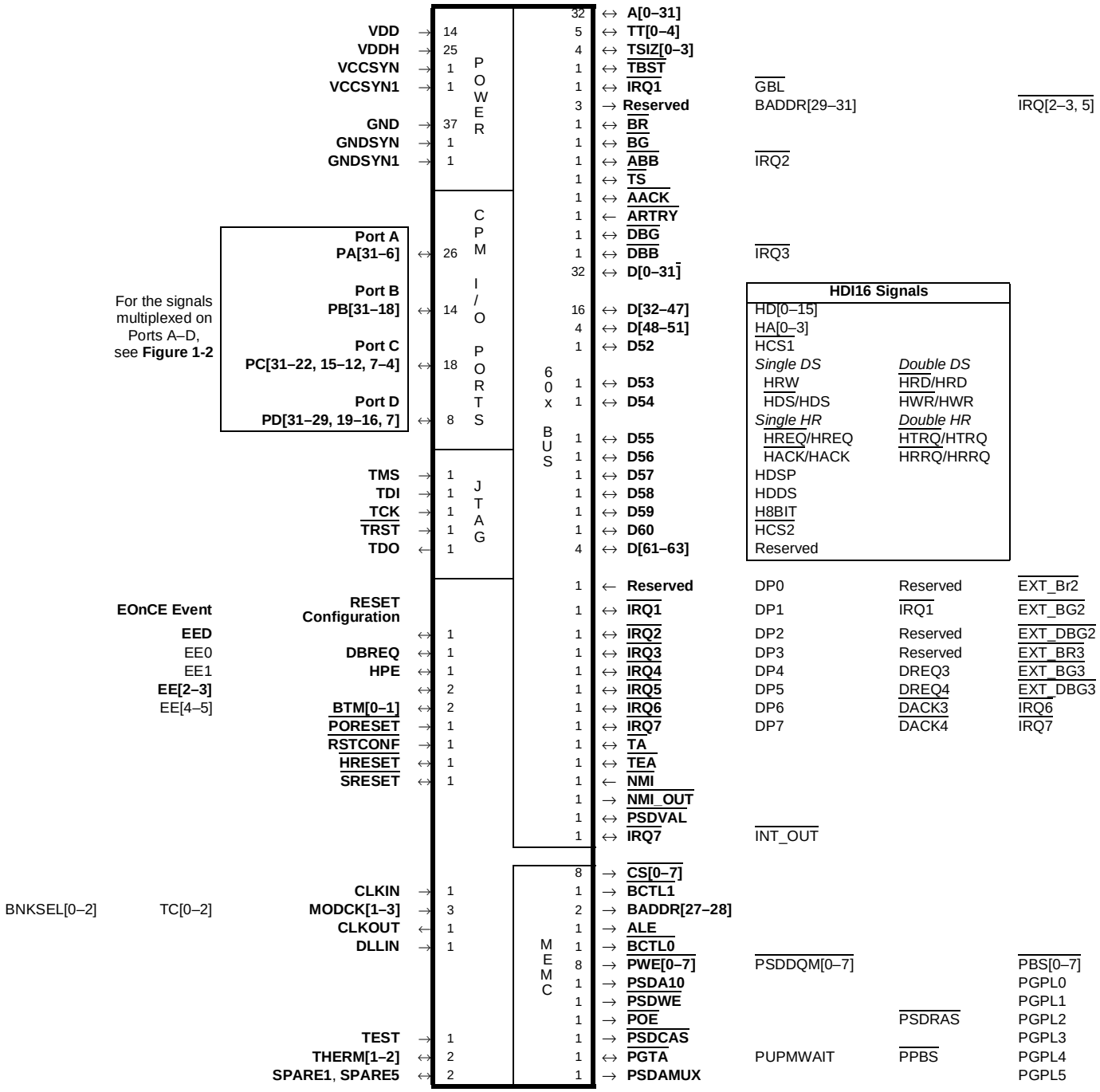
Name	Description	Order Number
MSC8101 Technical Data	MSC8101 features list and physical, electrical, timing, and package specifications	MSC8101/D
MSC8101 User's Guide	Detailed functional description of the MSC8101 memory configuration, operation, and register programming	MSC8101UG/D
MSC8101 Pocket Guide	Quick reference information for application development.	MSC8101PG/D
MSC8101 Reference Manual	Detailed description of the MSC8101 processor core and instruction set	MSC8101RM/D
SC140 DSP Core Reference Manual	Detailed description of the SC140 family processor core and instruction set	MNSC140CORE/D
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the MSC8101 product website

1.1 Signal Groupings

The MSC8101 external signals are organized into functional groups, as shown in **Table 1-1**, **Figure 1-1**, and **Figure 1-2**. **Table 1-1** lists the functional groups, the number of signal connections in each group, and references the table that gives a detailed listing of multiplexed signals within each group. **Figure 1-1** shows MSC8101 external signals organized by function. **Figure 1-2** indicates how the parallel input/output (I/O) ports signals are multiplexed. Because the parallel I/O design supported by the MSC8101 Communications Processor Module (CPM) is a subset of the parallel I/O signals supported by the MPC8260 device, port pins are not numbered sequentially.

Table 1-1. MSC8101 Functional Signal Groupings

Functional Group		Number of Signal Connections	Detailed Description
Power (V_{CC}, V_{DD}, and GND)		80	**Table 1-1** on page 1-4
Clock		6	**Table 1-2** on page 1-5
Reset, Configuration, and EOnCE		11	**Table 1-3** on page 1-6
System Bus, HDI16, and Interrupts		133	**Table 1-4** on page 1-8
Memory Controller		27	**Table 1-2** on page 1-16
Communications Processor Module (CPM) Input/Output Parallel Ports	Port A	26	**Table 1-3** on page 1-19
	Port B	14	**Table 1-4** on page 1-26
	Port C	18	**Table 1-5** on page 1-31
	Port D	8	**Table 1-6** on page 1-41
JTAG Test Access Port		5	**Table 1-7** on page 1-44
Reserved (denotes connections that are always reserved)		5	**Table 1-8** on page 1-45



Note: Refer to the *System Interface Unit (SIU)* chapter in the *MCS8101 Reference Manual* for details on how to configure these pins.

Figure 1-1. MSC8101 External Signals

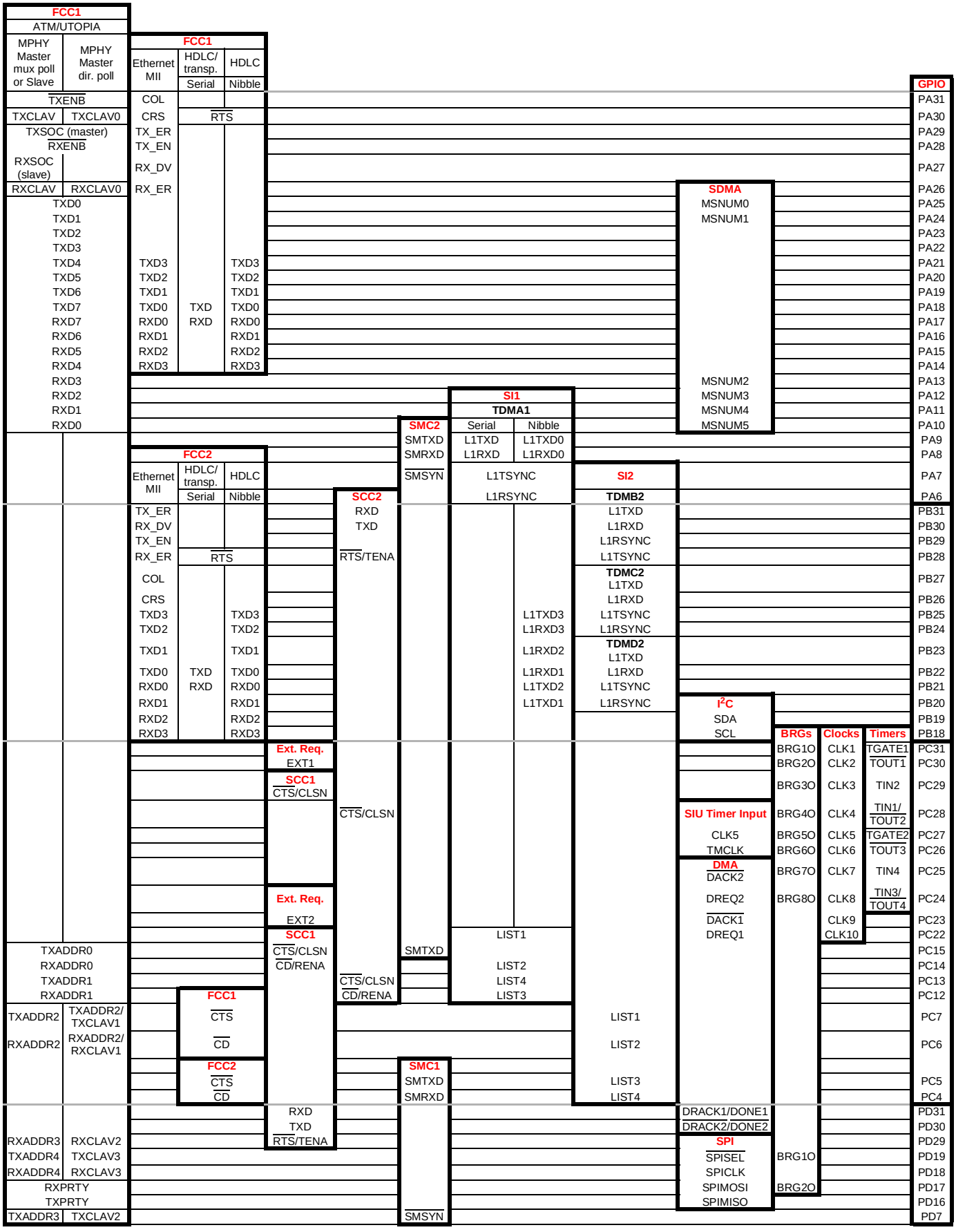


Figure 1-2. CPM Port A–D Pin Multiplexed Functionality

1.2 Power Signals

Table 1-1. Power and Ground Signal Inputs

Power Name	Description
V_{DD}	**Internal Logic Power** V_{DD} dedicated for use with the device core. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{DD} power rail.
V_{DDH}	**Input/Output Power** This source supplies power for the I/O buffers. The user must provide adequate external decoupling capacitors.
V_{CCSYN}	**System PLL Power** V_{CC} dedicated for use with the system Phase Lock Loop (PLL). The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
V_{CCSYN1}	**SC140 PLL Power** V_{CC} dedicated for use with the SC140 core PLL. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
GND	**System Ground** An isolated ground for the internal processing logic. This connection must be tied externally to all chip ground connections, except GND_{SYN} and GND_{SYN1}. The user must provide adequate external decoupling capacitors.
GND_{SYN}	**System PLL Ground** Ground dedicated for system PLL use. The connection should be provided with an extremely low-impedance path to ground.
GND_{SYN1}	**SC140 PLL Ground 1** Ground dedicated for SC140 core PLL use. The connection should be provided with an extremely low-impedance path to ground.

1.3 Clock Signals

Table 1-2. Clock Signals

Signal Name	Type	Signal Description
CLKIN	Input	**Clock In** Primary clock input to the MSC8101 PLL.
$\overline{\text{MODCK1}}$	Input	**Clock Mode Input 1** Defines the operating mode of internal clock circuits.
TC0	Output	**Transfer Code 0** Supplies information that can be useful for debugging bus transactions initiated by the MSC8101.
BNKSEL0	Output	**Bank Select 0** Selects the SDRAM bank when the MSC8101 is in 60x-compatible bus mode.
$\overline{\text{MODCK2}}$	Input	**Clock Mode Input 2** Defines the operating mode of internal clock circuits.
TC1	Output	**Transfer Code 1** Supplies information that can be useful for debugging bus transactions initiated by the MSC8101.
BNKSEL1	Output	**Bank Select 1** Selects the SDRAM bank when the MSC8101 is in 60x-compatible bus mode.
$\overline{\text{MODCK3}}$	Input	**Clock Mode Input 3** Defines the operating mode of internal clock circuits.
TC2	Output	**Transfer Code 2** Supplies information that can be useful for debugging bus transactions initiated by the MSC8101.
BNKSEL2	Output	**Bank Select 2** Selects the SDRAM bank when the MSC8101 is in 60x-compatible bus mode.
CLKOUT	Output	**Clock Out** The system bus clock.
DLLIN	Input	**DLLIN** Synchronizes with an external device.

1.4 Reset, Configuration, and EOnCE Event Signals

Table 1-3. Reset, Configuration, and EOnCE Event Signals

Signal Name	Type	Signal Description
DBREQ	Input	**Debug Request** Determines whether to go into SC140 Debug mode when $\overline{\text{PORESET}}$ is deasserted.
EE0[1]		**Enhanced OnCE (EOnCE) Event 0** After $\overline{\text{PORESET}}$ is deasserted, you can configure EE0 as an input (default) or an output.
	Input	Debug request, enable Address Event Detection Channel 0, or generate one of the EOnCE events.
	Output	Detection by Address Event Detection Channel 0. Used to trigger external debugging equipment.
HPE	Input	**Host Port Enable** When this pin is asserted during $\overline{\text{PORESET}}$, the Host port is enabled, the system data bus is 32 bits wide, and the Host *must* program the reset configuration word.
EE1[1]		**EOnCE Event 1** After $\overline{\text{PORESET}}$ is deasserted, you can configure EE1 as an input (default) or an output.
	Input	Enable Address Event Detection Channel 1 or generate one of the EOnCE events.
	Output	Debug Acknowledge or detection by Address Event Detection Channel 1. Used to trigger external debugging equipment.
EE2[1]		**EOnCE Event 2** After $\overline{\text{PORESET}}$ is deasserted, you can configure EE2 as an input (default) or an output.
	Input	Enable Address Event Detection Channel 2 or generate one of the EOnCE events or enable the Event Counter.
	Output	Detection by Address Event Detection Channel 2. Used to trigger external debugging equipment.
EE3[1]		**EOnCE Event 3** After $\overline{\text{PORESET}}$ is deasserted, you can configure EE3 as an input (default) or an output. See the *Emulation and Debug* chapter in the *SC140 DSP Core Reference Manual* for details on the ERCV Register.
	Input	Enable Address Event Detection Channel 3 or generate one of the EOnCE events.
	Output	EOnCE Receive Register (ERCV) was read by the DSP. Used to trigger external debugging equipment.

Table 1-3. Reset, Configuration, and EOnCE Event Signals (Continued)

Signal Name	Type	Signal Description
BTM[0–1]	Input	**Boot Mode 0–1** Determines the MSC8101 boot mode when $\overline{\text{PORESET}}$ is deasserted. See the *Emulation and Debug* chapter in the *SC140 DSP Core Reference Manual* for details on how to set these pins.
EE4[1]		**EOnCE Event 4** After $\overline{\text{PORESET}}$ is deasserted, you can configure EE4 as an input (default) or an output. See the *Emulation and Debug* chapter in the *SC140 DSP Core Reference Manual* for details on the ETRSMT Register.
	Input	Enable Address Event Detection Channel 4 or generate one of the EOnCE events
	Output	EOnCE Transmit Register (ETRSMT) was written by the DSP. Used to trigger external debugging equipment.
EE5[1]		**EOnCE Event 5** After $\overline{\text{PORESET}}$ is deasserted, you can configure EE5 as an input (default) or an output.
	Input	Enable Address Event Detection Channel 5.
	Output	Detection by Address Event Detection Channel 5. Used to trigger external debugging equipment.
EED[1]		**Enhanced OnCE (EOnCE) Event Detection** After $\overline{\text{PORESET}}$ is deasserted, you can configure EED as an input (default) or output:
	Input	Enable the Data Event Detection Channel.
	Output	Detection by the Data Event Detection Channel. Used to trigger external debugging equipment.
$\overline{\text{PORESET}}$	Input	**Power-On Reset** When asserted, this line causes the MSC8101 to enter power-on reset state.
$\overline{\text{RSTCONF}}$	Input	**Reset Configuration** Used during reset configuration sequence of the chip. A detailed explanation of its function is provided in the “Power-On Reset Flow” and “Hardware Reset Configuration” sections of the *MSC8101 Reference Manual*.
$\overline{\text{HRESET}}$	Input	**Hard Reset** When asserted, this open-drain line causes the MSC8101 to enter hard reset state.
$\overline{\text{SRESET}}$	Input	**Soft Reset** When asserted, this open-drain line causes the MSC8101 to enter soft reset state.

Note: See the *Emulation and Debug* chapter in the *SC140 DSP Core Reference Manual* for details on how to configure these pins.

1.5 System Bus, HDI16, and Interrupt Signals

The system bus, HDI16, and interrupt signals are grouped together because they use a common set of signal lines. Individual assignment of a signal to a specific signal line is configured through registers in the System Interface Unit (SIU) and the Host Interface (HDI16). Table 1-4 describes the signals in this group.

Note: To boot from the host interface, the HDI16 must be enabled by pulling up the HPE signal line during $\overline{\text{PORESET}}$. If the HPE signal is pulled up, the configuration word must then be loaded from the host. The configuration word must set the Internal Space Port Size bit in the Bus Control Register (BCR[ISPS]) to change the system data bus width from 64 bits to 32 bits and reassign the upper 32 bits to their HDI16 functions. Never set the Host Port Enable (HEN) bit in the Host Port Control Register (HPCR) to enable the HDI16, unless the bus size is first changed from 64 bits to 32 bits by setting the BCR[ISPS] bit. Otherwise, unpredictable operation may occur.

Although there are eight interrupt request (IRQ) connections to the core processor, there are multiple external lines that can connect to these internal signal lines. After reset, the default configuration includes two $\overline{\text{IRQ1}}$ and two $\overline{\text{IRQ7}}$ input lines. The designer must select one line for each required interrupt and reconfigure the other external signal line or lines for alternate functions.

Table 1-4. System Bus, HDI16, and Interrupt Signals

Signal	Data Flow	Description
A[0–31]	Input/Output	**Address Bus** When the MSC8101 is in external master bus mode, these pins function as the address bus. The MSC8101 drives the address of its internal bus masters and responds to addresses generated by external bus masters. When the MSC8101 is in Internal Master Bus mode, these pins are used as address lines connected to memory devices and are controlled by the MSC8101 memory controller.
TT[0–4]	Input/Output	**Bus Transfer Type** The bus master drives these pins during the address tenure to specify the type of transaction.
TSIZ[0–3]	Input/Output	**Transfer Size** The bus master drives these pins with a value indicating the number of bytes transferred in the current transaction.
$\overline{\text{TBST}}$	Input/Output	**Bus Transfer Burst** The bus master asserts this pin to indicate that the current transaction is a burst transaction (transfers four quad words).
$\overline{\text{IRQ1}}$	Input	**Interrupt Request 1**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{GBL}}$	Input/Output	**Global**[1] When a master within the chip initiates a bus transaction, it drives this pin. When an external master initiates a bus transaction, it should drive this pin. Assertion of this pin indicates that the transfer is global and it should be snooped by caches in the system.

Table 1-4. System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
Reserved	Output	The primary configuration is reserved.
BADDR29	Output	**Burst Address 29**[1] One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8101 memory controller.
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
Reserved	Output	The primary configuration is reserved.
BADDR30	Output	**Burst Address 30**[1] One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8101 memory controller.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
Reserved	Output	The primary configuration is reserved.
BADDR31	Output	**Burst Address 31**[1] One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8101 memory controller.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{BR}}$	Input/Output Output	**Bus Request**[2] An output when an external arbiter is used. The MSC8101 asserts this pin to request ownership of the bus.
	Input	An input when an internal arbiter is used. An external master should assert this pin to request bus ownership from the internal arbiter.
$\overline{\text{BG}}$	Input/Output Output	**Bus Grant**[2] An output when an internal arbiter is used. The MSC8101 asserts this pin to grant bus ownership to an external bus master.
	Input	An input when an external arbiter is used. The external arbiter should assert this pin to grant bus ownership to the MSC8101.
$\overline{\text{ABB}}$	Input/Output Output	**Address Bus Busy**[1] The MSC8101 asserts this pin for the duration of the address bus tenure. Following an address acknowledge ($\overline{\text{AACK}}$) signal, which terminates the address bus tenure, the MSC8101 deasserts $\overline{\text{ABB}}$ for a fraction of a bus cycle and then stops driving this pin.
	Input	The MSC8101 does not assume bus ownership as long as it senses that this pin is asserted by an external bus master.
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2**[1] One of the eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.

Table 1-4. System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
$\overline{\text{TS}}$	Input/Output	**Bus Transfer Start** Signals the beginning of a new address bus tenure. The MSC8101 asserts this signal when one of its internal bus masters (SC140 core or DMA) begins an address tenure. When the MSC8101 senses this pin being asserted by an external bus master, it responds to the address bus tenure as required (snoop if enabled, access internal MSC8101 resources, memory controller support).
$\overline{\text{AACK}}$	Input/Output	**Address Acknowledge** A bus slave asserts this signal to indicate that it identified the address tenure. Assertion of this signal terminates the address tenure.
$\overline{\text{ARTRY}}$	Input	**Address Retry** Assertion of this signal indicates that the bus transaction should be retried by the bus master. The MSC8101 asserts this signal to enforce data coherency with its internal cache and to prevent deadlock situations.
$\overline{\text{DBG}}$	Input/Output Output Input	**Data Bus Grant**[2] An output when an internal arbiter is used. The MSC8101 asserts this pin as an output to grant data bus ownership to an external bus master. An input when an external arbiter is used. The external arbiter should assert this pin as an input to grant data bus ownership to the MSC8101.
$\overline{\text{DBB}}$	Input/Output Output Input	**Data Bus Busy**[1] The MSC8101 asserts this pin as an output for the duration of the data bus tenure. Following a $\overline{\text{TA}}$, which terminates the data bus tenure, the MSC8101 deasserts $\overline{\text{DBB}}$ for a fraction of a bus cycle and then stops driving this pin. The MSC8101 does not assume data bus ownership as long as it senses $\overline{\text{DBB}}$ is asserted by an external bus master.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3**[1] One of the eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
D[0–31]	Input/Output	**Data Bus Most Significant Word** In write transactions the bus master drives the valid data on this bus. In read transactions the slave drives the valid data on this bus. In Host Port Disabled mode, these 32 bits are part of the 64-bit data bus. In Host Port Enabled mode, these bits are used as the bus in 32-bit mode.
D[32–47]	Input/Output	**Data Bus Bits 32–47** In write transactions the bus master drives the valid data on this bus. In read transactions the slave drives the valid data on this bus.
HD[0–15]	Input/Output	**Host Data**[2] When the HDI16 interface is enabled, these signals are lines 0-15 of the bidirectional tri-state data bus.
D[48–51]	Input/Output	**Data Bus Bits 48–51** In write transactions the bus master drives the valid data on these pins. In read transactions the slave drives the valid data on these pins.
HA[0–3]	Input	**Host Address Line 0–3**[3] When the HDI16 interface bus is enabled, these lines address internal host registers.

Table 1-4. System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
D52	Input/Output	**Data Bus Bit 52** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
$\overline{\text{HCS1}}$	Input	**Host Chip Select**[3] When the HDI16 interface is enabled, this is one of the two chip-select pins. The HDI16 chip select is a logical OR of $\overline{\text{HCS1}}$ and $\overline{\text{HCS2}}$.
D53	Input/Output	**Data Bus Bit 53** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
HRW	Input	**Host Read Write Select**[3] When the HDI16 interface is enabled in Single Strobe mode, this is the read/write input (HRW).
$\overline{\text{HRD}}$/HRD	Input	**Host Read Strobe**[3] When the HDI16 is programmed to interface with a double data strobe host bus, this pin is the read data strobe Schmitt trigger input ($\overline{\text{HRD}}$/HRD). The polarity of the data strobe is programmable.
D54	Input/Output	**Data Bus Bit 54** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
$\overline{\text{HDS}}$/HDS	Input	**Host Data Strobe**[3] When the HDI16 is programmed to interface with a single data strobe host bus, this pin is the data strobe Schmitt trigger input ($\overline{\text{HDS}}$/HDS). The polarity of the data strobe is programmable.
$\overline{\text{HWR}}$/HWR	Input	**Host Write Data Strobe**[3] When the HDI16 is programmed to interface with a double data strobe host bus, this pin is the write data strobe Schmitt trigger input ($\overline{\text{HWR}}$/HWR). The polarity of the data strobe is programmable.
D55	Input/Output	**Data Bus Bit 55** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
$\overline{\text{HREQ}}$/HREQ	Output	**Host Request**[3] When the HDI16 is programmed to interface with a single host request host bus, this pin is the host request output ($\overline{\text{HREQ}}$/HREQ). The polarity of the host request is programmable. The host request may be programmed as a driven or open-drain output.
$\overline{\text{HTRQ}}$/HTRQ	Output	**Transmit Host Request**[3] When the HDI16 is programmed to interface with a double host request host bus, this pin is the transmit host request output ($\overline{\text{HTRQ}}$/HTRQ). The signal can be programmed as driven or open drain. The polarity of the host request is programmable.

Table 1-4. System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
D56	Input/Output	**Data Bus Bit 56** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
$\overline{\text{HACK}}$/HACK	Output	**Host Acknowledge**[3] When the HDI16 is programmed to interface with a single host request host bus, this pin is the host acknowledge Schmitt trigger input (HACK). The polarity of the host acknowledge is programmable.
$\overline{\text{HRRQ}}$/HRRQ	Output	**Receive Host Request**[3] When the HDI16 is programmed to interface with a double host request host bus, this pin is the receive host request output ($\overline{\text{HRRQ}}$/HRRQ). The signal can be programmed as driven or open drain. The polarity of the host request is programmable.
D57	Input/Output	**Data Bus Bit 57** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
HDSP	Input	**Host Data Strobe Polarity**[3] When the HDI16 interface is enabled, this pin is the host data strobe polarity (HDSP).
D58	Input/Output	**Data Bus Bit 58** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
HDDS	Input	**Host Dual Data Strobe**[3] When the HDI16 interface is enabled, this pin is the host dual data strobe (HDDS).
D59	Input/Output	**Data Bus Bit 59** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
H8BIT	Input	**H8BIT**[3] When the HDI16 interface is enabled, this bit determines if the interface is in 8-bit or 16-bit mode.
D60	Input/Output	**Data Bus Bit 60** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
$\overline{\text{HCS2}}$	Input	**Host Chip Select** [3] When the HDI16 interface is enabled, this is one of the two chip-select pins. The HDI16 chip select is a logical OR of $\overline{\text{HCS1}}$ and $\overline{\text{HCS2}}$.
D[61–63]	Input/Output	**Data Bus Bits 61–63** Used only in 60x-mode-only mode. In write transactions the bus master drives the valid data on this bus. In read transactions the slave drives the valid data on this bus.
Reserved		These dedicated signals are reserved when the HDI16 is enabled.[3]

Table 1-4. System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
Reserved	Input	The primary configuration is reserved.
DP0	Input/Output	**Data Parity 0**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity zero pin should give odd parity (odd number of ones) on the group of signals that includes data parity 0 and D[0–7].
$\overline{\text{EXT\_BR2}}$	Input	**External Bus Request 2**[1,2] An external master asserts this pin to request bus ownership from the internal arbiter.
$\overline{\text{IRQ1}}$	Input	**Interrupt Request 1**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP1	Input/Output	**Data Parity 1**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity one pin should give odd parity (odd number of ones) on the group of signals that includes data parity 1 and D[8–15].
$\overline{\text{EXT\_BG2}}$	Output	**External Bus Grant 2**[1,2] The MSC8101 asserts this pin to grant bus ownership to an external bus master.
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP2	Input/Output	**Data Parity 2**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity two pin should give odd parity (odd number of ones) on the group of signals that includes data parity 2 and D[16–23].
$\overline{\text{EXT\_DBG2}}$	Output	**External Data Bus Grant 2**[1,2] The MSC8101 asserts this pin to grant data bus ownership to an external bus master.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP3	Input/Output	**Data Parity 3**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity three pin should give odd parity (odd number of ones) on the group of signals that includes data parity 3 and D[24–31].
$\overline{\text{EXT\_BR3}}$	Input	**External Bus Request 3**[1,2] An external master asserts this pin to request bus ownership from the internal arbiter.

Table 1-4. System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP4	Input/Output	**Data Parity 4**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity four pin should give odd parity (odd number of ones) on the group of signals that includes data parity 4 and D[32–39].
DREQ3	Input	**DMA Request 3**[1] An external peripheral uses this pin to request DMA service.
$\overline{\text{EXT\_BG3}}$	Output	**External Bus Grant 3**[1,2] The MSC8101 asserts this pin to grant bus ownership to an external bus master.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP5	Input/Output	**Data Parity 5**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity five pin should give odd parity (odd number of ones) on the group of signals that includes data parity 5 and D[40–47].
DREQ4	Input	**DMA Request 4**[1] An external peripheral uses this pin to request DMA service.
$\overline{\text{EXT\_DBG3}}$	Output	**External Data Bus Grant 3**[1,2] The MSC8101 asserts this pin to grant data bus ownership to an external bus master.
$\overline{\text{IRQ6}}$	Input	**Interrupt Request 6**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP6	Input/Output	**Data Parity 6**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity six pin should give odd parity (odd number of ones) on the group of signals that includes data parity 6 and D[48–55].
$\overline{\text{DACK3}}$	Output	**DMA Acknowledge 3**[1] The DMA drives this output to acknowledge the DMA transaction on the bus.
$\overline{\text{IRQ7}}$	Input	**Interrupt Request 7**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP7	Input/Output	**Data Parity 7**[1] The master or slave that drives the data bus also drives the data parity signals. The value driven on the data parity seven pin should give odd parity (odd number of ones) on the group of signals that includes data parity 7 and D[56–63].
$\overline{\text{DACK4}}$	Output	**DMA Acknowledge**[1] The DMA drives this output to acknowledge the DMA transaction on the bus.
$\overline{\text{TA}}$	Input/Output	**Transfer Acknowledge** Indicates that a data beat is valid on the data bus. For single beat transfers, assertion of $\overline{\text{TA}}$ indicates the termination of the transfer. For burst transfers, $\overline{\text{TA}}$ is asserted four times to indicate the transfer of four data beats with the last assertion indicating the termination of the burst transfer.

Table 1-4. System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
$\overline{\text{TEA}}$	Input/Output	**Transfer Error Acknowledge** Indicates a bus error. masters within the MSC8101 monitor the state of this pin. The MSC8101 internal bus monitor can assert this pin if it identifies a bus transfer that is hung.
$\overline{\text{NMI}}$	Input	**Non-Maskable Interrupt** When an external device asserts this line, the MSC8101 NMI input is asserted.
$\overline{\text{NMI\_OUT}}$	Output	**Non-Maskable Interrupt** Driven from the MSC8101 internal interrupt controller. Assertion of this output indicates that a non-maskable interrupt, pending in the MSC8101 internal interrupt controller, is waiting to be handled by an external host.
$\overline{\text{PSDVAL}}$	Input/Output	**Data Valid** Indicates that a data beat is valid on the data bus. The difference between the $\overline{\text{TA}}$ pin and $\overline{\text{PSDVAL}}$ is that the $\overline{\text{TA}}$ pin is asserted to indicate data transfer terminations while the $\overline{\text{PSDVAL}}$ signal is asserted with each data beat movement. Thus, when $\overline{\text{TA}}$ is asserted, $\overline{\text{PSDVAL}}$ is asserted, but when $\overline{\text{PSDVAL}}$ is asserted, $\overline{\text{TA}}$ is not necessarily asserted. For example when the SDMA initiates a double word (2x64 bits) transfer to a memory device that has a 32-bit port size, $\overline{\text{PSDVAL}}$ is asserted three times without $\overline{\text{TA}}$, and finally both pins are asserted to terminate the transfer.
$\overline{\text{IRQ7}}$	Input	**Interrupt Request 7**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{INT\_OUT}}$	Output	**Interrupt Output**[1] Driven from the MSC8101 internal interrupt controller. Assertion of this output indicates that an unmasked interrupt is pending in the MSC8101 internal interrupt controller.

Notes:
1. See the *System Interface Unit (SIU)* chapter in the *MCS8101 Reference Manual* for details on how to configure these pins.
2. When used as the bus control arbiter for the system bus, the MSC8101 can support up to three external bus masters. Each master uses its own set of Bus Request, Bus Grant, and Data Bus Grant signals ($\overline{\text{BR}}$/$\overline{\text{BG}}$/$\overline{\text{DBG}}$, EXT_$\overline{\text{BR2}}$/EXT_$\overline{\text{BG2}}$/EXT_$\overline{\text{DBG2}}$, and EXT_$\overline{\text{BR3}}$/EXT_$\overline{\text{BG3}}$/EXT_$\overline{\text{DBG3}}$). Each of these signal sets must be configured to indicate whether the external master is or is not a MSC8101 master device. See the Bus Configuration Register (BCR) description in the *System Interface Unit (SIU)* chapter in the *MCS8101 Reference Manual* for details on how to configure these pins. The second and third set of pins is defined by EXT_xxx to indicate that they can only be used with external master devices. The first set of pins ($\overline{\text{BR}}$/$\overline{\text{BG}}$/$\overline{\text{DBG}}$) have a dual function. When the MSC8101 is not the bus arbiter, these signals ($\overline{\text{BR}}$/$\overline{\text{BG}}$/$\overline{\text{DBG}}$) are used by the MSC8101 to obtain master control of the bus.
3. See the *Host Interface (HDI16)* chapter in the *MCS8101 Reference Manual* for details on how to configure these pins.

1.6 Memory Controller Signals

Refer to the *Memory Controller* chapter in the *MSC8101 Reference Manual (MSC8101RM/D)* for detailed information about configuring these signals.

Table 1-2. Memory Controller Signals

Signal	Data Flow	Description
$\overline{\text{CS}}$[0–7]	Output	**Chip Select** Enable specific memory devices or peripherals connected to MSC8101 buses.
$\overline{\text{BCTL1}}$	Output	**Buffer Control 1** Controls buffers on the data bus. Usually used with $\overline{\text{BCTL0}}$. The exact function of this pin is defined by the value of SIUMCR[BCTLC]. See the *System Interface Unit (SIU)* chapter in the *MS8101 Technical Reference* manual for details.
BADDR[27–28]	Output	**Burst Address 27–28** Two of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8101 memory controller.
ALE	Output	**Address Latch Enable** Controls the external address latch used in external master bus configuration.
$\overline{\text{BCTL0}}$	Output	**Buffer Control 0** Controls buffers on the data bus. The exact function of this pin is defined by the value of SIUMCR[BCTLC]. See the *System Interface Unit (SIU)* chapter in the *MS8101 Technical Reference* manual for details.
$\overline{\text{PWE}}$[0–7]	Output	**Bus Write Enable** Outputs of the bus General-Purpose Chip-select Machine (GPCM). These pins select byte lanes for write operations.
$\overline{\text{PSDDQM}}$[0–7]	Output	**Bus SDRAM DQM** Outputs of the SDRAM control machine. These pins select specific byte lanes of SDRAM devices.
$\overline{\text{PBS}}$[0–7]	Output	**Bus UPM Byte Select** Outputs of the User-Programmable Machine (UPM) in the memory controller. These pins select specific byte lanes during memory operations. The timing of these pins is programmed in the UPM. The actual driven value depends on the address and size of the transaction and the port size of the accessed device.
PSDA10	Output	**Bus SDRAM A10** Output from the bus SDRAM controller. This pin is part of the address when a row address is driven. It is part of the command when a column address is driven.
PGPL0	Output	**Bus UPM General-Purpose Line 0** One of six general-purpose output lines of the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{PSDWE}}$	Output	**Bus SDRAM Write Enable** Output from the bus SDRAM controller. This pin should connect to the SDRAM WE input signal.
PGPL1	Output	**Bus UPM General-Purpose Line 1** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.

Table 1-2. Memory Controller Signals (Continued)

Signal	Data Flow	Description
$\overline{\text{POE}}$	Output	**Bus Output Enable** Output of the bus GPCM. Controls the output buffer of memory devices during read operations.
$\overline{\text{PSDRAS}}$	Output	**Bus SDRAM RAS** Output from the bus SDRAM controller. This pin should connect to the SDRAM Row Address Strobe (RAS) input signal.
PGPL2	Output	**Bus UPM General-Purpose Line 2** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{PSDCAS}}$	Output	**Bus SDRAM CAS** Output from the bus SDRAM controller. This pin should connect to the SDRAM Column Address Strobe (CAS) input signal.
PGPL3	Output	**Bus UPM General-Purpose Line 3** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{PGTA}}$	Input	**GPCM TA** Terminates transactions during GPCM operation. Requires an external pull up resistor for proper operation.
PUPMWAIT	Input	**Bus UPM Wait** Input to the UPM. An external device can hold this pin high to force the UPM to wait until the device is ready for the operation to continue.
$\overline{\text{PPBS}}$	Output	**Bus Parity Byte Select** In systems in which data parity is stored in a separate chip, this output is the byte-select for that chip.
PGPL4	Output	**Bus UPM General-Purpose Line 4** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
PSDAMUX	Output	**Bus SDRAM Address Multiplexer** Controls the SDRAM address multiplexer when the MSC8101 is in External Master mode.
PGPL5	Output	**Bus UPM General-Purpose Line 5** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.

1.7 Communications Processor Module (CPM) Ports

The MSC8101 CPM supports a subset of signals included in the MPC8260. The following sections describe the functionality of the signals in the MSC8101.

- The MSC8101 CPM includes the following set of communication controllers:
- Two full-duplex Fast Serial Communications Controllers (FCCs) that support:
  - Asynchronous Transfer Mode (ATM) through a UTOPIA 8 interface (FCC1 only)—The MSC8101 can operate as one of the following:
    - UTOPIA slave device
    - UTOPIA multi-PHY master device using direct polling for up to 4 PHY devices
    - UTOPIA multi-PHY master device using multiplex polling that can address up to 31 PHY devices at addresses 0–30 (address 31 is reserved as a null port).
  - IEEE 802.3/Fast Ethernet through a Media-Independent Interface (MII)
  - High-Level Data Link Control (HDLC) Protocol:
    - Serial mode—Transfers data one bit at a time
    - Nibble mode—Transfers data four bits at a time
  - Transparent mode serial operation
- One FCC that operates with the TSA only
- Two Multi-Channel Controllers (MCCs) that together can handle up to 256 HDLC/transparent channels at 64 Kbps each, multiplexed on up to four TDM interfaces
- Two full-duplex serial communications controllers (SCCs) that support the following protocols:
  - IEEE 802.3/Fast Ethernet through a Media-Independent Interface (MII)
  - HDLC Protocol:
    - Serial mode—Transfers data one bit at a time
    - Nibble mode—Transfers data four bits at a time
  - Synchronous Data Link Control (SDLC)
  - LocalTalk (HDLC-based local area network protocol)
  - Universal Asynchronous Receiver/Transmitter (UART)
  - Synchronous UART (1x clock mode)
  - Binary Synchronous (BISYNC) communication
  - Transparent mode serial operation
- Two additional SCCs that operate with the TSA only
- Two full-duplex Serial Management Controllers (SMCs) that support the following protocols:
  - General Circuit Interface (GCI)/Integrated Services Digital Network (ISDN) monitor and C/I channels (TSA only)
  - UART
  - Transparent mode serial operation
- Serial Peripheral Interface (SPI) support for master or slave operation
- Inter-Integrated Circuit (I^2C) bus controller
- Time-Slot Assigner (TSA) that supports multiplexing from any of the SCCs, FCCs, SMCs, and two MCCs onto four time-division multiplexed (TDM) interfaces. The TSA uses two Serial Interfaces (SI1 and SI2). SI1 uses TDMA1 which supports both serial and nibble mode. SI2 does not support nibble mode and includes TDMB2, TDMC2, and TDMD2 which operate only in serial mode.

The individual sets of externals signals associated with a specific protocol and data transfer mode are multiplexed across any or all of the ports, as shown in **Figure 1-2**. The following sections provide detailed descriptions of the signals supported by Ports A–Port D.

1.7.1 Port A Signals

Table 1-3. Port A Signals

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA31	FCC1: TXENB *UTOPIA master*	Output	**FCC1: UTOPIA Master Transmit Enable** In the ATM UTOPIA interface supported by FCC1, TXENB is asserted by the MSC8101 (UTOPIA master PHY) when there is valid transmit cell data (TXD[0–7]).
	FCC1: TXENB *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Transmit Enable** In the ATM UTOPIA interface supported by FCC1, TXENB is asserted by an external UTOPIA master PHY when there is valid transmit cell data (TXD[0–7]).
	FCC1: COL *MII*	Input	**FCC1: Media Independent Interface Collision Detect** In the MII interface supported by FCC1, COL is asserted by an external fast Ethernet PHY.
PA30	FCC1: TXCLAV *UTOPIA slave*	Output	**FCC1: UTOPIA Slave Transmit Cell Available** In the ATM UTOPIA interface supported by FCC1, TXCLAV is asserted by the MSC8101 (UTOPIA slave PHY) when the MSC8101 can accept one complete ATM cell.
	FCC1: TXCLAV *UTOPIA master*, or	Input	**FCC1: UTOPIA Master Transmit Cell Available** In the ATM UTOPIA interface supported by FCC1, TXCLAV is asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell.
	FCC1: TXCLAV0 *UTOPIA master, Multi-PHY, direct polling*	Input	**FCC1: UTOPIA Master Transmit Cell Available Multi-PHY Direct Polling** In the ATM UTOPIA interface supported by FCC1, TXCLAV0 is asserted by an external UTOPIA slave PHY using direct polling to indicate that it can accept one complete ATM cell.
	FCC1: RTS *HDLC, Serial and Nibble*	Output	**FCC1: Request To Send** In the standard modem interface signals supported by FCC1 (RTS, CTS, and CD). RTS is asynchronous with the data. RTS is typically used in conjunction with CD. The MSC8101 FCC1 transmitter requests the receiver to send data by asserting RTS low. The request is accepted when CTS is returned low.
	FCC1: CRS *MII*	Input	**FCC1: Media Independent Interface Carrier Sense** In the MII interface supported by FCC1. CRS is asserted by an external fast Ethernet PHY. It indicates activity on the cable.
PA29	FCC1: TXSOC *UTOPIA master*	Output	**FCC1: UTOPIA Transmit Start of Cell** In the ATM UTOPIA interface supported by FCC1. TXSOC is asserted by the MSC8101 (UTOPIA master PHY) when TXD[0–7] contains the first valid byte of the cell.
	FCC1: TX_ER *MII*	Output	**FCC1: Media Independent Interface Transmit Error** In the MII interface supported by FCC1. TX_ER is asserted by the MSC8101 to force propagation of transmit errors.

Table 1-3. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA28	FCC1: RXENB *UTOPIA master*	Output	**FCC1: UTOPIA Master Receive Enable** In the ATM UTOPIA interface supported by FCC1. (UTOPIA master) RXENB is asserted by the MSC8101 (UTOPIA master PHY) to indicate that RXD[0–7] and RXSOC are to be sampled at the end of the next cycle. RXD[0–7] and RXSOC are enabled only in cycles following those with RXENB asserted.
	FCC1: RXENB *UTOPIA slave*	Input	**FCC1: UTOPIA Master Receive Enable** In the ATM UTOPIA interface supported by FCC1. (UTOPIA slave) RXENB is an input asserted by an external PHY to indicate that RXD[0–7] and RXSOC is to be sampled at the end of the next cycle. RXD[0–7] and RXSOC are enabled only in cycles following those with RXENB asserted.
	FCC1: TX_EN *MII*	Output	**FCC1: Media Independent Interface Transmit Enable** In the MII interface supported by FCC1. TX_EN is asserted by the MSC8101 when transmitting data.
PA27	FCC1: RXSOC *UTOPIA slave*	Output	**FCC1: UTOPIA Receive Start of Cell** Asserted by the MSC8101 (UTOPIA slave) for an external PHY when RXD[0–7] contains the first valid byte of the cell.
	FCC1: RX_DV *MII*	Input	**FCC1: Media Independent Interface Receive Data Valid** In the MII interface supported by FCC1. RX_DV is an input asserted by an external fast Ethernet PHY. RX_DV indicates that valid data is being sent. The presence of carrier sense but not RX_DV indicates reception of broken packet headers, probably due to bad wiring or a bad circuit.
PA26	FCC1: RXCLAV *UTOPIA slave*	Output	**FCC1: UTOPIA Slave Receive Cell Available** In the ATM UTOPIA interface supported by FCC1. RXCLAV is asserted by the MSC8101 (UTOPIA slave PHY) when one complete ATM cell is available for transfer.
	FCC1: RXCLAV *UTOPIA master, or*	Input	**FCC1: UTOPIA Master Receive Cell Available** In the ATM UTOPIA interface supported by FCC1. RXCLAV is asserted by an external PHY when one complete ATM cell is available for transfer.
	RXCLAV0 *UTOPIA master, Multi-PHY, direct polling*	Input	**FCC1: UTOPIA Master Receive Cell Available 0 Direct Polling** In the ATM UTOPIA interface supported by FCC1, RXCLAV0 is asserted by an external PHY when one complete ATM cell is available for transfer.
	FCC1: RX_ER *MII*	Input	**FCC1: Media Independent Interface Receive Error** In the MII interface and supported by FCC1. RX_ER is asserted by an external fast Ethernet PHY. This signal indicates a receive error, which often indicates bad wiring.

Table 1-3. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA25	FCC1: TXD0 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 0** In the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	SDMA: MSNUM0	Output	**Module Serial Number Bit 0** MSNUM[0–4] of is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates which section, transmit (0) or receive (1), is active during the transfer.
PA24	FCC1: TXD1 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 1** In the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	SDMA: MSNUM1	Output	**Module Serial Number Bit 1** MSNUM[0–4] of is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates which section, transmit (0) or receive (1), is active during the transfer.
PA23	FCC1: TXD2 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 2** TXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
PA22	FCC1: TXD3 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 3** TXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
PA21	FCC1: TXD4 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 4** TXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	FCC1: TXD3 *MII* and *HDLC nibble*	Output	**FCC1: MII and HDLC Nibble Transmit Data Bit 3** TXD[3–0] supports MII and HDLC nibble modes in FCC1. TXD3 is the most significant bit. TXD0 is the least significant bit.

Table 1-3. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA20	FCC1: TXD5 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 5** TXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	FCC1: TXD2 *MII* and *HDLC nibble*	Output	**FCC1: MII and HDLC Nibble Transmit Data Bit 2** TXD[3–0] is supported by MII and HDLC nibble modes in FCC1. TXD3 is the most significant bit. TXD0 is the least significant bit.
PA19	FCC1: TXD6 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 6** TXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	FCC1: TXD1 *MII* and *HDLC nibble*	Output	**FCC1: MII and HDLC Nibble Transmit Data Bit 1** TXD[3–0] is supported by MII and HDLC transparent nibble modes in FCC1. TXD3 is the most significant bit. TXD0 is the least significant bit.
PA18	FCC1: TXD7 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 7.** TXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	FCC1: TXD0 *MII* and *HDLC nibble*	Output	**FCC1: MII and HDLC Nibble Transmit Data Bit 0** TXD[3–0] is supported by MII and HDLC nibble modes in FCC1. TXD3 is the most significant bit. TXD0 is the least significant bit.
	FCC1: TXD *HDLC serial* and *transparent*	Output	**FCC1: HDLC Serial and Transparent Transmit Data Bit** The TXD serial bit is supported by HDLC serial and transparent modes in FCC1.
PA17	FCC1: RXD7 *UTOPIA*	Input	**FCC1: UTOPIA Receive Data Bit 7.** RXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when $\overline{\text{RXENB}}$ is asserted.
	FCC1: RXD0 *MII* and *HDLC nibble*	Input	**FCC1: MII and HDLC Nibble Receive Data Bit 0** RXD[3–0] is supported by MII and HDLC nibble mode in FCC1. RXD3 is the most significant bit. RXD0 is the least significant bit.
	FCC1: RXD *HDLC serial* and *transparent*	Input	**FCC1: HDLC Serial and Transparent Receive Data Bit** The RXD serial bit is supported by HDLC and transparent by FCC1.

Table 1-3. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA16	FCC1: RXD6 *UTOPIA*	Input	**FCC1: UTOPIA Receive Data Bit 6.** RXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when $\overline{\text{RXENB}}$ is asserted.
	FCC1: RXD1 *MII* and *HDLC nibble*	Input	**FCC1: MII and HDLC Nibble Receive Data Bit 1** RXD[3–0] is supported by MII and HDLC nibble mode in FCC1. RXD3 is the most significant bit. RXD0 is the least significant bit.
PA15	FCC1: RXD5 *UTOPIA*	Input	**FCC1: UTOPIA Receive Data Bit 5** In the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when $\overline{\text{RXENB}}$ is asserted.
	RXD2 *MII* and *HDLC nibble*	Input	**FCC1: MII and HDLC Nibble Receive Data Bit 2** RXD[3–0] is supported by MII and HDLC nibble mode in FCC1. RXD3 is the most significant bit. RXD0 is the least significant bit.
PA14	FCC1: RXD4 *UTOPIA*	Input	**FCC1: UTOPIA Receive Data Bit 4.** In the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when $\overline{\text{RXENB}}$ is asserted.
	FCC1: RXD3 *MII* and *HDLC nibble*	Input	**FCC1: MII and HDLC Nibble Receive Data Bit 3** RXD[3–0] is supported by MII and HDLC nibble mode in FCC1. RXD3 is the most significant bit. RXD0 is the least significant bit.
PA13	FCC1: RXD3 *UTOPIA*	Input	**FCC1: UTOPIA Receive Data Bit 3** In the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when $\overline{\text{RXENB}}$ is asserted.
	SDMA: MSNUM2	Output	**Module Serial Number Bit 2** MSNUM[0–4] is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates which section, transmit (0) or receive (1), is active during the transfer.

Table 1-3. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated Signal *Protocol*		
PA12	FCC1: RXD2 *UTOPIA*	Input	**FCC1: UTOPIA Receive Data Bit 2** In the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when $\overline{\text{RXENB}}$ is asserted.
	SDMA: MSNUM3	Output	**Module Serial Number Bit 3** MSNUM[0-4] of is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates which section, transmit (0) or receive (1), is active during the transfer.
PA11	FCC1: RXD1 *UTOPIA*	Input	**FCC1: UTOPIA RX Receive Data Bit 1** In the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when $\overline{\text{RXENB}}$ is asserted.
	SDMA: MSNUM4	Output	**Module Serial Number Bit 4** MSNUM[0–4] of is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates which section, transmit (0) or receive (1) is active during the transfer.
PA10	FCC1: RXD0 *UTOPIA*	Input	**FCC1: UTOPIA RX Receive Data Bit 0** In the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when $\overline{\text{RXENB}}$ is asserted.
	SDMA: MSNUM5	Output	**Module Serial Number Bit 5** MSNUM[0–4] of is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates which section, transmit (0) or receive (1), is active during the transfer.
PA9	SMC2: SMTXD	Output	**SMC2: Serial Management Transmit Data** Supported by SMC2. The SMC interface consists of SMTXD, SMRXD, $\overline{\text{SMSYN}}$, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI). See also PC15.
	SI1 TDMA1: L1TXD0 *TDM nibble*	Output	**Time-Division Multiplexing A1: Layer 1 Transmit Data Bit 0** In the TDMA1 interface supported by SI1. L1TXD3 is the most significant bit. L1TXD0 is the least significant bit in nibble mode. TDMA1 transmits nibble data out L1TXD[0–3].

Table 1-3. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA8	SMC2: SMRXD	Input	**SMC2: Serial Management Receive Data** Supported by SMC2. The SMC interface consists of SMTXD, SMRXD, $\overline{\text{SMSYN}}$, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI).
	SI1 TDMA1: L1RXD0 *TDM nibble*	Input	**Time-Division Multiplexing A1: Layer 1 Nibble Receive Data Bit 0** In the TDMA1 interface supported by SI1. L1RXD3 is the most significant bit. L1RXD0 is the least significant bit in nibble mode. TDMA1 receives nibble data from L1RXD[0–3].
	SI1 TDMA1: L1RXD *TDM serial*	Input	**Time-Division Multiplexing A1: Layer 1 Serial Receive Data** In the TDMA1 interface supported by SI1. TDMA1 receives serial data from L1RXD**.**
PA7	SMC2: $\overline{\text{SMSYN}}$	Input	**SMC2: Serial Management Synchronization** The SMC interface consists of SMTXD, SMRXD, $\overline{\text{SMSYN}}$, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI).
	SI1 TDMA1: L1TSYNC *TDM nibble* and *TDM serial*	Input	**Time-Division Multiplexing A1: Layer 1 Transmit Synchronization** In the TDMA1 interface supported by SI1, this is the synchronizing signal for the transmit channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8101 Technical Reference* manual.
PA6	SI1 TDMA1: L1RSYNC *TDM nibble* and *TDM serial*	Input	**Time-Division Multiplexing A1: Layer 1 Receive Synchronization.** In the TDMA1 interface supported by SI1, this is the synchronizing signal for the receive channel.

1.7.2 Port B Signals

Table 1-4. Port B Signals

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PB31	FCC2: TX_ER *MII*	Output	**FCC2: Media Independent Interface Transmit Error** In the MII interface supported by FCC2. TX_ER is asserted by the MSC8101 to force propagation of transmit errors.
	SCC2: RXD	Input	**SCC2: Receive Data** Supported by SCC2. SCC2 receives serial data from RXD.
	SI2 TDMB2: L1TXD *TDM serial*	Output	**Time-Division Multiplexing B2: Layer 1 Transmit Data** In the TDMB2 interface supported by SI2. L1TXD supports serial mode. TDMB2 transmits serial data out of L1TXD.
PB30	SCC2: TXD	Output	**SCC2: Transmit Data.** Supported by SCC2. SCC2 transmits serial data out of TXD.
	FCC2: RX_DV *MII*	Input	**FCC2: Media Independent Interface Receive Data Valid** In the MII interface supported by FCC2, RX_DV is asserted by an external fast Ethernet PHY. RX_DV indicates that valid data is being sent. The presence of carrier sense, but not RX_DV, indicates reception of broken packet headers, probably due to bad wiring or a bad circuit.
	SI2 TDMB2: L1RXD *TDM serial*	Input	**Time-Division Multiplexing B2: Layer 1 Receive Data** In the TDMB2 interface supported by SI2. L1RXD supports serial mode. TDMB2 receives serial data from L1RXD.
PB29	FCC2: TX_EN *MII*	Output	**FCC2: Media Independent Interface Transmit Enable** In the MII interface supported by FCC2. TX_EN is asserted by the MSC8101 when transmitting data.
	SI2 TDMB2: L1RSYNC *TDM serial*	Input	**Time-Division Multiplexing B2: Layer 1 Receive Synchronization** In the TDMB2 interface supported by SI2, this is the synchronizing signal for the receive channel.

Table 1-4. Port B Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PB28	FCC2: $\overline{\text{RTS}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Output	**FCC2: Request to Send** One of the standard modem interface signals supported by FCC2 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{RTS}}$ is asynchronous with the data. $\overline{\text{RTS}}$ is typically used in conjunction with $\overline{\text{CD}}$. The MSC8101 FCC2 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low.
	FCC2: RX_ER *MII*	Input	**FCC2: Media Independent Interface Receive Error** In the MII interface supported by FCC2, RX_ER is asserted by an external fast Ethernet PHY. This signal indicates a receive error, which often indicates bad wiring.
	SCC2: $\overline{\text{RTS}}$, TENA	Output	**SCC2: Request to Send, Transmit Enable** Typically used in conjunction with $\overline{\text{CD}}$ supported by SCC2. The MSC8101 SCC2 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low. TENA is the signal used in Ethernet mode.
	SI2 TDMB2: L1TSYNC *TDM serial*	Input	**Time-Division Multiplexing B2: Layer 1 Transmit Synchronization** In the TDMB2 interface supported by SI2, this is the synchronizing signal for the transmit channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8101 Technical Reference* manual.
PB27	FCC2: COL *MII*	Input	**FCC2: Media Independent Interface Collision Detect** In the MII interface supported by FCC2. COL is asserted by an external fast Ethernet PHY.
	SI2 TDMC2: L1TXD *TDM serial*	Output	**Time-Division Multiplexing C2: Layer 1 Transmit Data** In the TDMC2 interface supported by SI2. L1TXD supports serial mode. TDMC2 transmits serial data out of L1TXD.
PB26	FCC2: CRS *MII*	Input	**FCC2: Media Independent Interface Carrier Sense Input** In the MII interface, CRS is asserted by an external fast Ethernet PHY. This signal indicates activity on the cable.
	SI2 TDMC2: L1RXD *TDM serial*	Input	**Time-Division Multiplexing C2: Layer 1 Receive Data** In the TDMC2 interface supported by SI2. L1RXD supports serial mode. TDMC2 receives serial data from L1RXD.

Table 1-4. Port B Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PB25	FCC2: TXD3 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble Transmit Data Bit 3** Supported by MII and HDLC nibble mode in FCC2. TXD3 is the most significant bit. TXD0 is the least significant bit.
	SI1 TDMA1: L1TXD3 *TDM nibble*	Output	**Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 3** TDMA1 transmits nibble data out of L1TXD[0–3]. L1TXD3 is the most significant bit and L1TXD0 is the least significant bit in nibble mode.
	SI2 TDMC2: L1TSYNC *TDM serial*	Input	**Time-Division Multiplexing C2: Layer 1 Transmit Synchronization** In the TDMC2 interface supported by SI2, this is the synchronizing signal for the transmit channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8101 Technical Reference* manual.
PB24	FCC2: TXD2 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble: Transmit Data Bit 2** Supported by MII and HDLC nibble mode in FCC2. TXD3 is the most significant bit. TXD0 is the least significant bit.
	SI1 TDMA1: L1RXD3 *nibble*	Input	**Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 3** TDMA1 receives nibble data into L1RXD[0–3]. L1RXD3 is the most significant bit and L1RXD0 is the least significant bit in nibble mode.
	SI2 TDMC2: L1RSYNC *serial*	Input	**Time-Division Multiplexing C2: Layer 1 Receive Synchronization** In the TDMC2 interface supported by SI2, this is the synchronizing signal for the receive channel.
PB23	FCC2: TXD1 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble: Transmit Data Bit 1** Supported by MII and HDLC nibble mode in FCC2. TXD3 is the most significant bit. TXD0 is the least significant bit.
	SI1 TDMA1: L1RXD2 *TDM nibble*	Input	**Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 2** In the TDMA1 interface supported by SI1. TDMA1 supports bit and nibble modes. L1RXD3 is the most significant bit. L1RXD0 is the least significant bit in nibble mode. TDMA1 receives nibble data from L1RXD[0–3].
	SI2 TDMD2: L1TXD *TDM serial*	Output	**Time-Division Multiplexing D2: Layer 1 Transmit Data** In the TDMD2 interface supported by SI2. L1TXD supports serial mode. TDMA1 transmits serial data out of L1TXD.

Table 1-4. Port B Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PB22	FCC2: TXD0 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble Transmit Data Bit 0** TXD[0–3] is supported by MII and HDLC nibble mode in FCC2. TXD3 is the most significant bit. TXD0 is the least significant bit.
	FCC2: TXD *HDLC serial* and *transparent*	Output	**FCC2: HDLC Serial and Transparent Transmit Data** TXD is supported by HDLC serial mode and transparent mode in FCC2.
	SI1 TDMA1: L1RXD1 *TDM nibble*	Input	**Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 1** In the TDMA1 interface supported by SI1. TDMA1 supports bit and nibble modes. L1RXD3 is the most significant bit. L1RXD0 is the least significant bit in nibble mode. TDMA1 receives nibble data from L1RXD[0–3].
	SI2 TDMD2: L1RXD *TDM serial*	Input	**Time-Division Multiplexing D2: Layer 1 Receive Data** In the TDMD2 interface supported by SI2. TDMD2 supports serial mode. TDMD2 receives serial data from L1RXD.
PB21	FCC2: RXD0 *MII* and *HDLC nibble*	Input	**FCC2: MII and HDLC Nibble Receive Data Bit 0** RXD[0–3] is supported by MII and HDLC nibble mode in FCC2. RXD3 is the most significant bit. RXD0 is the least significant bit.
	FCC2: RXD *HDLC serial* and *transparent*	Input	**FCC2: HDLC Serial and Transparent Receive Data** Supported by HDLC serial mode and transparent mode in FCC2.
	SI1 TDMA1: L1TXD2 *TDM nibble*	Output	**Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 2** In the TDMA1 interface supported by SI1. TDMA1 supports bit and nibble modes. L1TXD3 is the most significant bit. L1TXD0 is the least significant bit in nibble mode. TDMA1 transmits nibble data out of L1TXD[0–3].
	SI2 TDMD2: L1TSYNC *TDM serial*	Input	**Time-Division Multiplexing D2: Layer 1 Transmit Synchronize Data** In the TDMD2 interface supported by SI2, this is the synchronizing signal for the transmit channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8101 Technical Reference* manual.

Table 1-4. Port B Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PB20	FCC2: RXD1 *MII* and *HDLC nibble*	Input	**FCC2: MII and HDLC Nibble: Receive Data Bit 1** RXD[0–3] is supported by MII and HDLC nibble mode in FCC2. RXD3 is the most significant bit. RXD0 is the least significant bit.
	SI1 TDMA1: L1TXD1 *TDM nibble*	Output	**Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 1** In the TDMA1 interface supported by SI1. TDMA1 supports bit and nibble modes. L1TXD3 is the most significant bit. L1TXD0 is the least significant bit in nibble mode. TDMA1 transmits nibble data out of L1TXD[0–3].
	SI2 TDMD2: L1RSYNC *TDM serial*	Input	**Time-Division Multiplexing D2: Layer 1 Receive Synchronize Data** In the TDMD2 interface supported by SI2, this is the synchronizing signal for the receive channel.
PB19	FCC2: RXD2 *MII* and *HDLC nibble*	Input	**FCC2: MII and HDLC Nibble Receive Data Bit 2** RXD[0–3] is supported by MII and HDLC nibble mode in FCC2. RXD3 is the most significant bit. RXD0 is the least significant bit.
	I^2C: SDA	Input/ Output	**I^2C: Inter-Integrated Circuit Serial Data** The I^2C interface comprises two signals: serial data (SDA) and serial clock (SDA). The I^2C controller uses a synchronous, multimaster bus that can connect several integrated circuits on a board. Clock rates run up to 520 kHz@25 MHz system clock.
PB18	FCC2: RXD3 *MII* and *HDLC nibble*	Input	**FCC2: MII and HDLC Nibble Receive Data Bit 3** RXD[0–3] is supported by MII and HDLC nibble mode in FCC2. RXD3 is the most significant bit. RXD0 is the least significant bit.
	I^2C: SCL	Input/ Output	**I^2C: Inter-Integrated Circuit Serial Clock** The I^2C interface comprises two signals: serial data (SDA) and serial clock (SDA). The I^2C controller uses a synchronous, multimaster bus that can connect several integrated circuits on a board. Clock rates run up to 520 kHz@25 MHz system clock.

1.7.3 Port C Signals

Table 1-5. Port C Signals

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC31	BRG1O	Output	**Baud-Rate Generator 1 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins. BRG1O can be the internal input to the SIU timers. When CLK5 is selected (see PC27 below), it is the source for BRG1O which is the default input for the SIU timers. See the *System Interface Unit (SIU)* chapter in the *MSC8101 Technical Reference* manual for additional information. If CLK5 is not enabled, BRG1O uses an internal input. If TMCLK is enabled (see PC26 below), the BRG1O input to the SIU timers is disabled.
	CLK1	Input	**Clock 1** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	TIMER1/2: $\overline{\text{TGATE1}}$	Input	**Timer 1/2: Timer Gate 1** The timers can be gated/restarted by an external gate signal. There are two gate signals: $\overline{\text{TGATE1}}$ controls timer 1 and/or 2 and $\overline{\text{TGATE2}}$ controls timer 3 and/or 4.
PC30	BRG2O	Output	**Baud-Rate Generator 2 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK2	Input	**Clock 2** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	Timer1: $\overline{\text{TOUT1}}$	Output	**Timer 1: Timer Out 1** The timers (Timer[1–4]) can output a signal on a timer output ($\overline{\text{TOUT}}$[1–4]) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also connect internally to the input of another timer, resulting in a 32-bit timer.
	EXT1	Input	**External Request 1** External request input line 1 asserts an internal request to the CPM processor. The signal can be programmed as level- or edge-sensitive, and also has programmable priority. Refer to the RISC Controller Configuration Register (RCCR) description in the Chapter 17 of the MSC8101 Reference Manual for programming information. There are no current microcode applications for this request line. It is reserved for future development.

Table 1-5. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC29	BRG3O	Output	**Baud-Rate Generator 3 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK3	Input	**Clock 3** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	TIN2	Input	**Timer Input 2** A timer can have one of the following sources: another timer, system clock, system clock divided by 16 or a timer input. The CPM supports up to 4 timer inputs. The timer inputs can be captured on the rising, falling or both edges.
	SCC1: $\overline{\text{CTS}}$, CLSN	Input	**SCC1: Clear to Send, Collision** Typically used in conjunction with $\overline{\text{RTS}}$. The MSC8101 SCC1 transmitter sends out a request to send data signal ($\overline{\text{RTS}}$). The request is accepted when $\overline{\text{CTS}}$ is returned low. CLSN is the signal used in Ethernet mode. See also PC15.
PC28	BRG4O	Output	**Baud-Rate Generator 4 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK4	Input	**Clock 4** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	TIN1	Input	**Timer Input 1** A timer can have one of the following sources: another timer, system clock, system clock divided by 16 or a timer input. The CPM supports up to 4 timer inputs. The timer inputs can be captured on the rising, falling or both edges.
	Timer2: $\overline{\text{TOUT2}}$	Output	**Timer 2: Timer Output 2** The timers (Timer[1–4]) can output a signal on a timer output ($\overline{\text{TOUT}}$[1–4]) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also be connected internally to the input of another timer, resulting in a 32-bit timer.
	SCC2: $\overline{\text{CTS}}$, CLSN	Input	**SCC2: Clear to Send, Collision** Typically used in conjunction with $\overline{\text{RTS}}$. The MSC8101 SCC2 transmitter sends out a request to send data signal ($\overline{\text{RTS}}$). The request is accepted when $\overline{\text{CTS}}$ is returned low. CLSN is the signal used in Ethernet mode. See also PC13.

Table 1-5. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC27	BRG5O	Output	**Baud-Rate Generator 5 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK5	Input	**Clock 5** When selected, CLK5 is a source for the SIU timers via BRG1O. See the *System Interface Unit (SIU)* chapter in the *MSC8101 Technical Reference* manual for additional information. If CLK5 is not enabled, BRG1O uses an internal input. If TMCLK is enabled (see PC26 below), the BRG1O input to the SIU timers is disabled.
	TIMER3/4: $\overline{\text{TGATE2}}$	Input	**Timer 3/4: Timer Gate 2** The timers can be gated/restarted by an external gate signal. There are two gate signals: $\overline{\text{TGATE1}}$ controls timer 1 and/or 2 and $\overline{\text{TGATE2}}$ controls timer 3 and/or 4.
PC26	BRG6O	Output	**Baud-Rate Generator 6 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK6	Input	**Clock 6** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	Timer3: $\overline{\text{TOUT3}}$	Output	**Timer 3: Timer Out 3** The timers (Timer[1–4]) can output a signal on a timer output ($\overline{\text{TOUT}}$[1–4]) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also connect internally to the input of another timer, resulting in a 32-bit timer.
	TMCLK	Input	**Timer Clock** When selected, TMCLK is the designated input to the SIU timers. When TMCLK is configured as the input to the SIU timers, the BRG1O input is disabled. See the *System Interface Unit (SIU)* chapter in the *MSC8101 Technical Reference* manual for additional information.

Table 1-5. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC25	BRG7O	Output	**Baud-Rate Generator 7 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK7	Input	**Clock 7** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	TIN4	Input	**Timer Input 4** A timer can have one of the following sources: another timer, system clock, system clock divided by 16 or a timer input. The CPM supports up to 4 timer inputs. The timer inputs can be captured on the rising, falling or both edges.
	DMA: $\overline{\text{DACK2}}$	Output	**DMA: Data Acknowledge 2** $\overline{\text{DACK2}}$, $\overline{\text{DREQ2}}$, $\overline{\text{DRACK2}}$ and $\overline{\text{DONE2}}$ belong to the SIU DMA. $\overline{\text{DONE2}}$ and $\overline{\text{DRACK2}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.
PC24	BRG8O	Output	**Baud-Rate Generator 8 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK8	Input	**Clock 8** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	TIN3	Input	**Timer Input 3** A timer can have one of the following sources: another timer, system clock, system clock divided by 16, or a timer input. The CPM supports up to four timer inputs. The timer inputs can be captured on the rising, falling, or both edges.
	Timer4: $\overline{\text{TOUT4}}$	Output	**Timer 4: Timer Out 4** The timers (Timer1–4]) can output a signal on a timer output ($\overline{\text{TOUT}}$[1–4]) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also be connected internally to the input of another timer, resulting in a 32-bit timer.
	DMA: DREQ2	Input	**DMA: Data Request 2** $\overline{\text{DACK2}}$, $\overline{\text{DREQ2}}$, $\overline{\text{DRACK2}}$, and $\overline{\text{DONE2}}$ belong to the SIU DMA. $\overline{\text{DONE2}}$ and $\overline{\text{DRACK2}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.

Table 1-5. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC23	CLK9	Input	**Clock 9** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	DMA: $\overline{\text{DACK1}}$	Output	**DMA: Data Acknowledge 1** $\overline{\text{DACK1}}$, DREQ1, $\overline{\text{DRACK1}}$, and $\overline{\text{DONE1}}$ belong to the SIU DMA. $\overline{\text{DONE1}}$ and $\overline{\text{DRACK1}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.
	EXT2	Input	**External Request 2** External request input line 2 asserts an internal request to the CPM processor. The signal can be programmed as level- or edge-sensitive, and also has programmable priority. Refer to the RISC Controller Configuration Register (RCCR) description in the Chapter 17 of the MSC8101 Reference Manual for programming information. There are no current microcode applications for this request line. It is reserved for future development.
PC22	SI1: L1ST1	Output	**Serial Interface 1: Layer 1 Strobe 1** In the time-slot assigner supported by SI1. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	CLK10	Input	**Clock 10** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	DMA: DREQ1	Input/ Output	**DMA: Request 1** $\overline{\text{DACK1}}$, DREQ1, $\overline{\text{DRACK1}}$, and $\overline{\text{DONE1}}$ belong to the SIU DMA. $\overline{\text{DONE1}}$ and $\overline{\text{DRACK1}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.

Table 1-5. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC15	SMC2: SMTXD	Output	**SMC2: Serial Management Transmit Data** Supported by SMC2. The SMC interface consists of SMTXD, SMRXD, SMSYN, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that support three protocols or modes: UART, transparent, or general-circuit interface (GCI). See also PA9.
	SCC1: $\overline{\text{CTS}}$/CLSN	Input	**SCC1: Clear To Send, Collision** Typically used in conjunction with $\overline{\text{RTS}}$. The MSC8101 SCC1 transmitter sends out a request to send data signal ($\overline{\text{RTS}}$). The request is accepted when $\overline{\text{CTS}}$ is returned low. CLSN is the signal used in Ethernet mode. See also PC29.
	FCC1: TXADDR0 *UTOPIA master*	Output	**FCC1: UTOPIA Master Transmit Address Bit 0** In the ATM UTOPIA master interface supported by FCC1, this is transmit address bit 0.
	FCC1: TXADDR0 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Transmit Address Bit 0** In the ATM UTOPIA slave interface supported by FCC1, this is transmit address bit 0.
PC14	SI1: L1ST2	Output	**Serial Interface 1: Layer 1 Strobe 2** In the time-slot assigner supported by SI1. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also be generate output wave forms for such applications as stepper-motor control.
	SCC1: $\overline{\text{CD}}$, RENA	Input	**SCC1: Carrier Detect, Receive Enable** Typically used in conjunction with $\overline{\text{RTS}}$ supported by SCC1. The MSC8101 SCC1 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low.
	FCC1: RXADDR0 *UTOPIA master*	Output	**FCC1: UTOPIA Multi-PHY Master Receive Address Bit 0** In the ATM UTOPIA master interface supported by FCC1, this is receive address bit 0.
	FCC1: RXADDR0 *UTOPIA slave*	Input	**FCC1: UTOPIA Multi-PHY Slave Receive Address Bit 0** In the ATM UTOPIA slave interface supported by FCC1, this is receive address bit 0.

Table 1-5. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC13	SI1: L1ST4	Output	**Serial Interface 1: Layer 1 Strobe 4** In the time-slot assigner supported by SI1. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	SCC2: $\overline{\text{CTS}}$,CLSN	Input	**SCC2: Clear to Send, Collision** Typically used in conjunction with $\overline{\text{RTS}}$. The MSC8101 SCC2 transmitter sends out a request to send data signal ($\overline{\text{RTS}}$). The request is accepted when $\overline{\text{CTS}}$ is returned low. CLSN is the signal used in Ethernet mode. See also PC28.
	FCC1:TXADDR1 *UTOPIA master*	Output	**FCC1: UTOPIA Multi-PHY Master Transmit Address Bit 1** In the ATM UTOPIA master interface supported by FCC1, this is transmit address bit 1.
	FCC1: TXADDR1 *UTOPIA slave*	Input	**FCC1: UTOPIA Multi-PHY Slave Transmit Address Bit 1** In the ATM UTOPIA slave interface supported by FCC1, this is transmit address bit 1.
PC12	SI1: L1ST3	Output	**Serial Interface 1: Layer 1 Strobe 3** In the time-slot assigner supported by SI1. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	SCC2: $\overline{\text{CD}}$, RENA	Input	**SCC2: Carrier Detect, Request Enable** Typically used in conjunction with $\overline{\text{RTS}}$ supported by SCC2. The MSC8101 SCC2 transmitter requests to the receiver that it sends data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low.
	FCC1: RXADDR1 *UTOPIA master*	Output	**FCC1: UTOPIA Multi-PHY Master Receive Address Bit 1** In the ATM UTOPIA master interface supported by FCC1, this is receive address bit 1.
	FCC1: RXADDR1 *UTOPIA slave*	Input	**FCC1: UTOPIA Multi-PHY Slave Receive Address Bit 1** In the ATM UTOPIA slave interface supported by FCC1, this is receive address bit 1.

Table 1-5. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC7	SI2: L1ST1	Output	**Serial Interface 2: Strobe 1** In the time-slot assigner supported by SI2. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	FCC1: $\overline{\text{CTS}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Input	**FCC1: Clear To Send** In the standard modem interface signals supported by FCC1 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{CTS}}$ is asynchronous with the data.
	FCC1: TXADDR2 *UTOPIA master*	Output	**FCC1: UTOPIA Multi-PHY Master Transmit Address Bit 2** In the ATM UTOPIA master interface supported by FCC1, this is transmit address bit 2.
	FCC1: TXADDR2 *UTOPIA slave*	Input	**FCC1: UTOPIA Multi-PHY Slave Transmit Address Bit 2** In the ATM UTOPIA slave interface supported by FCC1 using multiplexed polling, this is transmit address bit 2.
	FCC1: TXCLAV1 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY Master Transmit Cell Available 1 Direct Polling** In the ATM UTOPIA master interface supported by FCC1 using direct polling, TXCLAV1 is asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell.

Table 1-5. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC6	SI2: L1ST2	Output	**Serial Interface 2: Layer 1 Strobe 2** In the time-slot assigner supported by SI2. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	FCC1: $\overline{\text{CD}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Input	**FCC1: Carrier Detect** In the standard modem interface signals supported by FCC1 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{CD}}$ is an input asynchronous with the data.
	FCC1: RXADDR2 *UTOPIA master*	Output	**FCC1: UTOPIA Multi-PHY Master Receive Address Bit 2** In the ATM UTOPIA master interface supported by FCC1, this is receive address bit 2.
	FCC1: RXADDR2 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Receive Address Bit 2** In the ATM UTOPIA slave interface supported by FCC1 using multiplexed polling, this is receive address bit 2.
	FCC1: RXCLAV1 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY Master Receive Cell Available 1 Direct Polling** In the ATM UTOPIA master interface supported by FCC1 using direct polling, RXCLAV1 is asserted by an external PHY when one complete ATM cell is available for transfer.
PC5	SMC1: SMTXD	Output	**SMC1: Transmit Data** Supported by SMC1. The SMC interface consists of SMTXD, SMRXD, $\overline{\text{SMSYN}}$, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI).
	SI2: L1ST3	Output	**Serial Interface 2: Layer 1 Strobe 3** In the time-slot assigner supported by SI2. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	FCC2: $\overline{\text{CTS}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Input	**FCC2: Clear To Send** In the standard modem interface signals supported by FCC2 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{CTS}}$ is asynchronous with the data.

Table 1-5. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC4	SMC1: SMRXD	Input	**SMC1: Receive Data** Supported by SMC1. The SMC interface consists of SMTXD, SMRXD, SMSYN, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI).
	SI2: L1ST4	Output	**Serial Interface 2: Layer 1 Strobe 4** In the time-slot assigner supported by SI2. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	FCC2: $\overline{\text{CD}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Input	**FCC2: Carrier Detect** In the standard modem interface signals supported by FCC2 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$ and $\overline{\text{CD}}$). $\overline{\text{CD}}$ is asynchronous with the data.

1.7.4 Port D Signals

Table 1-6. Port D Signals

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PD31	SCC1: RXD	Input	**SCC1: Receive Data** Supported by SCC1. SCC1 receives serial data from RXD.
	DMA: $\overline{\text{DRACK1}}$	Output	**DMA: Data Request Acknowledge 1** $\overline{\text{DACK1}}$, DREQ1, $\overline{\text{DRACK1}}$, and $\overline{\text{DONE1}}$ belong to the SIU DMA. $\overline{\text{DONE1}}$ and $\overline{\text{DRACK1}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.
	DMA: $\overline{\text{DONE1}}$	Input/ Output	**DMA: Done 1** $\overline{\text{DACK1}}$, DREQ1, $\overline{\text{DRACK1}}$, and $\overline{\text{DONE1}}$ belong to the SIU DMA. $\overline{\text{DONE1}}$ and $\overline{\text{DRACK1}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.
PD30	SCC1: TXD	Output	**SCC1: Transmit Data** Supported by SCC1. SCC1 transmits serial data out of TXD.
	DMA: $\overline{\text{DRACK2}}$	Output	**DMA: Data Request Acknowledge 2** $\overline{\text{DACK2}}$, DREQ2, $\overline{\text{DRACK2}}$, and $\overline{\text{DONE2}}$ belong to the SIU DMA. $\overline{\text{DONE2}}$ and $\overline{\text{DRACK2}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.
	DMA: $\overline{\text{DONE2}}$	Input/ Output	**DMA: Done 2** $\overline{\text{DACK2}}$, DREQ2, $\overline{\text{DRACK2}}$, and $\overline{\text{DONE2}}$ belong to the SIU DMA. $\overline{\text{DONE2}}$ and $\overline{\text{DRACK2}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.
PD29	SCC1: $\overline{\text{RTS}}$, TENA	Output	**SCC1: Request to Send, Transmit Enable** Typically used in conjunction with $\overline{\text{CD}}$ supported by SCC2. The MSC8101 SCC1 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low. TENA is the signal used in Ethernet mode.
	FCC1: RXADDR3 UTOPIA master	Output	**FCC1: UTOPIA Multi-PHY Master Receive Address Bit 3** In the ATM UTOPIA master interface supported by FCC1 using multiplexed polling, this is receive address bit 3.
	FCC1: RXADDR3 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Receive Address Bit 3** In the ATM UTOPIA slave interface supported by FCC1 using multiplexed polling, this is receive address bit 3.
	FCC1: RXCLAV2 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY Master Receive Cell Available 2 Direct Polling** In the ATM UTOPIA master interface supported by FCC1 using direct polling, RXCLAV2 is asserted by an external PHY when one complete ATM cell is available for transfer.

Table 1-6. Port D Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PD19	FCC1: TXADDR4 *UTOPIA master*	Output	**FCC1: Multi-PHY Master Transmit Address Bit 4 Multiplexed Polling** In the ATM UTOPIA master interface supported by FCC1 using multiplexed polling, this is transmit address bit 4.
	FCC1: TXADDR4 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Transmit Address Bit 4** In the ATM UTOPIA slave interface supported by FCC1 using multiplexed polling, this is transmit address bit 4.
	FCC1: TXCLAV3 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY master Transmit Cell Available 3 Direct Polling** In the ATM UTOPIA master interface supported by FCC1 using direct polling, TXCLAV3 is asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell.
	BRG1O	Output	**Baud Rate Generator 1 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins. BRG1O can be the internal input to the SIU timers. When CLK5 is selected (see PC27 above), it is the source for BRG1O which is the default input for the SIU timers. See the *System Interface Unit (SIU)* chapter in the *MSC8101 Technical Reference* manual for additional information. If CLK5 is not enabled, BRG1O uses an internal input. If TMCLK is enabled (see PC26 above), the BRG1O input to the SIU timers is disabled.
	SPI: $\overline{\text{SPISEL}}$	Input	**SPI: Select** The SPI interface comprises four signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK) and select ($\overline{\text{SPISEL}}$). The SPI can be configured as a slave or master in single- or multiple-master environments. $\overline{\text{SPISEL}}$ is the enable input to the SPI slave. In a multimaster environment, $\overline{\text{SPISEL}}$ (always an input) detects an error when more than one master is operating. SPI masters must output a slave select signal to enable SPI slave devices by using a separate general-purpose I/O signal. Assertion of an SPI $\overline{\text{SPISEL}}$ while it is master causes an error.

Table 1-6. Port D Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PD18	FCC1: RXADDR4 *UTOPIA master*	Output	**FCC1: UTOPIA Master Receive Address Bit 4** In the ATM UTOPIA master interface supported by FCC1 using multiplexed polling, this is receive address bit 4.
	FCC1: RXADDR4 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Receive Address Bit 4** In the ATM UTOPIA slave interface supported by FCC1, this is the receive address bit 4.
	FCC1: RXCLAV3 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY Master Receive Cell Available 3 Direct Polling** In the ATM UTOPIA master interface supported by FCC1 using direct polling, RXCLAV3 is asserted by an external PHY when one complete ATM cell is available for transfer.
	SPI: SPICLK	Input/ Output	**SPI: Clock** The SPI interface comprises four signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK) and select (SPISEL). The SPI can be configured as a slave or master in single- or multiple-master environments. SPICLK is a gated clock, active only during data transfers. Four combinations of SPICLK phase and polarity can be configured. When the SPI is a master, SPICLK is the clock output signal that shifts received data in from SPIMISO and transmitted data out to SPIMOSI.
PD17	BRG2O	Output	**Baud Rate Generator 2 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally to the MSC8101 and/or provide an output to one of the 8 BRG pins.
	FCC1: RXPRTY *UTOPIA*	Input	**FCC1: UTOPIA Receive Parity** In the ATM UTOPIA interface supported by FCC1, this is the odd parity bit for RXD[0–7].
	SPI: SPIMOSI	Input/ Output	**SPI: Master Output Slave Input** The SPI interface comprises our signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK) and select (SPISEL**).** The SPI can be configured as a slave or master in single- or multiple-master environments. When the SPI is a slave, SPICLK is the clock input that shifts received data in from SPIMOSI and transmitted data out through SPIMISO.
PD16	FCC1: TXPRTY *UTOPIA*	Output	**FCC1: UTOPIA Transmit Parity** In the ATM UTOPIA interface supported by FCC1, this is the odd parity bit for TXD[0–7].
	SPI: SPIMISO	Input/ Output	**SPI: Master Input Slave Output** The SPI interface comprises four signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK), and select (SPISEL). The SPI can be configured as a slave or master in single- or multiple-master environments. When the SPI is a slave, SPICLK is the clock input that shifts received data in from SPIMOSI and transmitted data out through SPIMISO.

Table 1-6. Port D Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PD7	SMC1: $\overline{\text{SMSYN}}$	Input	**SMC1: Serial Management Synchronization** Supported by SMC1. $\overline{\text{SMSYN}}$ is an input. The SMC interface consists of SMTXD, SMRXD, $\overline{\text{SMSYN}}$ and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent or general-circuit interface (GCI).
	FCC1: TXADDR3 *UTOPIA master*	Output	**FCC1: UTOPIA Master Transmit Address Bit 3** In the ATM UTOPIA master interface supported by FCC1 using multiplexed polling, this is transmit address bit 3.
	FCC1: TXADDR3 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Transmit Cell Available 2** In the ATM UTOPIA slave interface supported by FCC1 using multiplexed polling, this is transmit address bit 3.
	FCC1: TXCLAV2 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY Master Transmit Cell Available 2 Direct Polling** In the ATM UTOPIA master interface supported by FCC1 using direct polling, TXCLAV2 is asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell.

1.8 JTAG Test Access Port Signals

The MSC8101 supports the standard set of Test Access Port (TAP) signals defined by IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture specification and described in **Table 1-7**.

Table 1-7. JTAG Test Access Port Signals

Signal Name	Type	Signal Description
TCK	Input	**Test Clock—**A test clock signal for synchronizing JTAG test logic.
TDI	Input	**Test Data Input—**A test data serial signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.
TDO	Output	**Test Data Output—**A test data serial signal for test instructions and data. TDO can be tri-stated. The signal is actively driven in the shift-IR and shift-DR controller states and changes on the falling edge of TCK.
TMS	Input	**Test Mode Select—**Sequences the test controller's state machine, is sampled on the rising edge of TCK, and has an internal pull-up resistor.
$\overline{\text{TRST}}$	Input	**Test Reset—**Asynchronously initializes the test controller, has an internal pull-up resistor, and must be asserted after power up.

1.9 Reserved Signals

Table 1-8. Reserved Signals

Signal Name	Type	Signal Description
TEST	Input	**Test** Used for manufacturing testing. You must connect this input to GND.
THERM[1–2]	—	Leave disconnected.
SPARE1, 5	—	**Spare Pins** Leave disconnected for backward compatibility with future revisions of this device.

Chapter 2A

Specifications (mask set 2K42A)

2A.1 Introduction

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MSC8101 communications processor, mask set 2K42A. For additional information, see the *MSC8101 Reference Manual*.

2A.2 Absolute Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2A-1 describes the maximum electrical ratings for the MSC8101.

Table 2A-1. Absolute Maximum Ratings[2]

Rating	Symbol	Value	Unit
Core supply voltage[3]	V_{DD}	–0.2 to 1.7	V
PLL supply voltage[3]	V_{CCSYN}	–0.2 to 1.7	V
I/O supply voltage[3]	V_{DDH}	–0.2 to 3.6	V
Input voltage[3]	V_{IN}	(GND – 0.2) to 3.6	V
Maximum operating temperature range[4]	T_J	–40 to 120	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 2A-2.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. The input voltage must not exceed the I/O supply V_{DDH} by more than 2.5 V at any time, including during power-on reset. In turn, V_{DDH} can exceed V_{DD}/V_{CCSYN} by more than 3.3 V during power-on reset, but for no more than 100 ms. V_{DDH} should not exceed V_{DD}/V_{CCSYN} by more than 2.1 V during normal operation. V_{DD}/V_{CCSYN} must not exceed V_{DDH} by more than 0.4 V at any time, including during power-on reset. See **Section 4.2**, *Electrical Design Considerations*, on page 4-2 for more information.
4. **Section 4.1**, *Thermal Design Considerations*, on page 4-1 includes a formula for computing the chip junction temperature (T_J).

2A.3 Recommended Operating Conditions

Table 2A-2 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2A-2. Recommended Operating Conditions

Rating	Symbol	Value	Unit
SC140 Core supply voltage	V_{DD}	1.5 to 1.7	V
PLL supply voltage	V_{CCSYN}	1.5 to 1.7	V
I/O supply voltage	V_{DDH}	3.135 to 3.465	V
Input voltage	V_{IN}	–0.2 to V_{DDH} + 0.2	V
Operating temperature range	T_J	–40 to 105	°C

2A.4 Thermal Characteristics

Table 2A-3 describes thermal characteristics of the MSC8101.

Table 2A-3. Thermal Characteristics

Characteristic	Symbol	Lidded FC-PBGA 17 × 17mm	Unit
Junction-to-ambient[1, 2]	$R_{\theta JA}$ or θ_{JA}	26	°C/W
Junction-to-board (bottom)[3]	$R_{\theta JB}$ or θ_{JB}	9.5	°C/W
Junction-to-case (top)[4]	$R_{\theta JC}$ or θ_{JC}	0.8	°C/W

Table 2A-3. Thermal Characteristics (Continued)

Characteristic	Symbol	Lidded FC-PBGA 17 × 17mm	Unit
Notes: **1.** Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. **2.** Per SEMI G38-87 and EIA/JESD51-2 with the single layer (1s) board horizontal. **3.** Thermal resistance between the die and the printed circuit board per JESD 51-8. **4.** Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for case temperature. **5.** Numbers based on simulations. Actual values TBD.			

See **Section 4.1**, *Thermal Design Considerations*, on page 4-1 for details on these characteristics.

2A.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8101. The measurements in **Table 2A-4** assume the following system conditions:

- T_J = 0 – 100 °C
- V_{DD} = 1.6 V ± 5% V_{DC}
- V_{DDH} = 3.3 V ± 5% V_{DC}
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal V_{DDH} and V_{DD} or both V_{DDH} and V_{DD} must vary in the same direction (for example, both V_{DDH} and V_{DD} vary by ± 5 percent).

Table 2A-4. DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.5	3.465	V
CLKIN input low voltage[1]	V_{ILC}	GND	0.8	V
Input leakage current, V_{IN} = V_{DDH}	I_{IN}	—	10	µA
Tri-state (high impedance off state) leakage current, V_{IN} = V_{DDH}	I_{OZ}	—	10	µA
Signal low input current, V_{IL} = 0.4 V	I_L	—	–4.0	mA
Signal high input current, V_{IH} = 2.0 V	I_H	—	4.0	mA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.4	—	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0.4	V
Notes: **1.** The optimum CLKIN duty cycle is obtained when: V_{ILC} = V_{DDH} – V_{IHC}.				

Table 2A-5. Typical Power Dissipation

Characteristic	Symbol	Typical	Unit
Core power dissipation at 275 MHz	P_{CORE}	320	mW
CPM power dissipation at 137.5 MHz	P_{CPM}	220	mW
SIU power dissipation at 68.75 MHz	P_{SIU}	55	mW
Core leakage power	P_{LCO}	3	mW
CPM leakage power	P_{LCP}	6	mW
SIU leakage power	P_{LSI}	2	mW

2A.6 Clock Configuration

The following sections provide a general description of clock configuration.

2A.6.1 Valid Clock Modes

Table 2A-6 shows the maximum frequency values for each rated core frequency (250 or 275 MHz). The user must ensure that maximum frequency values are not exceeded.

Table 2A-6. Maximum Frequencies

Characteristic	Maximum Frequency in MHz	
Core Frequency	250	275
CPM Frequency (CPMCLK)	125	137.5
Bus Frequency (BCLK)	50	68.75
Serial Communication Controller Clock Frequency (SCLK)	62.5	68.75
Baud Rate Generator Clock Frequency (BRGCLK)	62.5	68.75
External Clock Output Frequency (CLKOUT)	50	68.75

Six bit values map the MSC8101 clocks to one of the valid configuration mode options. Each option determines the CLKIN, SC140 core, system bus, SCC clock, CPM, and CLKOUT frequencies. The six bit values are derived from three dedicated input pins (MODCK[1–3]) and three bits from the reset configuration word (MODCK_H). To configure the SPLL pre-division factor, SPLL multiplication factor, and the frequencies for the SC140 core, SCC clocks, CPM parallel I/O ports, and system buses, the MODCK[1–3] pins are sampled and combined with the MODCK_H values when the internal power-on reset (internal $\overline{\text{PORESET}}$) is deasserted. Clock configuration changes only when the internal $\overline{\text{PORESET}}$ signal is deasserted.

The following factors are configured:

- SPLL pre-division factor (SPLL PDF)
- SPLL multiplication factor (SPLL MF)
- Bus post-division factor (Bus DF)

The SCC division factor (SCC DF) is fixed at 4 and the CPM division factor (CPM DF) is fixed at 2. The BRG division factor (BRG DF) is configured through the System Clock Control Register (SCCR) and can be 4, 16 (default after reset), 64, or 256.

Note: Refer to *AN2288/D Clock Mode Selection for MSC8101 Mask Set 2K42A* for details on clock configuration.

2A.6.2 Clocks Programming Model

This section describes the clock registers in detail. The registers discussed are as follows:

- System Clock Control Register (SCCR)
- System Clock Mode Register (SCMR)

2A.6.2.1 System Clock Control Register

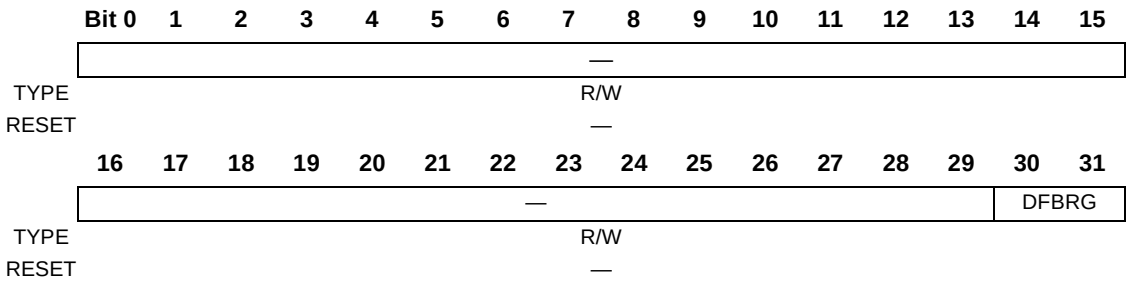


Figure 2A-1. System Clock Control Register (SCCR)—**0x10C80**

The SCCR is memory-mapped into the SIU register map of the MSC8101.

Table 2A-7. SCCR Bit Descriptions

Name Bit No.	Defaults		Description	Settings
	PORESET	Hard Reset		
— 0–29	—	—	Reserved	
DFBRG 30–31	01	Unaffected	**Division Factor for the BRG Clock** Defines the BRGCLK frequency. Changing this value does not result in a loss of lock condition.	00 Divide by 4 01 Divide by 16 (default value) 10 Divide by 64 11 Divide by 256

2A.6.2.2 System Clock Mode Register

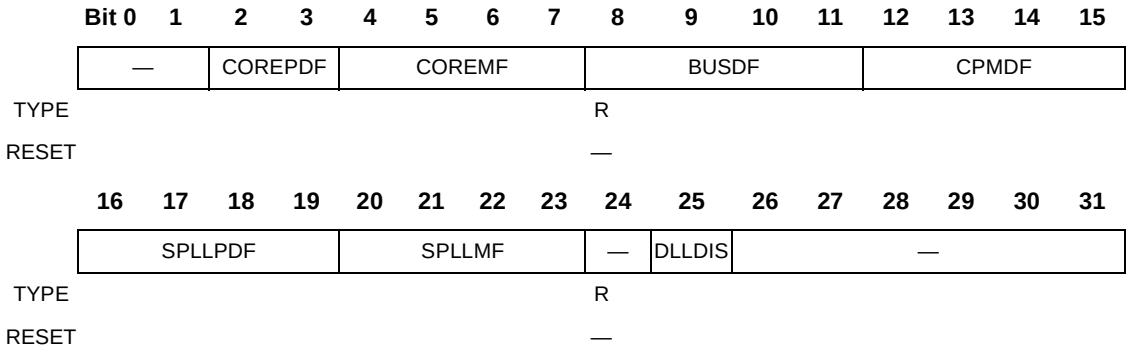


Figure 2A-2. System Clock Mode Register (SCMR)—**0x10C88**

SCMR is a read-only register that is updated during power-on reset (PORESET) and provides the mode control signals to the PLLs, DLL, and clock logic. This register reflects the currently defined configuration settings. For details of the available setting options, see *AN2288*.

Table 2A-8. SCMR Bit Descriptions

Name Bit No.	Defaults		Description	Settings
	PORESET	**Hard Reset**		
— 0–1	—	—	Reserved	
COREPDF 2–3	Configuration Pins	Unaffected	**Core PLL Pre-Division Factor**	00 CPLL PDF= 1 01 CPLL PDF= 2 10 CPLL PDF= 3 11 CPLL PDF= 4
COREMF 4–7	Configuration Pins	Unaffected	**Core Multiplication Factor**	0101 MF = 10 0110 MF = 12 All other combinations not used.
BUSDF 8–11	Configuration Pins	Unaffected	**60x Bus Division Factor**	0010 Bus DF = 3 0011 Bus DF = 4 0100 Bus DF = 5 All other combinations not used.
CPMDF 12–15	Configuration Pins	Unaffected	**CPM Division Factor**	0001 CPM DF = 2 All other combinations are not used.
SPLLPDF 16–19	Configuration Pins	Unaffected	**SPLL Pre-Division Factor**	0000 SPLL PDF = 1 0001 SPLL PDF = 2 0010 SPLL PDF = 3 0011 SPLL PDF = 4 All other combinations not used
SPLLMF 20–23	Configuration Pins	Unaffected	**SPLL Multiplication Factor**	0110 SPLL MF = 12 0111 SPLL MF = 14 1000 SPLL MF = 16 1001 SPLL MF = 18 1010 SPLL MF = 20 1011 SPLL MF = 22 1100 SPLL MF = 24 1101 SPLL MF = 26 1110 SPLL MF = 28 1111 SPLL MF = 30 All other combinations not used
— 24	—	—	Reserved	
DLLDIS 25	Configuration Pins	Unaffected	**DLL Disable**	0 DLL operation is enabled 1 DLL is disabled
— 26–31	—	—	Reserved	

2A.7 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. AC timings are based on a 50 pF load, except where noted otherwise, and 50 Ω transmission line.

2A.7.1 Clocking and Timing Characteristics

Table 2A-9. System Clock Parameters

Characteristic	Minimum	Maximum	Unit
Phase Jitter between BCLK and DLLIN	—	0.5	ns
CLKIN frequency[1,2]	18	75	MHz
CLKIN slope	—	5	ns
DLLIN slope	—	2	ns
CLKOUT frequency jitter	—	(0.01/CLKOUT) + CLKIN jitter	ns
Delay between CLKOUT and DLLIN	—	5	ns

Notes: **1.** Low CLKIN frequency causes poor PLL performance. Choose a CLKIN frequency high enough to keep the frequency after the predivider (SPLLMFCLK) higher than 18 MHz.
2. CLKIN should have a 50% ± 5% duty cycle.

Table 2A-10. Clock Ranges

Clock	Symbol	Maximum Rated Core Frequency		
		All	Max. Values for SC140 Clock Rating of:	
		Min	250 MHz	275 MHz
Input Clock	CLKIN	18 MHz	62.5	68.75 MHz
SPLL MF Clock	SPLLMFCLK	18 MHz	20.83	22.9 MHz
Bus	BCLK	18 MHz	62.5 MHz	68.75 MHz
Output	CLKOUT	43.2 MHz	62.5 MHz	68.75 MHz
Serial Communications Controller	SCLK	18 MHz	62.5 MHz	68.75 MHz
Communications Processor Module	CPMCLK	36 MHz	125 MHz	137.5 MHz
SC140 Core	DSPCLK	72 MHz	250 MHz	275 MHz
Baud Rate Generator • For BRG DF = 4 • For BRG DF = 16 (default) • For BRG DF = 64 • For BRG DF = 256	BRGCLK	 36 MHz 9 MHz 2.25 MHz 562.5 KHz	 62.5 MHz 15.63 MHz 3.91 MHz 976.6 KHz	 68.75 MHz 17.19 MHz 4.30 MHz 1.07 MHz

2A.7.2 Reset Timing

The MSC8101 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)

Asserting an external $\overline{\text{PORESET}}$ causes concurrent assertion of an internal $\overline{\text{PORESET}}$ signal, $\overline{\text{HRESET}}$, and $\overline{\text{SRESET}}$. When the external $\overline{\text{PORESET}}$ signal is deasserted, the MSC8101 samples several configuration pins:

- $\overline{\text{RSTCONF}}$—determines whether the MSC8101 is a master (0) or slave (1) device
- DBREQ—determines whether to operate in normal mode (0) or invoke the SC140 debug mode (1)
- HPE—disable (0) or enable (1) the host port (HDI16)
- BTM[0–1]—boot from external memory (00) or the HDI16 (01)

All these reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the last sources to cause a reset. **Table 2A-11** describes reset causes.

Table 2A-11. Reset Causes

Name	Direction	Description
Power-on reset ($\overline{\text{PORESET}}$)	Input	$\overline{\text{PORESET}}$ initiates the power-on reset flow that resets all the MSC8101s and configures various attributes of the MSC8101, including its clock mode.
Hard reset ($\overline{\text{HRESET}}$)	Input/Output	The MSC8101 can detect an external assertion of $\overline{\text{HRESET}}$ only if it occurs while the MSC8101 is not asserting reset. During $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ is asserted. $\overline{\text{HRESET}}$ is an open-drain pin.
Soft reset ($\overline{\text{SRESET}}$)	Input/Output	The MSC8101 can detect an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8101 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin.

2A.7.2.1 Reset Operation

The reset control logic determines the cause of a reset, synchronizes it if necessary, and resets the appropriate logic modules. The memory controller, system protection logic, interrupt controller, and parallel I/O pins are initialized only on hard reset. Soft reset initializes the internal logic while maintaining the system configuration. The MSC8101 has two mechanisms for reset configuration: host reset configuration and hardware reset configuration.

2A.7.2.2 Power-On Reset Flow

Asserting the $\overline{\text{PORESET}}$ external pin initiates the power-on reset flow. $\overline{\text{PORESET}}$ should be asserted externally for at least 16 input clock cycles after external power to the MSC8101 reaches at least 2/3 V_{CC}. As **Table 2A-12** shows, the MSC8101 has five configuration pins, four of which are multiplexed with the SC140 core EONCE Event (EE[0–1], EE[4–5]) pins and the fifth of which is the $\overline{\text{RSTCONF}}$ pin. These pins are sampled at the rising edge of $\overline{\text{PORESET}}$. In addition to these configuration pins, three (MODCK[1–3]) pins are sampled by the MSC8101. The signals on these pins and the MODCK_H value in the Hard Reset Configuration Word determine the PLL locking mode, by defining the ratio between the DSP clock, the bus clocks, and the CPM clock frequencies.

Table 2A-12. External Configuration Signals

Pin	Description	Settings
RSTCONF	**Reset Configuration** Input line sampled by the MSC8101 at the rising edge of PORESET.	0 Reset Configuration Master. 1 Reset Configuration Slave.
DBREQ/ EE0	**EONCE Event Bit 0** Input line sampled after SC140 core PLL locks. Holding EE0 high when PORESET is deasserted puts the SC140 core into Debug mode.	0 SC140 core starts the normal processing mode after reset. 1 SC140 core enters Debug mode immediately after reset.
HPE/EE1	**Host Port Enable** Input line sampled at the rising edge of PORESET. If asserted, the Host port is enabled, the system data bus is 32-bit wide, and the Host *must* program the reset configuration word.	0 Host port disabled (hardware reset configuration enabled). 1 Host port enabled.
BTM[0–1]/ EE[4–5]	**Boot Mode** Input lines sampled at the rising edge of PORESET, which determine the MSC8101 Boot mode.	00 MSC8101 boots from external memory. 01 MSC8101 boots from HDI16. 10 Reserved. 11 Reserved.

Table 2A-13. Reset Timing

No.	Characteristics	Expression	Min	Max	Unit
1	Required external PORESET duration minimum • CLKIN = 18 MHz • CLKIN = 75 MHz	16 / CLKIN	 888.8 213.3	 — —	 ns ns
2	Delay from deassertion of external PORESET to deassertion of internal PORESET • CLKIN = 18 MHz • CLKIN = 75 MHz	1024 / CLKIN	 56.89 13.65		 µs µs
3	Delay from deassertion of internal PORESET to SPLL lock • SPLLMFCLK = 18 MHz • SPLLMFCLK = 25 MHz	800 / SPLLMFCLK	 44.4 32.0		 µs µs
4	Delay from SPLL lock to DLL lock • DLL enabled — BCLK = 18 MHz — BCLK = 75 MHz • DLL disabled	 3073 / BLCK —	 170.72 40.97 0.0		 µs µs ns
5	Delay from SPLL lock to HRESET deassertion • DLL enabled — BCLK = 18 MHz — BCLK = 75 MHz • DLL disabled — BCLK = 18 MHz — BCLK = 75 MHz	 3585 / BLCK 512 / BLCK	 199.17 47.5 28.4 6.83		 µs µs µs µs
6	Delay from SPLL lock to SRESET deassertion • DLL enabled — BCLK = 18 MHz — BCLK = 75 MHz • DLL disabled — BCLK = 18 MHz — BCLK = 75 MHz	 3588 / BLCK 515 / BLCK	 199.33 47.84 28.61 6.87		 µs µs µs µs
Note:	Value given for lowest possible CLKIN frequency 18 MHz to ensure proper initialization of reset sequence.				

2A.7.2.3 Host Reset Configuration

Host reset configuration allows the host to program the reset configuration word via the Host port after PORESET is deasserted, as described in the *MSC8101 Reference Manual*. The MSC8101 samples the signals described in **Table 2A-12** one the rising edge of PORESET when the signal is deasserted.

If HPE is sampled high, the host port is enabled. In this mode the RSTCONF pin *must* be pulled up. The device extends the internal PORESET until the host programs the reset configuration word register. The host must write four 8-bit half-words to the Host Reset Configuration Register address to program the reset configuration word, which is 32 bits wide. For more information, see the *MSC8101 Reference Manual*. The reset configuration word is programmed before the internal PLL and DLL in the MSC8101 are locked. The host must program it after the rising edge of the PORESET input. In this mode, the host must have its own clock that does not depend on the MSC8101 clock. After the PLL and DLL are locked, HRESET remains asserted for another 512 bus clocks and is then released. The SRESET is released three bus clocks later (see **Figure 2A-3**).

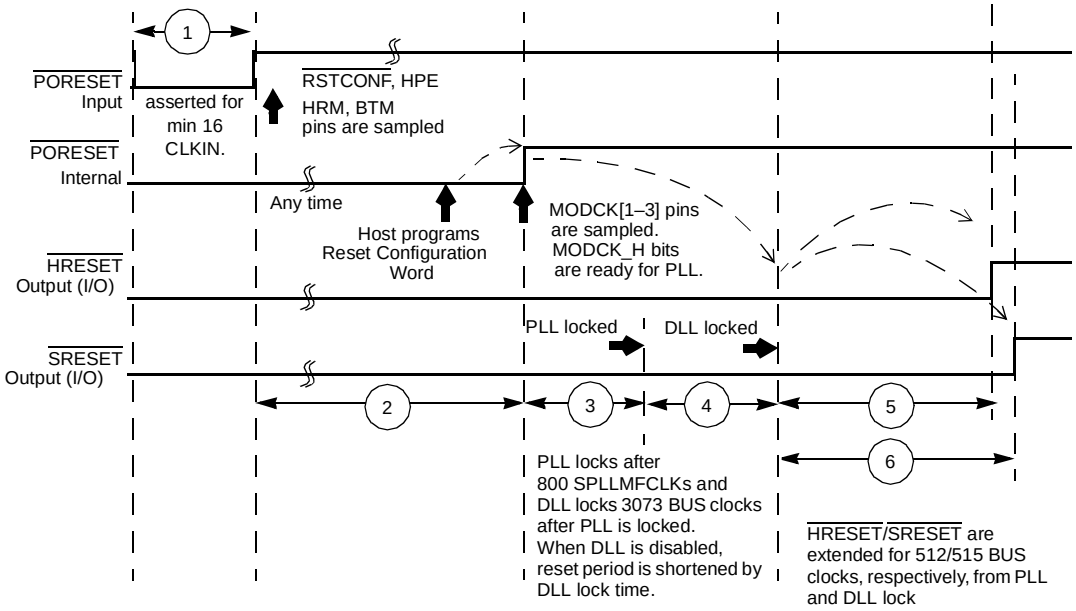


Figure 2A-3. Host Reset Configuration Timing

2A.7.2.4 Hardware Reset Configuration

Hardware reset configuration is enabled if HPE is sampled low at the rising edge of PORESET. The value driven on RSTCONF while PORESET changes from assertion to deassertion determines the MSC8101 configuration. If RSTCONF is deasserted (driven high) while PORESET changes, the MSC8101 acts as a configuration slave. If RSTCONF is asserted (driven low) while PORESET changes, the MSC8101 acts as a configuration master. **Section 2A.7.2.4**, *Hardware Reset Configuration*, explains the configuration sequence and the terms “configuration master” and “configuration slave.”

Directly after the deassertion of PORESET and choice of the reset operation mode as configuration master or configuration slave, the MSC8101 starts the configuration process. The MSC8101 asserts HRESET and SRESET throughout the power-on reset process, including configuration. Configuration takes 1024 CLOCKIN cycles, after which MODCK[1–3] are sampled to determine the MSC8101’s working mode.

Next, the MSC8101 halts until the SPLL locks. The SPLL locks according to MODCK[1–3], which are sampled, and to MODCK_H taken from the Reset Configuration Word. SPLL locking time is 800 reference clocks, which is the clock at the output of the SPLL Pre-divider. After the SPLL is locked, all the clocks to the MSC8101 are enabled. If the DLLDIS bit in the reset configuration word is reset, the DLL starts the locking process after the SPLL is locked. During PLL and DLL locking, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are asserted. $\overline{\text{HRESET}}$ remains asserted for another 512 BUS clocks and is then released. The $\overline{\text{SRESET}}$ is released three bus clocks later. If the DLLDIS bit in the reset configuration word is set, the DLL is bypassed and there is no locking process, thus saving the DLL locking time. **Figure 2A-4** shows the power-on reset flow.

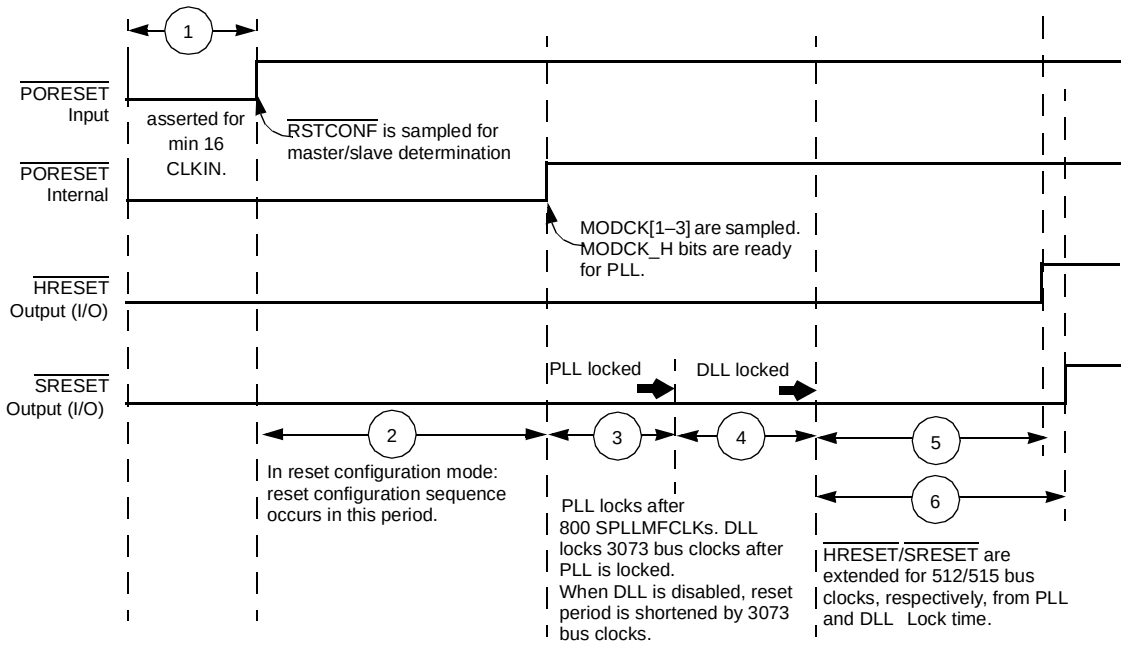


Figure 2A-4. Hardware Reset Configuration Timing

2A.7.3 System Bus Access Timing

2A.7.3.1 Core Data Transfers

Generally, all MSC8101 bus and system output signals are driven from the rising edge of the reference clock (REFCLK), which is DLLIN or, if the DLL is disabled, CLKOUT. Memory controller signals, however, trigger on four points within a REFCLK cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of REFCLK (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 2A-14** shows.

Table 2A-14. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of REFCLK)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 REFCLK	1/2 REFCLK	3/4 REFCLK
1:2.5	3/10 REFCLK	1/2 REFCLK	8/10 REFCLK
1:3.5	4/14 REFCLK	1/2 REFCLK	11/14 REFCLK

Figure 2A-5 is a graphical representation of **Table 2A-14**.

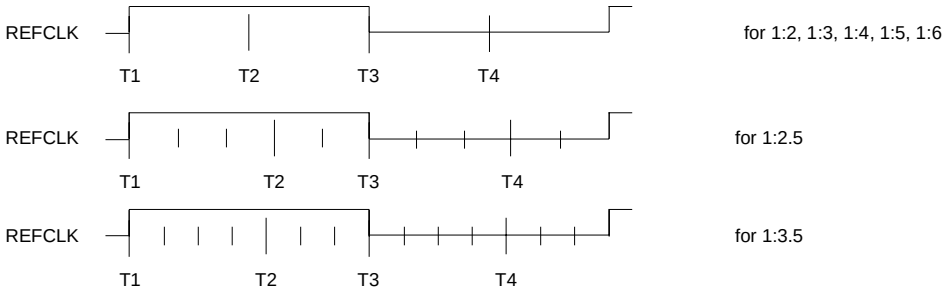


Figure 2A-5. Internal Tick Spacing for Memory Controller Signals

Note: The UPM machine and GPCM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. SDRAM machine outputs change only on the REFCLK rising edge.

Table 2A-15. AC Characteristics for SIU Inputs

No.	Characteristic[1]	Value	Units
10	Hold time for all signals after the 50% level of the REFCLK rising edge	0.5	ns
11	$\overline{\text{AACK}}$/$\overline{\text{ARTRY}}$/$\overline{\text{TA}}$/$\overline{\text{TEA}}$/$\overline{\text{DBG}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$ setup time before the 50% level of the REFCLK rising edge	5	ns
12	Data bus setup time before the 50% level of the REFCLK rising edge	7.5	ns
13	Data bus setup time in ECC and parity modes before the 50% level of the REFCLK rising edge	11	ns
14	DP setup time before the 50% level of the REFCLK rising edge	5.5	ns
15a[2,3]	Address setup time before the 50% level of the REFCLK rising edge	4	ns
15b	$\overline{\text{TS}}$, TT, and $\overline{\text{TBST}}$ setup time before the 50% level of the REFCLK rising edge	6	ns
15c	$\overline{\text{PSDVAL}}$ setup time before the 50% level of the REFCLK rising edge	5.5	ns
15d	Setup time before the 50% level of the REFCLK rising edge for all other signals	7	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the REFCLK rising edge.
2. EXDD = 0 only. For EXDD = 1, the maximum bus speed is 50 MHz.
3. TSIZ is multicycle.

Table 2A-16. AC Characteristics for SIU Outputs

No.	Characteristic	Max.[2]	Min.	Units
31	$\overline{\text{PSDVAL}}$/$\overline{\text{TEA}}$/$\overline{\text{TA}}$ delay from the 50% level of the REFCLK rising edge	9	1.0	ns
32a	Address bus/Address attributes/$\overline{\text{GBL}}$ delay from the 50% level of the REFCLK rising edge	8.5	1.0	ns
32b	BADDR delay from the 50% level of the REFCLK rising edge	10	1.0	ns
32c	$\overline{\text{TS}}$ delay from the 50% level of the REFCLK rising edge	8.5	1.0	ns
33a	Data bus delay from the 50% level of the REFCLK rising edge	7	1.0	ns
33b	DP delay from the 50% level of the REFCLK rising edge	8.5	1.0	ns

Table 2A-16. AC Characteristics for SIU Outputs (Continued)

No.	Characteristic	Max.[2]	Min.	Units
34	Memory controller signals/ALE delay from the 50% level of the REFCLK rising edge	6	1.0	ns
35	All other signals delay from the 50% level of the REFCLK rising edge	6	1.0	ns

Notes:
1. Certain bus modes, such as non-extra cycle (EXDD = 1), non-pipelined, and ECC/Parity modes, result in slower bus frequencies.
2. Output specifications are measured from the 50% level of the REFCLK rising edge to the 50% level of the signal.

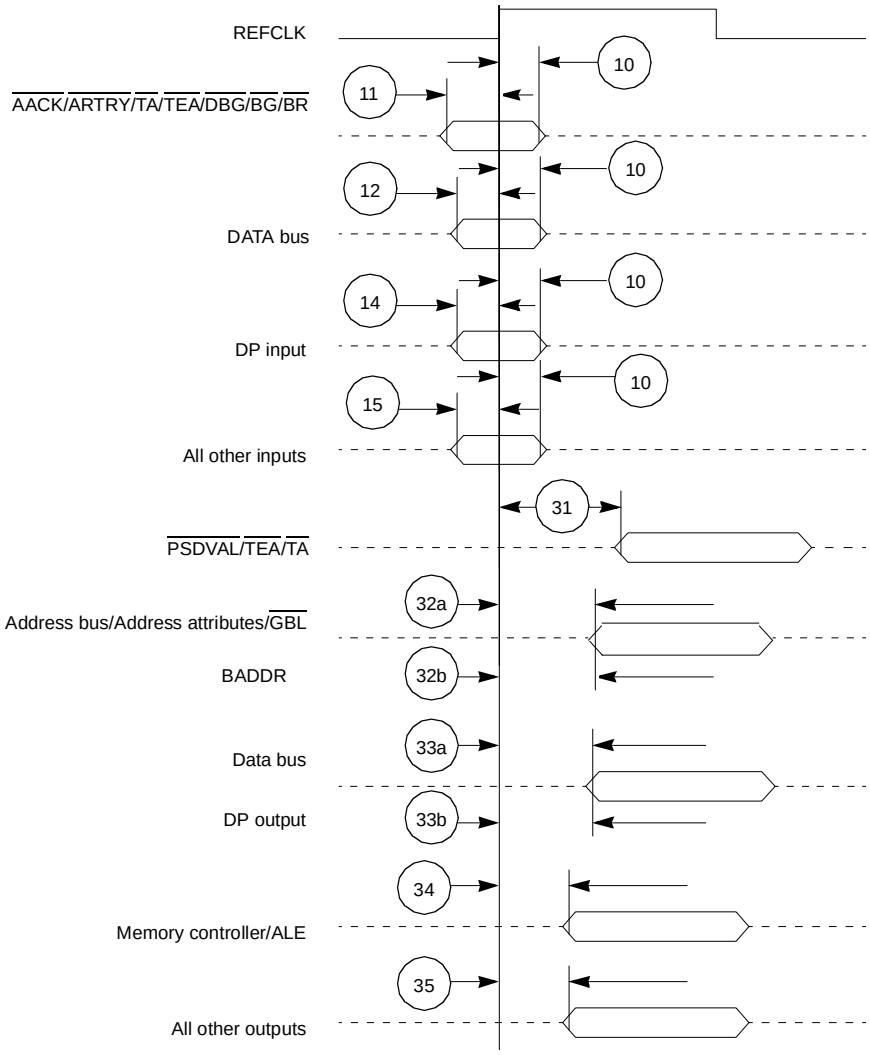


Figure 2A-6. Bus Signals

2A.7.3.2 DMA Data Transfers

Table 2A-17 describes the DMA signal timing.

Table 2A-17. DMA Signals

Number	Characteristic	Minimum	Maximum	Units
72	DREQ setup time before the 50% level of the REFCLK falling edge	6	—	ns
73	DREQ hold time after the 50% level of the REFCLK falling edge	0.5	—	ns
74	$\overline{\text{DONE}}$ setup time before the 50% level of the REFCLK rising edge	9	—	ns
75	$\overline{\text{DONE}}$ hold time after the 50% level of the REFCLK rising edge	0.5	—	ns
76	$\overline{\text{DACK}}$/$\overline{\text{DRACK}}$/$\overline{\text{DONE}}$ delay after the 50% level of the REFCLK rising edge	0.5	9	ns

The DREQ signal is synchronized with the 50% level of the falling edge of REFCLK. $\overline{\text{DONE}}$ timing is relative to the 50% level of the rising edge of REFCLK. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 2A-17**. **Figure 2A-7** shows synchronous peripheral interaction.

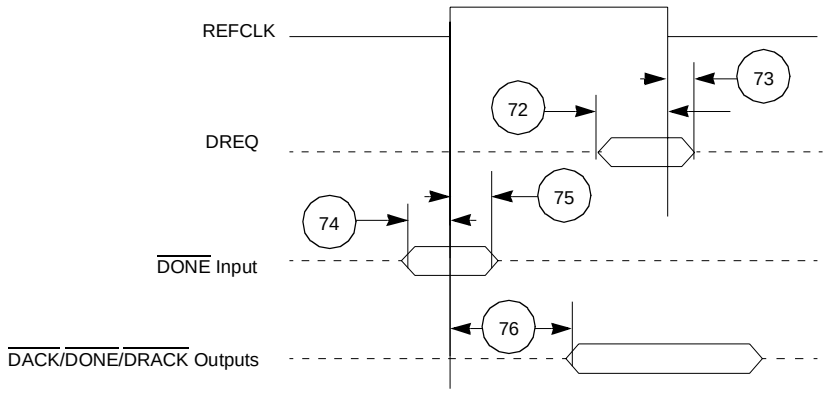


Figure 2A-7. DMA Signals

2A.7.4 HDI16 Signals

Table 2A-18. Host Interface (HDI16) Timing[1, 2]

Number	Characteristics[3]	Expression	Value	Unit
44a	Read data strobe minimum assertion width[4] HACK read minimum assertion width	$(1.5 \times T_C) + 5.0$	Note 11	ns
44b	Read data strobe minimum deassertion width[4] HACK read minimum deassertion width	$T_C + 5.0$	Note 11	ns
44c	Read data strobe minimum deassertion width[4] after "Last Data Register" reads[5,6], or between two consecutive CVR, ICR, or ISR reads[7] HACK minimum deassertion width after "Last Data Register" reads[5,6]	$(2.5 \times T_C) + 5.0$	Note 11	ns
45	Write data strobe minimum assertion width[8] HACK write minimum assertion width	$(1.5 \times T_C) + 5.0$	Note 11	ns
46	Write data strobe minimum deassertion width[8] HACK write minimum deassertion width after ICR, CVR and Data Register writes[5]	$(2.5 \times T_C) + 5.0$	Note 11	ns
47	Host data input minimum setup time before write data strobe deassertion[8] Host data input minimum setup time before HACK write deassertion	—	5.0	ns
48	Host data input minimum hold time after write data strobe deassertion[8] Host data input minimum hold time after HACK write deassertion	—	5.0	ns
49	Read data strobe minimum assertion to output data active from high impedance[4] HACK read minimum assertion to output data active from high impedance	—	5.0	ns
50	Read data strobe maximum assertion to output data valid[4] HACK read maximum assertion to output data valid	$(2.0 \times T_C) + 5.0$	Note 11	ns
51	Read data strobe maximum deassertion to output data high impedance[4] HACK read maximum deassertion to output data high impedance	—	5.0	ns
52	Output data minimum hold time after read data strobe deassertion[4] Output data minimum hold time after HACK read deassertion	—	5.0	ns
53	HCS[1–2] minimum assertion to read data strobe assertion[4]	—	5.0	ns
54	HCS[1–2] minimum assertion to write data strobe assertion[8]	—	5.0	ns
55	HCS[1–2] maximum assertion to output data valid	$T_C + 5.0$	Note 11	ns
56	HCS[1–2] minimum hold time after data strobe deassertion[9]	—	0.0	ns
57	HA[0–3], HRW minimum setup time before data strobe assertion[9] • Read • Write	—	 0 5.0	 ns ns
58	HA[0–3], HRW minimum hold time after data strobe deassertion[9]	—	5.0	ns
61	Maximum delay from read data strobe deassertion to host request deassertion for "Last Data Register" read[4, 5, 10]	$(3.5 \times T_C) + 5.0$	Note 11	ns
62	Maximum delay from write data strobe deassertion to host request deassertion for "Last Data Register" write[5,8,10]	$(2.5 \times T_C) + 5$	Note 11	ns
63	Minimum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) deassertion to HREQ assertion.	$(4.0 \times T_C) + 5.0$	Note 11	ns
64	Maximum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) assertion to HREQ deassertion	$(3.5 \times T_C) + 5.0$	Note 11	ns

Table 2A-18. Host Interface (HDI16) Timing[1, 2] (Continued)

Number	Characteristics[3]	Expression	Value	Unit

Notes:

1. T_C = 1/ DSPCLK. At 300 MHz, T_C = 3.3 ns
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF
4. The read data strobe is $\overline{\text{HRD}}$/HRD in the dual data strobe mode and $\overline{\text{HDS}}$/HDS in the single data strobe mode.
5. In 64-bit mode, The “last data register” is the register at address $7, which is the last location to be read or written in data transfers. This is RX0/TX0 in the little endian mode (HBE = 0), or RX3/TX3 in the big endian mode (HBE = 1).
6. This timing is applicable only if a read from the “last data register” is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the $\overline{\text{HREQ}}$/HREQ signal.
7. This timing is applicable only if two consecutive reads from one of these registers are executed.
8. The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.
9. The data strobe is host read ($\overline{\text{HRD}}$/HRD) or host write ($\overline{\text{HWR}}$/HWR) in the dual data strobe mode and host data strobe ($\overline{\text{HDS}}$/HDS) in the single data strobe mode.
10. The host request is $\overline{\text{HREQ}}$/HREQ in the single host request mode and $\overline{\text{HRRQ}}$/HRRQ and $\overline{\text{HTRQ}}$/HTRQ in the double host request mode. $\overline{\text{HRRQ}}$/HRRQ is deasserted only when HOTX fifo is empty, $\overline{\text{HTRQ}}$/HTRQ is deasserted only if HORX fifo is full (treat as level Host Request).
11. Compute the value using the expression.

Figure 2A-8 and **Figure 2A-9** show HDI16 read signal timing. **Figure 2A-10** and **Figure 2A-11** show HDI16 write signal timing.

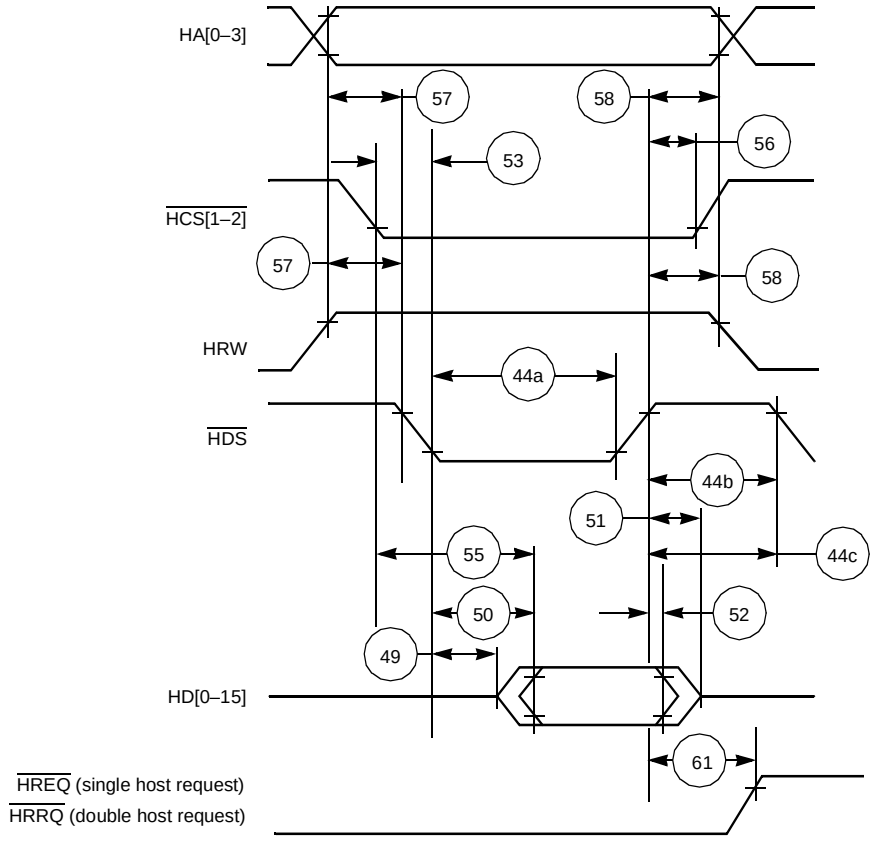


Figure 2A-8. Read Timing Diagram, Single Data Strobe

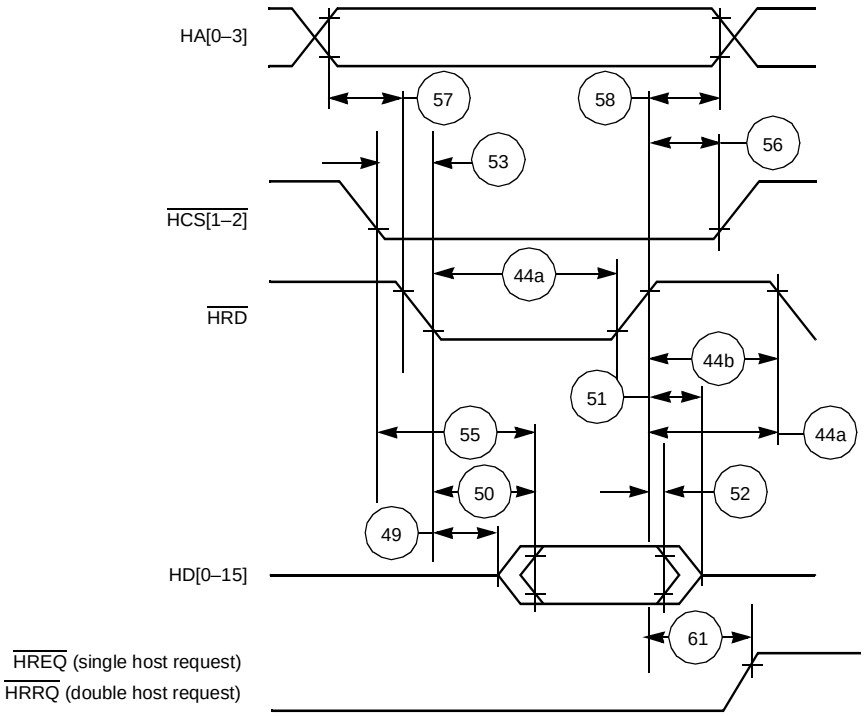


Figure 2A-9. Read Timing Diagram, Double Data Strobe

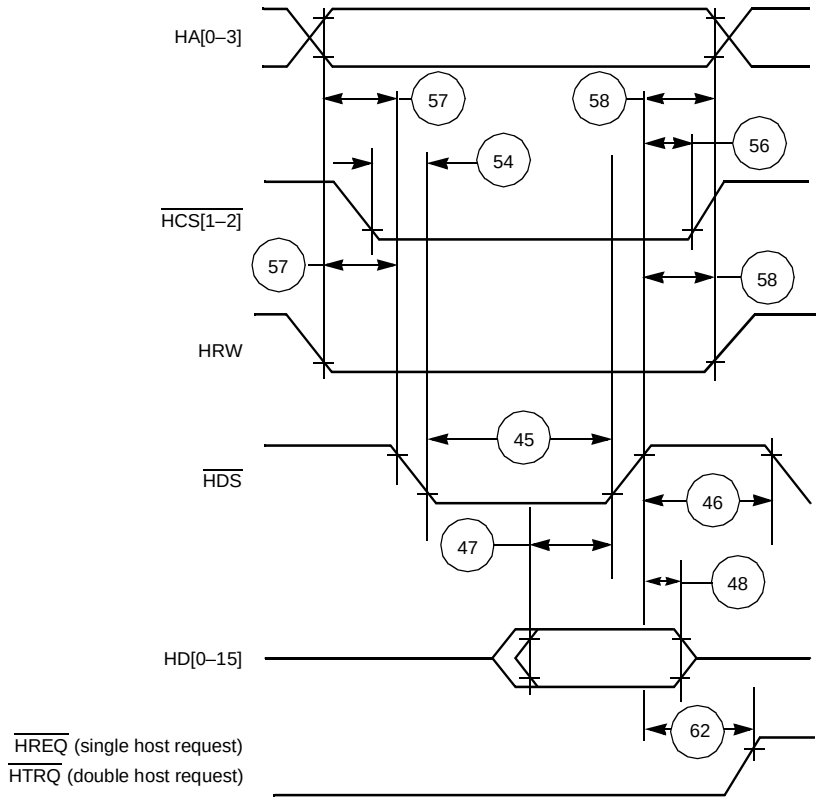


Figure 2A-10. Write Timing Diagram, Single Data Strobe

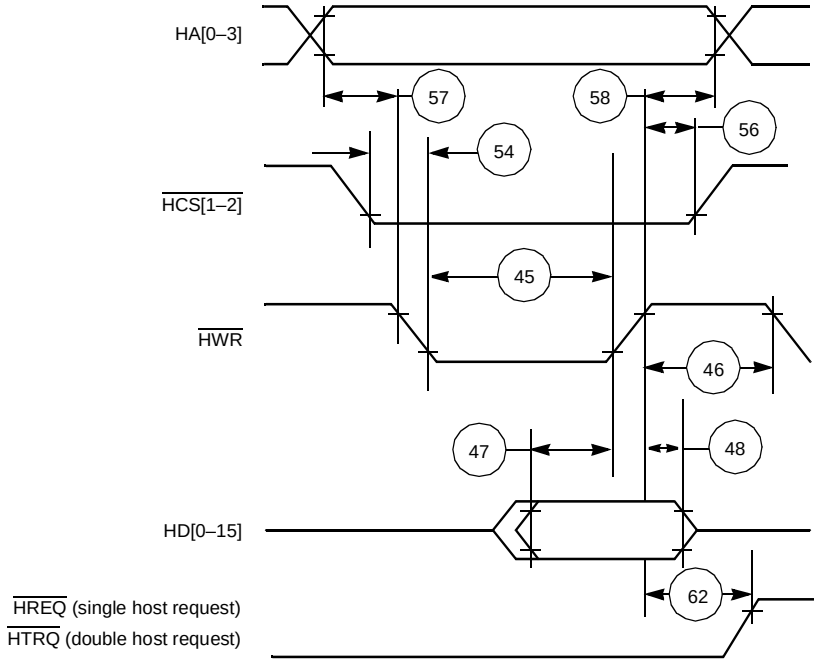


Figure 2A-11. Write Timing Diagram, Double Data Strobe

Figure 2A-12 shows Host DMA read timing.

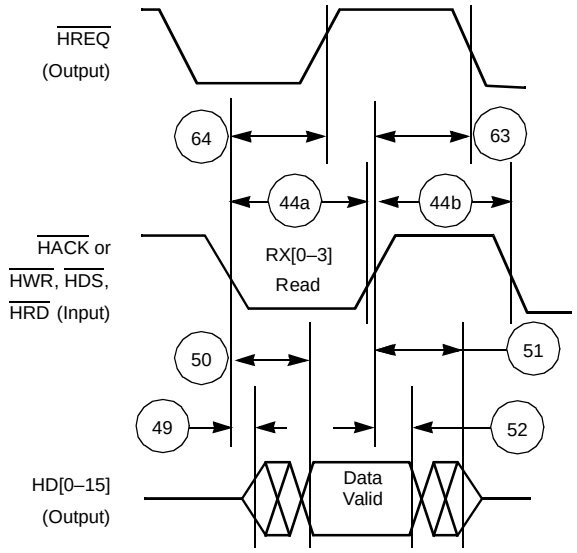


Figure 2A-12. Host DMA Read Timing Diagram

Figure 2A-13 shows Host DMA write timing.

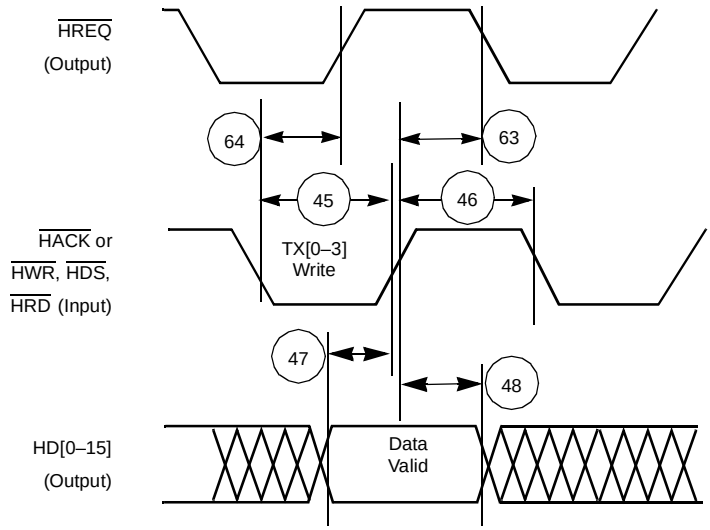


Figure 2A-13. Host DMA Write Timing Diagram

2A.7.5 CPM Timings

Table 2A-19. CPM Input Characteristics

No.	Characteristic	Typical	Unit
16	FCC input setup time before low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 10 5	 ns ns
17	FCC input hold time after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 0 3	 ns ns
18	SCC/SMC/SPI/I^2C input setup time before low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 20 5	 ns ns
19	SCC/SMC/SPI/I^2C input hold time after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 0 5	 ns ns
20	TDM input setup time before low-to-high serial clock transition	20	ns
21	TDM input hold time after low-to-high serial transition	20	ns
22	PIO/TIMER/DMA input setup time before low-to-high serial clock transition	10	ns
23	PIO/TIMER/DMA input hold time after low-to-high serial clock transition	3	ns
Note:	FCC, SCC, SMC, SPI, I^2C are Non-Multiplexed Serial Interface signals.		

Table 2A-20. CPM Output Characteristics

No.	Characteristic	Min	Max	Unit
36	FCC output delay after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial input clock)	 0 2	 6 18	 ns ns
38	SCC/SMC/SPI/I^2C output delay after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial input clock)	 0 0	 20 30	 ns ns
40	TDM output delay after low-to-high serial clock transition	5	35	ns
42	PIO/TIMER/DMA output delay after low-to-high serial clock transition	1	14	ns
Note:	FCC, SCC, SMC, SPI, I^2C are Non-Multiplexed Serial Interface signals.			

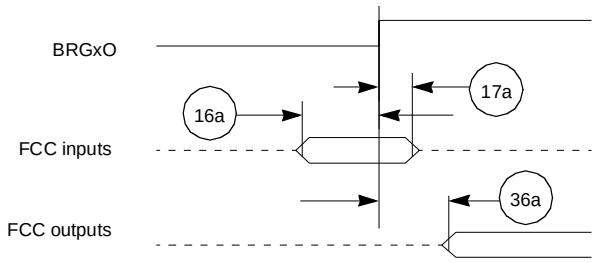


Figure 2A-14. FCC Internal Clock Diagram

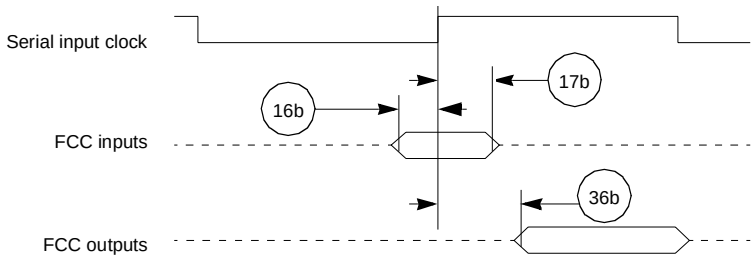


Figure 2A-15. FCC External Clock Diagram

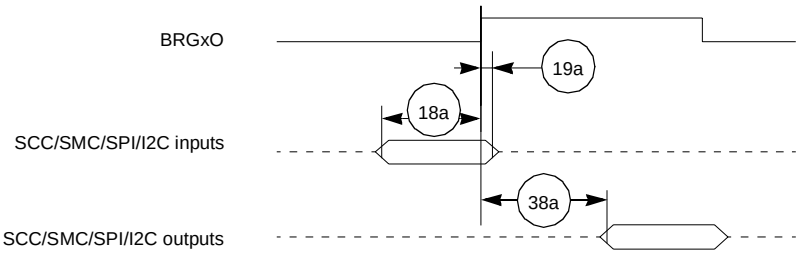


Figure 2A-16. SCC/SMC/SPI/I^2C Internal Clock Diagram

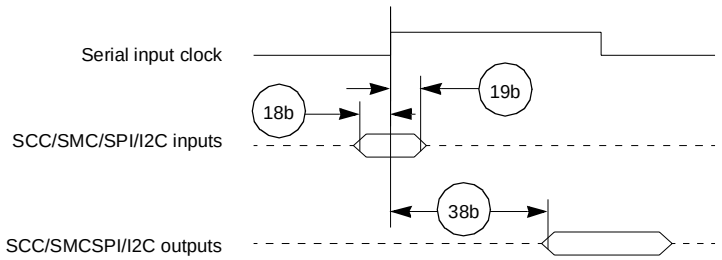


Figure 2A-17. SCC/SMC/SPI/I^{2}C External Clock Diagram

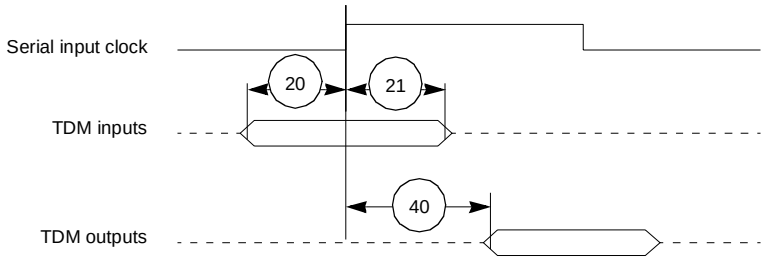


Figure 2A-18. TDM Signal Diagram

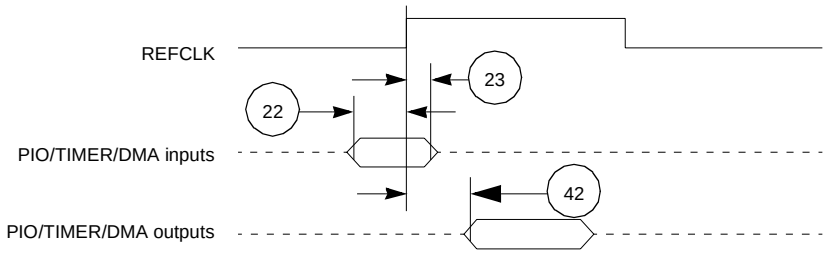


Figure 2A-19. PIO, Timer, and DMA Signal Diagram

Note: The timing values listed are preliminary and refer to minimum system timing requirements. Actual implementation requires conformance to the specific protocol requirements. Refer to **Chapter 1** to identify the specific input and output signals associated with the referenced internal controllers and supported communication protocols. For example, FCC1 supports ATM/Utopia operation in slave mode, multi-PHY master direct polling mode, and multi-PHY master multiplexed polling mode and each of these modes supports its own set of signals; the direction (input or output) of some of the shared signal names depends on the selected mode.

2A.7.6 JTAG Signals

Table 2A-21. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
500	TCK frequency of operation	0.0	40.0	MHz
501	TCK cycle time	25.0	—	ns
502	TCK clock pulse width measured at 1.6 V	12.5	—	ns
503	TCK rise and fall times	0.0	3.0	ns
508	TMS, TDI data set-up time	6.0	—	ns
509	TMS, TDI data hold time	3.0	—	ns
510	TCK low to TDO data valid	0.0	15.0	ns
511	TCK low to TDO high impedance	0.0	5.0	ns
512	$\overline{\text{TRST}}$ assert time	100.0	—	ns
513	$\overline{\text{TRST}}$ set-up time to TCK low	40.0	—	ns

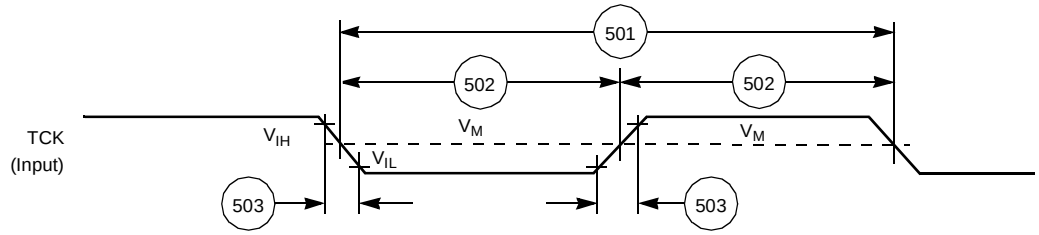


Figure 2A-20. Test Clock Input Timing Diagram

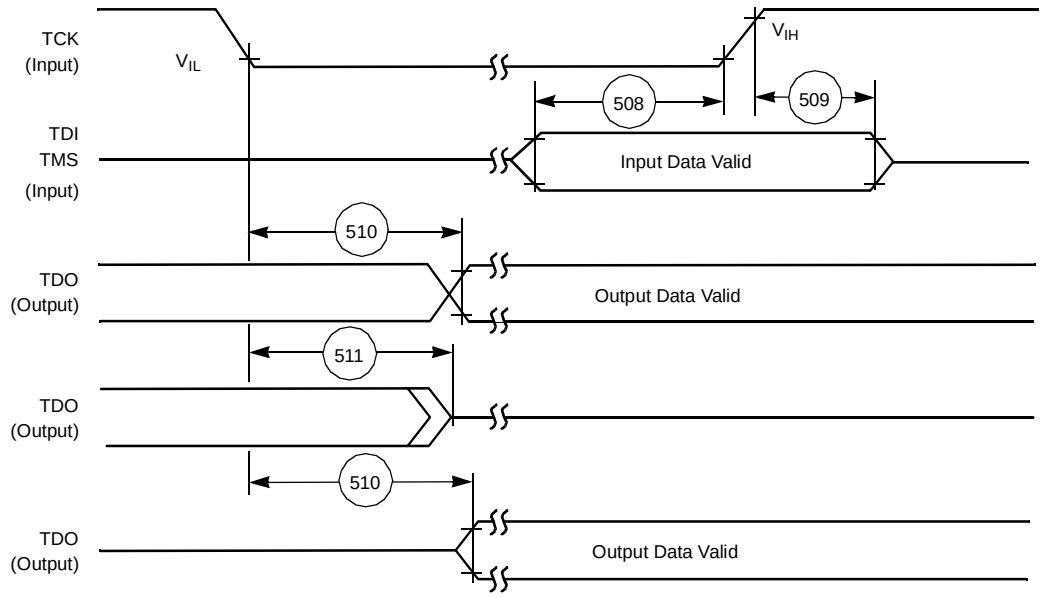


Figure 2A-21. Test Access Port Timing Diagram

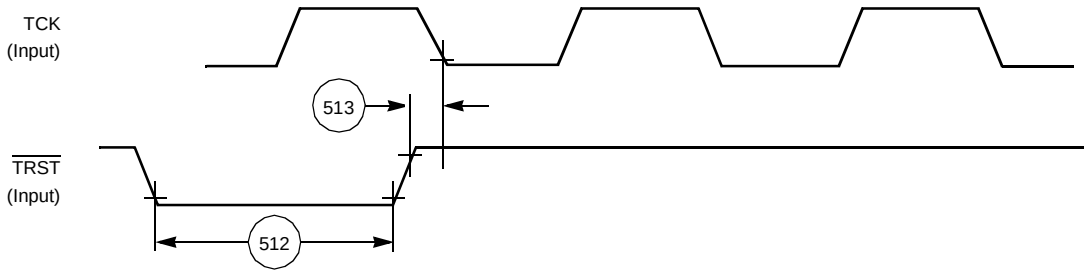


Figure 2A-22. $\overline{\text{TRST}}$ Timing Diagram

Chapter 2B

Specifications (mask set 1K87M)

2B.1 Introduction

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MSC8101 communications processor, mask set 1K87M. For additional information, see the *MSC8101 Reference Manual*.

Note: The MSC8101 electrical specifications are preliminary and many are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after thorough characterization and device qualifications have been completed.

2B.2 Absolute Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2B-1 describes the maximum electrical ratings for the MSC8101.

Table 2B-1. Absolute Maximum Ratings[2]

Rating	Symbol	Value	Unit
Core supply voltage[3]	V_{DD}	–0.2 to 1.7	V
PLL supply voltage[3]	V_{CCSYN}	–0.2 to 1.7	V
I/O supply voltage[3]	V_{DDH}	–0.2 to 3.6	V
Input voltage[3]	V_{IN}	(GND – 0.2) to 3.6	V
Maximum operating temperature range[4]	T_J	–40 to 120	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 2B-2.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. The input voltage must not exceed the I/O supply V_{DDH} by more than 2.5 V at any time, including during power-on reset. In turn, V_{DDH} can exceed V_{DD}/V_{CCSYN} by more than 3.3 V during power-on reset, but for no more than 100 ms. V_{DDH} should not exceed V_{DD}/V_{CCSYN} by more than 2.1 V during normal operation. V_{DD}/V_{CCSYN} must not exceed V_{DDH} by more than 0.4 V at any time, including during power-on reset. See **Section 4.2**, *Electrical Design Considerations*, on page 4-2 for more information.
4. **Section 4.1**, *Thermal Design Considerations*, on page 4-1 includes a formula for computing the chip junction temperature (T_J).

2B.3 Recommended Operating Conditions

Table 2B-2 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2B-2. Recommended Operating Conditions

Rating	Symbol	Value	Unit
SC140 Core supply voltage	V_{DD}	250/275 MHz: 1.5 to 1.7 300 MHz: 1.55 to 1.7	V V
PLL supply voltage	V_{CCSYN}	250/275 MHz: 1.5 to 1.7 300 MHz: 1.55 to 1.7	V V
I/O supply voltage	V_{DDH}	3.135 to 3.465	V
Input voltage	V_{IN}	–0.2 to V_{DDH} + 0.2	V
Operating temperature range	T_J	250/275 MHz: –40 to 105 300 MHz: –40 to 75	°C °C

2B.4 Thermal Characteristics

Table 2B-3 describes thermal characteristics of the MSC8101.

Table 2B-3. Thermal Characteristics

Characteristic	Symbol	Lidded FC-PBGA 17 × 17mm	Unit
Junction-to-ambient[1, 2]	$R_{\theta JA}$ or θ_{JA}	26	°C/W
Junction-to-board (bottom)[3]	$R_{\theta JB}$ or θ_{JB}	9.5	°C/W
Junction-to-case (top)[4]	$R_{\theta JC}$ or θ_{JC}	0.8	°C/W

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and EIA/JESD51-2 with the single layer (1s) board horizontal.
3. Thermal resistance between the die and the printed circuit board per JESD 51-8.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for case temperature.
5. Numbers based on simulations. Actual values TBD.

See **Section 4.1**, *Thermal Design Considerations*, on page 4-1 for details on these characteristics.

2B.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8101. The measurements in **Table 2B-4** assume the following system conditions:

- T_J = 0 – 100 °C
- V_{DD} = 1.6 V ± 5% V_{DC}
- V_{DDH} = 3.3 V ± 5% V_{DC}
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal V_{DDH} and V_{DD} or both V_{DDH} and V_{DD} must vary in the same direction (for example, both V_{DDH} and V_{DD} vary by ± 5 percent).

Table 2B-4. DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.5	3.465	V
CLKIN input low voltage[1]	V_{ILC}	GND	0.8	V
Input leakage current, V_{IN} = V_{DDH}	I_{IN}	—	10	µA
Tri-state (high impedance off state) leakage current, V_{IN} = V_{DDH}	I_{OZ}	—	10	µA
Signal low input current, V_{IL} = 0.4 V	I_L	—	–4.0	mA
Signal high input current, V_{IH} = 2.0 V	I_H	—	4.0	mA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.4	—	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0.4	V

Notes:
1. The optimum CLKIN duty cycle is obtained when: V_{ILC} = V_{DDH} – V_{IHC}.

Table 2B-5. Typical Power Dissipation

Characteristic	Symbol	Typical	Unit
Core power dissipation at 300 MHz	P_{CORE}	350	mW
CPM power dissipation at 200 MHz	P_{CPM}	320	mW
SIU power dissipation at 100 MHz	P_{SIU}	80	mW
Core leakage power	P_{LCO}	3	mW
CPM leakage power	P_{LCP}	6	mW
SIU leakage power	P_{LSI}	2	mW

2B.6 Clock Configuration

The following sections provide a general description of clock configuration.

2B.6.1 Valid Clock Modes

Table 2B-6 shows the maximum frequency values for each rated core frequency (250, 275, or 300 MHz). The user must ensure that maximum frequency values are not exceeded.

Table 2B-6. Maximum Frequencies

Characteristic	Maximum Frequency in MHz		
Core Frequency	250	275	300
CPM Frequency (CPMCLK)	166.67	183.33	200
Bus Frequency (BCLK)	83.33	91.67	100
Serial Communication Controller Clock Frequency (SCLK)	83.33	91.67	100
Baud Rate Generator Clock Frequency (BRGCLK)	83.33	91.67	100
External Clock Output Frequency (CLKOUT)	83.33	91.67	100

Six bit values map the MSC8101 clocks to one of the valid configuration mode options. Each option determines the CLKIN, SC140 core, system bus, SCC clock, CPM, and CLKOUT frequencies. The six bit values are derived from three dedicated input pins (MODCK[1–3]) and three bits from the hard reset configuration word (MODCK_H). To configure the SPLL pre-division factor, SPLL multiplication factor, and the frequencies for the SC140 core, SCC clocks, CPM parallel I/O ports, and system buses, the MODCK[1–3] pins are sampled and combined with the MODCK_H values when the internal power-on reset (internal $\overline{\text{PORESET}}$) is deasserted. Clock configuration changes only when the internal $\overline{\text{PORESET}}$ signal is deasserted. The following factors are configured:

- SPLL pre-division factor (SPLL PDF)
- SPLL multiplication factor (SPLL MF)
- Bus post-division factor (Bus DF)
- CPM division factor (CPM DF)
- Core division factor (Core DF)
- CPLL pre-division factor (CPLL PDF)
- CPLL multiplication factor (CPLL MF)

The SCC division factor (SCC DF) is fixed at 4. The BRG division factor (BRG DF) is configured through the System Clock Control Register (SCCR) and can be 4, 16 (default after reset), 64, or 256.

Note: Refer to *AN2306/D Clock Mode Selection for MSC8101 Mask Set 1K87M* for details on clock configuration.

2B.6.2 Clocks Programming Model

This section describes the clock registers in detail. The registers discussed are as follows:

- System Clock Control Register (SCCR)
- System Clock Mode Register (SCMR)

2B.6.2.1 System Clock Control Register

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	—															
TYPE	Reserved															
RESET	—															
Bit	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
	—											CLKODIS	—		DFBRG	
TYPE	Reserved											R/W	Reserved		R/W	
RESET	—											0	—		0	1

Figure 2B-1. System Clock Control Register (SCCR)—**0x10C80**

The SCCR is memory-mapped into the SIU register map of the MSC8101.

Table 2B-7. SCCR Bit Descriptions

Name Bit No.	Defaults		Description	Settings	
	POWERSET	Hard Reset			
— 0–26	—	—	Reserved. Write to 0 fro future compatibility.		
CLKODIS 27	0	Unaffected	**CLKOUT Disable** Disables the CLKOUT signal. The value of CLKOUT when disabled is indeterminate (can be 1 or 0).	0 1	CLKOUT enabled (default) CLKOUT disabled
— 28–29	—	—	Reserved. Write to 0 fro future compatibility.		
DFBRG 30–31	01	Unaffected	**Division Factor for the BRG Clock** Defines the BRGCLK frequency. Changing this value does not result in a loss of lock condition.	00 01 10 11	Divide by 4 Divide by 16 (default value) Divide by 64 Divide by 256

2B.6.2.2 System Clock Mode Register

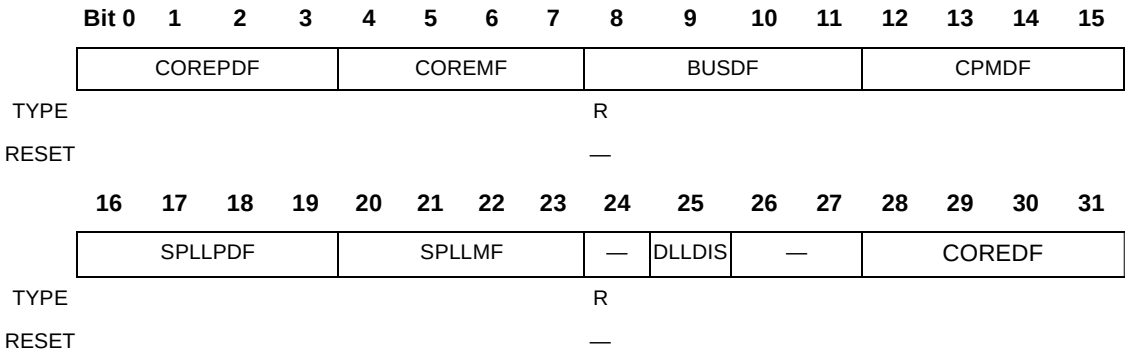


Figure 2B-2. System Clock Mode Register (SCMR)—**0x10C88**

SCMR is a read-only register that is updated during power-on reset (PORESET) and provides the mode control signals to the PLLs, DLL, and clock logic. This register reflects the currently defined configuration settings. For details of the available setting options, see *AN2306/D*.

Table 2B-8. SCMR Field Descriptions

Name Bit No.	Defaults		Description	Settings
	PORESET	**Hard Reset**		
COREPDF 0–3	Configuration Pins	Unaffected	**Core PLL Pre-Division Factor**	0000 CPLL PDF = 1 0001 CPLL PDF = 2 0010 CPLL PDF = 3 0011 CPLL PDF = 4 All other combinations not used.
COREMF 4–7	Configuration Pins	Unaffected	**Core Multiplication Factor**	0101 CPLL MF = 10 0110 CPLL MF = 12 0111 CPLL MF = 14 All other combinations not used.
BUSDF 8–11	Configuration Pins	Unaffected	**60x-compatible Bus Division Factor**	0001 Bus DF = 2 0010 Bus DF = 3 0011 Bus DF = 4 0100 Bus DF = 5 0101 Bus DF = 6 All other combinations not used.
CPMDF 12–15	Configuration Pins	Unaffected	**CPM Division Factor**	0000 CPM DF = 1 0001 CPM DF = 2 0010 CPM DF = 3 All other combinations not used.
SPLLPDF 16–19	Configuration Pins	Unaffected	**SPLL Pre-Division Factor**	0000 SPLL PDF = 1 0001 SPLL PDF = 2 0010 SPLL PDF = 3 0011 SPLL PDF = 4 0100 SPLL PDF = 5 0101 SPLL PDF = 6 All other combinations not used

Table 2B-8. SCMR Field Descriptions (Continued)

Name Bit No.	Defaults		Description	Settings
	PORESET	**Hard Reset**		
SPLLMF 20–23	Configuration Pins	Unaffected	**SPLL Multiplication Factor**	0101 SPLL MF = 10 0110 SPLL MF = 12 0111 SPLL MF = 14 1000 SPLL MF = 16 1001 SPLL MF = 18 1010 SPLL MF = 20 1011 SPLL MF = 22 1100 SPLL MF = 24 1101 SPLL MF = 26 1110 SPLL MF = 28 1111 SPLL MF = 30 All other combinations not used
— 24	—	—	Reserved	
DLLDIS 25	Configuration Pins	Unaffected	**DLL Disable**	0 DLL operation is enabled 1 DLL is disabled
— 26–27	—	—	Reserved	
COREDF 28–31	Configuration Pins	Unaffected	**Core Division Factor**	0000 CORE DF = 1 0001 CORE DF = 2 0010 CORE DF = 3 0011 CORE DF = 4 0100 CORE DF = 5 0101 CORE DF = 6 All other combinations not used.

2B.7 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. AC timings are based on a 50 pF load, except where noted otherwise, and 50 Ω transmission line.

2B.7.1 Clocking and Timing Characteristics

Table 2B-9. System Clock Parameters

Characteristic	Minimum	Maximum	Unit
Phase Jitter between BCLK and DLLIN	—	0.5	ns
CLKIN frequency[1,2]	18	75	MHz
CLKIN slope	—	5	ns
DLLIN slope	—	2	ns
CLKOUT frequency jitter	—	(0.01/CLKOUT) + CLKIN jitter	ns
Delay between CLKOUT and DLLIN	—	5	ns

Notes: **1.** Low CLKIN frequency causes poor PLL performance. Choose a CLKIN frequency high enough to keep the frequency after the predivider (SPLLMFCLK) higher than 18 MHz.
2. CLKIN should have a 50% ± 5% duty cycle.

Table 2B-10. Clock Ranges

Clock	Symbol	Maximum Rated Core Frequency			
		All	Max. Values for SC140 Clock Rating of:		
		Min	250 MHz	275 MHz	300 MHz
Input Clock	CLKIN	18 MHz	62.5	68.75 MHz	75 MHz
SPLL MF Clock	SPLLMFCLK	18 MHz	20.83	22.9 MHz	25 MHz
Bus	BCLK	18 MHz	83.3 MHz	91.67 MHz	100 MHz
Output	CLKOUT	43.2 MHz	83.3 MHz	91.67 MHz	100 MHz
Serial Communications Controller	SCLK	18 MHz	83.3 MHz	91.67 MHz	100 MHz
Communications Processor Module	CPMCLK	36 MHz	166.7 MHz	183.3 MHz	200 MHz
SC140 Core	DSPCLK	72 MHz	250 MHz	275 MHz	300 MHz
Baud Rate Generator • For BRG DF = 4 • For BRG DF = 16 (default) • For BRG DF = 64 • For BRG DF = 256	BRGCLK	 36 MHz 9 MHz 2.25 MHz 562.5 KHz	 83.3 MHz 20.83 MHz 5.21 MHz 1.3 MHz	 91.67 MHz 22.91 MHz 5.73 MHz 1.43 MHz	 100 MHz 25 MHz 6.25 MHz 1.56 MHz

2B.7.2 Reset Timing

The MSC8101 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)

Asserting an external $\overline{\text{PORESET}}$ causes concurrent assertion of an internal $\overline{\text{PORESET}}$ signal, $\overline{\text{HRESET}}$, and $\overline{\text{SRESET}}$. When the external $\overline{\text{PORESET}}$ signal is deasserted, the MSC8101 samples several configuration pins:

- $\overline{\text{RSTCONF}}$—determines whether the MSC8101 is a master (0) or slave (1) device
- DBREQ—determines whether to operate in normal mode (0) or invoke the SC140 debug mode (1)
- HPE—disable (0) or enable (1) the host port (HDI16)
- BTM[0–1]—boot from external memory (00) or the HDI16 (01)

All these reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the last sources to cause a reset. **Table 2B-11** describes reset causes.

Table 2B-11. Reset Causes

Name	Direction	Description
Power-on reset ($\overline{\text{PORESET}}$)	Input	$\overline{\text{PORESET}}$ initiates the power-on reset flow that resets all the MSC8101s and configures various attributes of the MSC8101, including its clock mode.
Hard reset ($\overline{\text{HRESET}}$)	Input/Output	The MSC8101 can detect an external assertion of $\overline{\text{HRESET}}$ only if it occurs while the MSC8101 is not asserting reset. During $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ is asserted. $\overline{\text{HRESET}}$ is an open-drain pin.
Soft reset ($\overline{\text{SRESET}}$)	Input/Output	The MSC8101 can detect an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8101 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin.

2B.7.2.1 Reset Operation

The reset control logic determines the cause of a reset, synchronizes it if necessary, and resets the appropriate logic modules. The memory controller, system protection logic, interrupt controller, and parallel I/O pins are initialized only on hard reset. Soft reset initializes the internal logic while maintaining the system configuration. The MSC8101 has three mechanisms for reset configuration: host reset configuration, hardware reset configuration, and reduced reset configuration.

2B.7.2.2 Power-On Reset Flow

Asserting the $\overline{\text{PORESET}}$ external pin initiates the power-on reset flow. $\overline{\text{PORESET}}$ should be asserted externally for at least 16 input clock cycles after external power to the MSC8101 reaches at least 2/3 V_{CC}. As **Table 2B-12** shows, the MSC8101 has five configuration pins, four of which are multiplexed with the SC140 core EONCE Event (EE[0–1], EE[4–5]) pins and the fifth of which is the $\overline{\text{RSTCONF}}$ pin. These pins are sampled at the rising edge of $\overline{\text{PORESET}}$. In addition to these configuration pins, three (MODCK[1–3]) pins are sampled by the MSC8101. The signals on these pins and the MODCK_H value in the Hard Reset Configuration Word determine the PLL locking mode, by defining the ratio between the DSP clock, the bus clocks, and the CPM clock frequencies.

Table 2B-12. External Configuration Signals

Pin	Description	Settings
RSTCONF	**Reset Configuration** Input line sampled by the MSC8101 at the rising edge of PORESET.	0 Reset Configuration Master. 1 Reset Configuration Slave.
DBREQ/ EE0	**EONCE Event Bit 0** Input line sampled after SC140 core PLL locks. Holding EE0 high when PORESET is deasserted puts the SC140 core into Debug mode.	0 SC140 core starts the normal processing mode after reset. 1 SC140 core enters Debug mode immediately after reset.
HPE/EE1	**Host Port Enable** Input line sampled at the rising edge of PORESET. If asserted, the Host port is enabled, the system data bus is 32-bit wide, and the Host *must* program the reset configuration word.	0 Host port disabled (hardware reset configuration enabled). 1 Host port enabled.
BTM[0–1]/ EE[4–5]	**Boot Mode** Input lines sampled at the rising edge of PORESET, which determine the MSC8101 Boot mode.	00 MSC8101 boots from external memory. 01 MSC8101 boots from HDI16. 10 Reserved. 11 Reserved.

Table 2B-13. Reset Timing

No.	Characteristics	Expression	Min	Max	Unit
1	Required external PORESET duration minimum • CLKIN = 18 MHz • CLKIN = 75 MHz	16 / CLKIN	 888.8 213.3	 — —	 ns ns
2	Delay from deassertion of external PORESET to deassertion of internal PORESET • CLKIN = 18 MHz • CLKIN = 75 MHz	1024 / CLKIN	 56.89 13.65		 µs µs
3	Delay from deassertion of internal PORESET to SPLL lock • SPLLMFCLK = 18 MHz • SPLLMFCLK = 25 MHz	800 / SPLLMFCLK	 44.4 32.0		 µs µs
4	Delay from SPLL lock to DLL lock • DLL enabled — BCLK = 18 MHz — BCLK = 75 MHz • DLL disabled	 3073 / BLCK —	 170.72 40.97 0.0		 µs µs ns
5	Delay from SPLL lock to HRESET deassertion • DLL enabled — BCLK = 18 MHz — BCLK = 75 MHz • DLL disabled — BCLK = 18 MHz — BCLK = 75 MHz	 3585 / BLCK 512 / BLCK	 199.17 47.5 28.4 6.83		 µs µs µs µs
6	Delay from SPLL lock to SRESET deassertion • DLL enabled — BCLK = 18 MHz — BCLK = 75 MHz • DLL disabled — BCLK = 18 MHz — BCLK = 75 MHz	 3588 / BLCK 515 / BLCK	 199.33 47.84 28.61 6.87		 µs µs µs µs

Note: Value given for lowest possible CLKIN frequency 18 MHz to ensure proper initialization of reset sequence.

2B.7.2.3 Host Reset Configuration

Host reset configuration allows the host to program the reset configuration word via the Host port after PORESET is deasserted, as described in the *MSC8101 Reference Manual*. The MSC8101 samples the signals described in **Table 2B-12** one the rising edge of PORESET when the signal is deasserted.

If HPE is sampled high, the host port is enabled. In this mode the RSTCONF pin *must* be pulled up. The device extends the internal PORESET until the host programs the reset configuration word register. The host must write four 8-bit half-words to the Host Reset Configuration Register address to program the reset configuration word, which is 32 bits wide. For more information, see the *MSC8101 Reference Manual*. The reset configuration word is programmed before the internal PLL and DLL in the MSC8101 are locked. The host must program it after the rising edge of the PORESET input. In this mode, the host must have its own clock that does not depend on the MSC8101 clock. After the PLL and DLL are locked, HRESET remains asserted for another 512 bus clocks and is then released. The SRESET is released three bus clocks later (see **Figure 2B-3**).

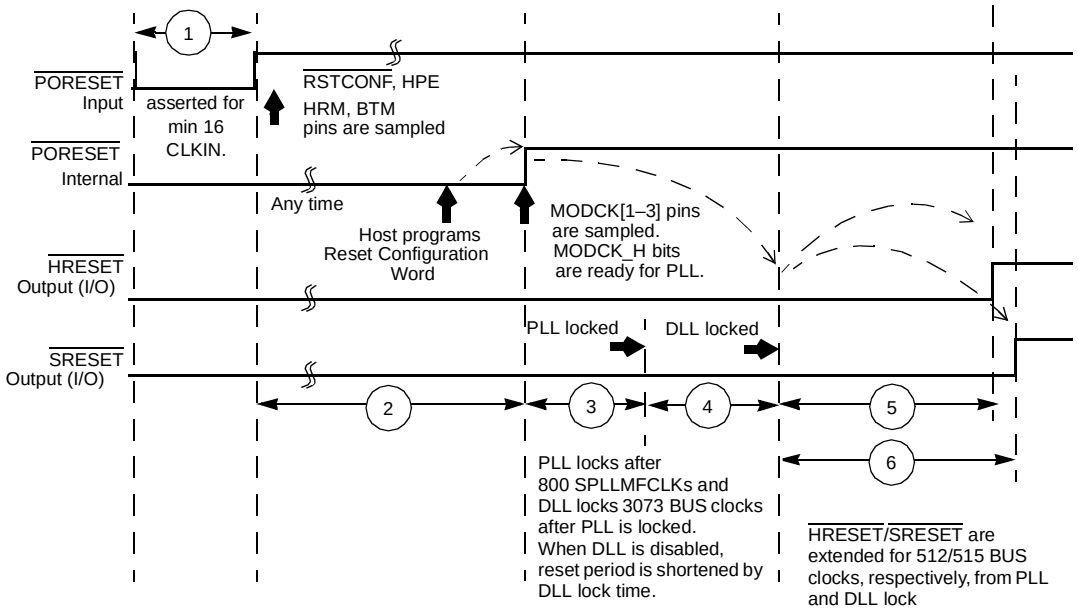


Figure 2B-3. Host Reset Configuration Timing

2B.7.2.4 Hardware Reset Configuration

Hardware reset configuration is enabled if HPE is sampled low at the rising edge of PORESET. The value driven on RSTCONF while PORESET changes from assertion to deassertion determines the MSC8101 configuration. If RSTCONF is deasserted (driven high) while PORESET changes, the MSC8101 acts as a configuration slave. If RSTCONF is asserted (driven low) while PORESET changes, the MSC8101 acts as a configuration master. **Section 2B.7.2.4**, *Hardware Reset Configuration*, explains the configuration sequence and the terms “configuration master” and “configuration slave.”

Directly after the deassertion of PORESET and choice of the reset operation mode as configuration master or configuration slave, the MSC8101 starts the configuration process. The MSC8101 asserts HRESET and SRESET throughout the power-on reset process, including configuration. Configuration takes 1024 CLOCKIN cycles, after which MODCK[1–3] are sampled to determine the MSC8101’s working mode.

Next, the MSC8101 halts until the SPLL locks. The SPLL locks according to MODCK[1–3], which are sampled, and to MODCK_H taken from the Reset Configuration Word. SPLL locking time is 800 reference clocks, which is the clock at the output of the SPLL Pre-divider. After the SPLL is locked, all the clocks to the MSC8101 are enabled. If the DLLDIS bit in the reset configuration word is reset, the DLL starts the locking process after the SPLL is locked. During PLL and DLL locking, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are asserted. $\overline{\text{HRESET}}$ remains asserted for another 512 BUS clocks and is then released. The $\overline{\text{SRESET}}$ is released three bus clocks later. If the DLLDIS bit in the reset configuration word is set, the DLL is bypassed and there is no locking process, thus saving the DLL locking time. **Figure 2B-4** shows the power-on reset flow.

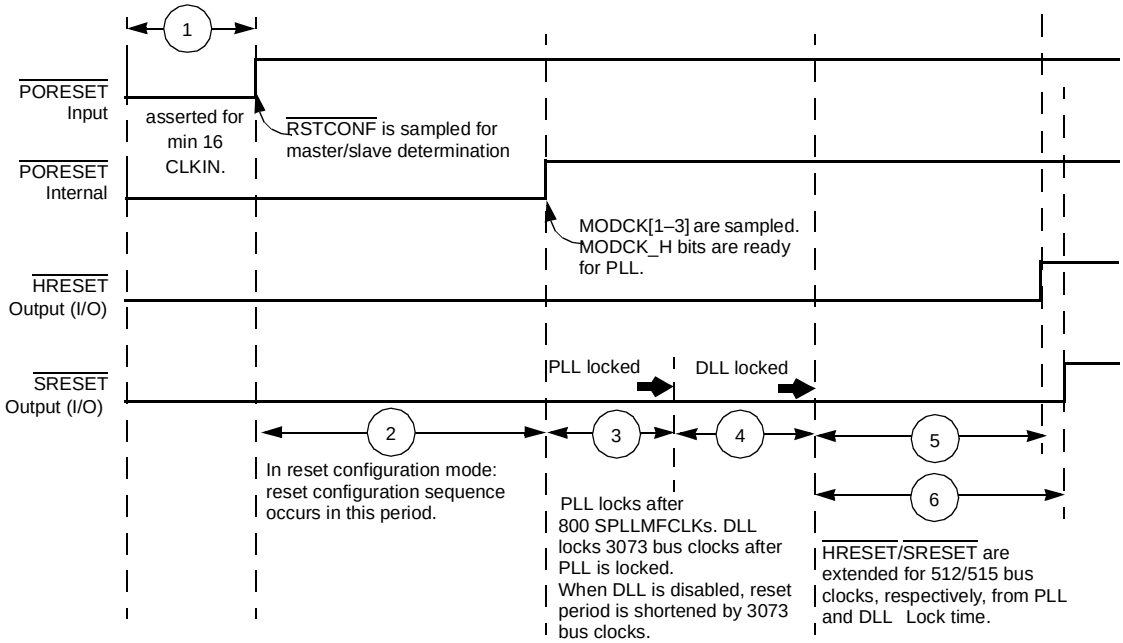


Figure 2B-4. Hardware Reset Configuration Timing

2B.7.3 System Bus Access Timing

2B.7.3.1 Core Data Transfers

Generally, all MSC8101 bus and system output signals are driven from the rising edge of the reference clock (REFCLK), which is DLLIN or, if the DLL is disabled, CLKOUT. Memory controller signals, however, trigger on four points within a REFCLK cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of REFCLK (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 2B-14** shows.

Table 2B-14. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of REFCLK)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 REFCLK	1/2 REFCLK	3/4 REFCLK
1:2.5	3/10 REFCLK	1/2 REFCLK	8/10 REFCLK
1:3.5	4/14 REFCLK	1/2 REFCLK	11/14 REFCLK

Figure 2B-5 is a graphical representation of **Table 2B-14**.

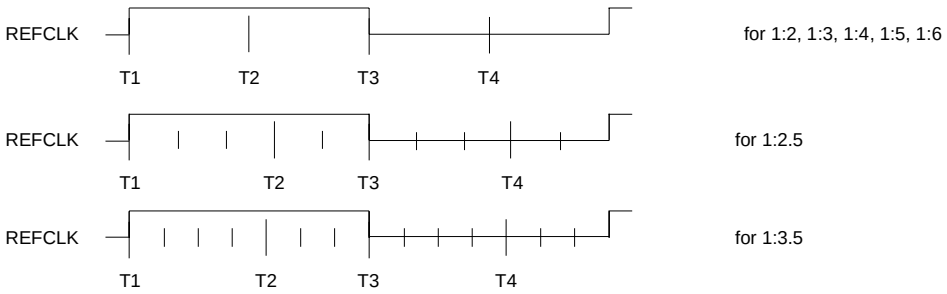


Figure 2B-5. Internal Tick Spacing for Memory Controller Signals

Note: The UPM machine and GPCM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. SDRAM machine outputs change only on the REFCLK rising edge.

Table 2B-15. AC Timing for SIU Inputs

No.	Characteristic	Value[2]	Units
10	Hold time for all signals after the 50% level of the REFCLK rising edge	0.5	ns
11a	$\overline{ABB}$/$\overline{AACK}$ setup time before the 50% level of the REFCLK rising edge	3.0	ns
11b	$\overline{DBG}$/$\overline{DBB}$/$\overline{BR}$/$\overline{TC}$ setup time before the 50% level of the REFCLK rising edge	3.0	ns
11c	ARTRY setup time before the 50% level of the REFCLK rising edge	7.0	ns
11d	$\overline{TA}$ setup time before the 50% level of the REFCLK rising edge • Pipeline mode • Non-pipeline mode	 4.0 4.5	 ns ns
11e	$\overline{TEA}$ setup time before the 50% level of the REFCLK rising edge • Pipeline mode • Non-pipeline mode	 5.5 6.0	 ns ns
11f	$\overline{PSDVAL}$ setup time before the 50% level of the REFCLK rising edge • Pipeline mode • Non-pipeline mode	 2.5 3.0	 ns ns
11g	$\overline{TS}$ setup time before the 50% level of the REFCLK rising edge	4.5	ns
11h	$\overline{BG}$ setup time before the 50% level of the REFCLK rising edge	4.0	ns
12	Data bus setup time before the 50% level of the REFCLK rising edge in Normal • Pipeline mode • Non-pipeline mode	 5.5 5.5	 ns ns
13	Data bus setup time before the 50% level of the REFCLK rising edge in ECC and PARITY modes	9.0	ns
14	DP setup time before the 50% level of the REFCLK rising edge • Pipeline mode • Non-pipeline mode	 4.0 4.5	 ns ns
15a	Address bus setup time before the 50% level of the REFCLK rising edge • Extra cycle mode (SIUBCR[EXDD] = 0) • Non-extra cycle mode (SIUBCR[EXDD] = 1)	 3.0 5.0	 ns ns
15b	Address attributes: TT/$\overline{TBST}$/TSIZ/$\overline{GBL}$ setup time before the 50% level of the REFCLK rising edge • Extra cycle mode (SIUBCR[EXDD] = 0) • Non-extra cycle mode (SIUBCR[EXDD] = 1)	 3.0 5.0	 ns ns
16[1]	PUPMWAIT/$\overline{IRQ}$ signals Setup time before the 50% level of the REFCLK rising edge	3.0	ns

Notes:
1. The setup time for these signals is for synchronous operation. Any setup time can be used for asynchronous operation.
2. Input specifications are measured from the 50% level of the rising edge of REFCLK to the 50% level of the signal. Timings are measured at the pin.

Table 2B-16. AC Timing for SIU Outputs

No.	Characteristic	Min.	Maximum[2]		Units
			30 pF	50 pF	
31a	$\overline{TA}$ delay from the 50% level of the REFCLK rising edge				
	• Pipeline mode	1.0	5.0	6.5	ns
	• Non-pipeline mode	1.0	6.0	7.5	ns
31b	$\overline{TEA}$ delay from the 50% level of the REFCLK rising edge				
	• Pipeline mode	1.0	4.0	5.5	ns
	• Non-pipeline mode	1.0	5.0	6.0	ns
31c	$\overline{PSDVAL}$ delay from the 50% level of the REFCLK rising edge				
	• Pipeline mode	1.0	6.0	7.5	ns
	• Non-pipeline mode	1.0	6.5	8.0	ns
32a	Address bus delay from the 50% level of the REFCLK rising edge				
	• Multi master mode (SIUBCR[EBM] = 1)	1.0	6.5	8.0	ns
	• Single master mode (SIUBCR[EBM] = 0)	1.0	6.0	7.5	ns
32b	Address attributes: TT/$\overline{TBST}$/TSIZ/$\overline{GBL}$ delay from the 50% level of the REFCLK rising edge	1.0	6.5	8.0	ns
32c	BADDR delay from the 50% level of the REFCLK rising edge	1.0	4.5	6.0	ns
33a	Data bus delay from the 50% level of the REFCLK rising edge				
	• Pipeline mode	1.0	7.0	8.5	ns
	• Non-pipeline mode	1.0	7.5	9.0	ns
33b	DP delay from the 50% level of the REFCLK rising edge				
	• Pipeline mode	1.0	5.0	6.5	ns
	• Non-pipeline mode	1.0	5.5	7.0	ns
34	Memory controller signals/ALE delay from the 50% level of the REFCLK rising edge	1.0	6.0	7.5	ns
35a	$\overline{DBG}$/$\overline{BR}$/$\overline{DBB}$ delay from the 50% level of the REFCLK rising edge	1.0	4.0	5.5	ns
35b	$\overline{AACK}$/$\overline{ABB}$/$\overline{CS}$ delay from the 50% level of the REFCLK rising edge	1.0	5.0	6.5	ns
35c	$\overline{BG}$ delay from the 50% level of the REFCLK rising edge	1.0	4.5	6.0	ns
35d	$\overline{TS}$ delay from the 50% level of the REFCLK rising edge	1.0	4.5	6.0	ns
36	Delay from the 50% level of the REFCLK rising edge for all other signals	1.0	6.5	8.0	ns

Notes:

1. The maximum bus frequency depends on the mode:
- In 60x-compatible mode connected to another MSC8101 device, the frequency is determined by adding the input and output longest timing values, which results in a frequency of 75 MHz for 30 pF output capacitance. In multi-master mode when connected to another MSC8101 device, the frequency is determined by adding the input and output longest timing values, which results in a frequency of 75 MHz for 30 pF output capacitance.
- Certain bus modes, such as non-extra cycle (EXDD = 1), non-pipelined, and ECC/Parity modes, result in slower bus frequencies.
- In single-master mode, the frequency depends on the timing of the devices connected to the MSC8101.

2. Output specifications are measured from the 50% level of the rising edge of REFCLK to the 50% level of the signal. Timings are measured at the pin.

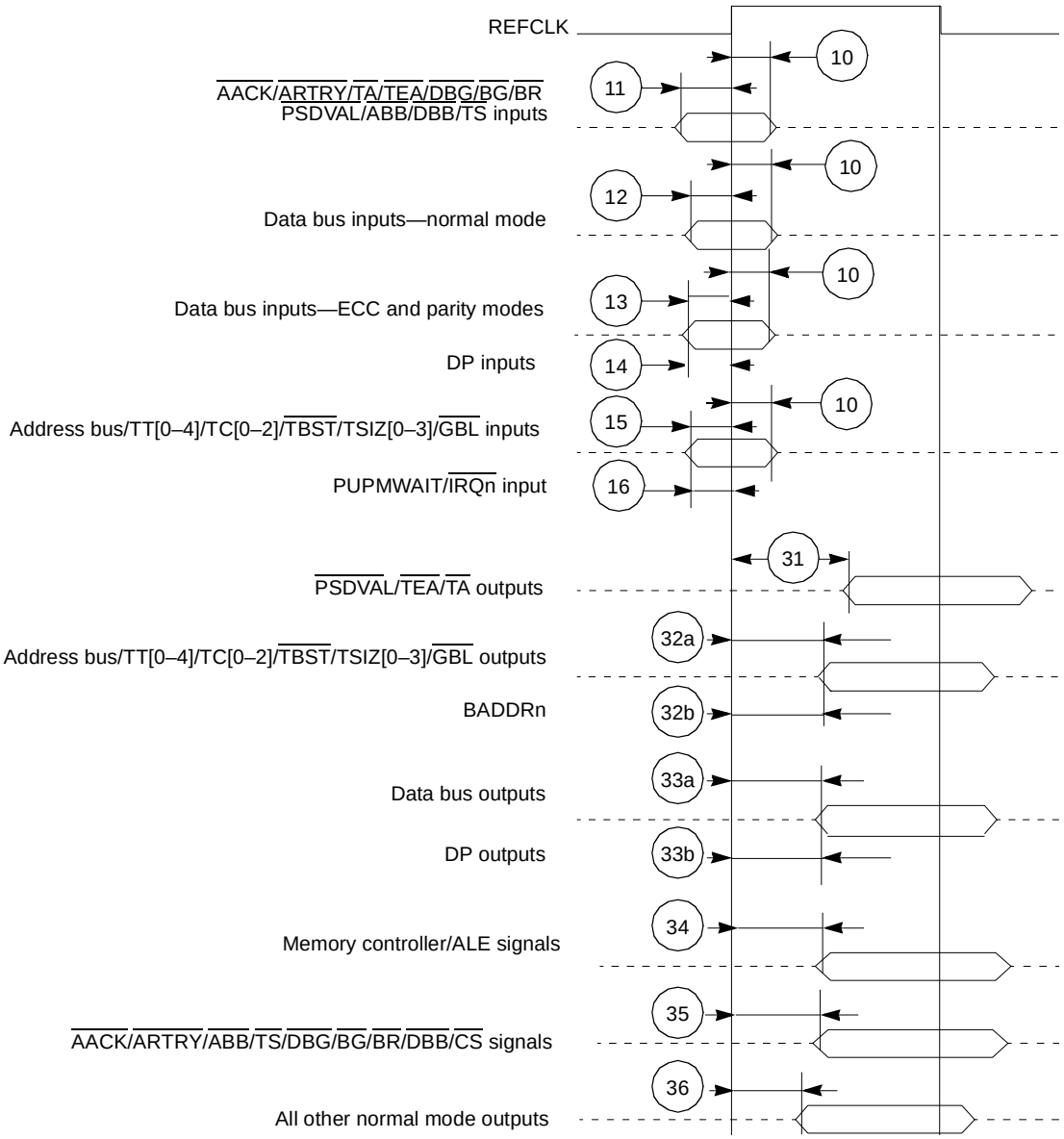


Figure 2B-6. Bus Signal Timing

2B.7.3.2 DMA Data Transfers

Table 2B-17 describes the DMA signal timing.

Table 2B-17. DMA Signals

Number	Characteristic	Minimum	Maximum	Units
72	DREQ setup time before REFCLK falling edge	6	—	ns
73	DREQ hold time after REFCLK falling edge	0.5	—	ns
74	$\overline{\text{DONE}}$ setup time before REFCLK rising edge	9	—	ns
75	$\overline{\text{DONE}}$ hold time after REFCLK rising edge	0.5	—	ns
76	$\overline{\text{DACK}}$/$\overline{\text{DRACK}}$/$\overline{\text{DONE}}$ delay after REFCLK rising edge	0.5	9	ns

The DREQ signal is synchronized with the falling edge of REFCLK. $\overline{\text{DONE}}$ timing is relative to the rising edge of REFCLK. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 2B-17**. **Figure 2B-7** shows synchronous peripheral interaction.

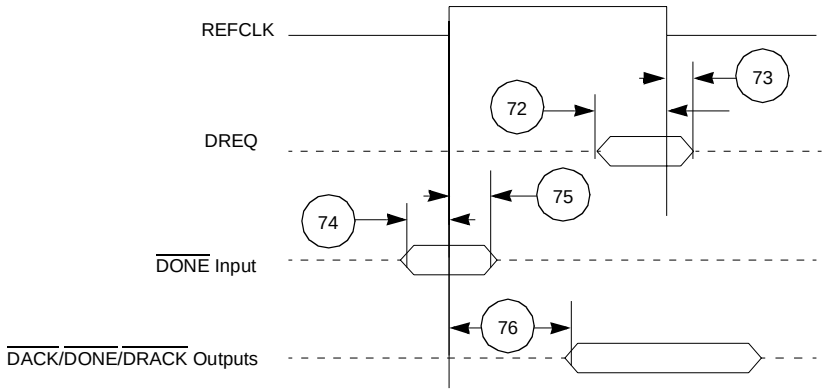


Figure 2B-7. DMA Signals

2B.7.4 HDI16 Signals

Table 2B-18. Host Interface (HDI16) Timing[1, 2]

Number	Characteristics[3]	Expression	Value	Unit
44a	Read data strobe minimum assertion width[4] HACK read minimum assertion width	$(1.5 \times T_C) + 5.0$	Note 11	ns
44b	Read data strobe minimum deassertion width[4] HACK read minimum deassertion width	$T_C + 5.0$	Note 11	ns
44c	Read data strobe minimum deassertion width[4] after "Last Data Register" reads[5,6], or between two consecutive CVR, ICR, or ISR reads[7] HACK minimum deassertion width after "Last Data Register" reads[5,6]	$(2.5 \times T_C) + 5.0$	Note 11	ns
45	Write data strobe minimum assertion width[8] HACK write minimum assertion width	$(1.5 \times T_C) + 5.0$	Note 11	ns
46	Write data strobe minimum deassertion width[8] HACK write minimum deassertion width after ICR, CVR and Data Register writes[5]	$(2.5 \times T_C) + 5.0$	Note 11	ns
47	Host data input minimum setup time before write data strobe deassertion[8] Host data input minimum setup time before HACK write deassertion	—	5.0	ns
48	Host data input minimum hold time after write data strobe deassertion[8] Host data input minimum hold time after HACK write deassertion	—	5.0	ns
49	Read data strobe minimum assertion to output data active from high impedance[4] HACK read minimum assertion to output data active from high impedance	—	5.0	ns
50	Read data strobe maximum assertion to output data valid[4] HACK read maximum assertion to output data valid	$(2.0 \times T_C) + 5.0$	Note 11	ns
51	Read data strobe maximum deassertion to output data high impedance[4] HACK read maximum deassertion to output data high impedance	—	5.0	ns
52	Output data minimum hold time after read data strobe deassertion[4] Output data minimum hold time after HACK read deassertion	—	5.0	ns
53	HCS[1–2] minimum assertion to read data strobe assertion[4]	—	5.0	ns
54	HCS[1–2] minimum assertion to write data strobe assertion[8]	—	5.0	ns
55	HCS[1–2] maximum assertion to output data valid	$T_C + 5.0$	Note 11	ns
56	HCS[1–2] minimum hold time after data strobe deassertion[9]	—	0.0	ns
57	HA[0–3], HRW minimum setup time before data strobe assertion[9] • Read • Write	—	 0 5.0	 ns ns
58	HA[0–3], HRW minimum hold time after data strobe deassertion[9]	—	5.0	ns
61	Maximum delay from read data strobe deassertion to host request deassertion for "Last Data Register" read[4, 5, 10]	$(3.5 \times T_C) + 5.0$	Note 11	ns
62	Maximum delay from write data strobe deassertion to host request deassertion for "Last Data Register" write[5,8,10]	$(2.5 \times T_C) + 5$	Note 11	ns
63	Minimum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) deassertion to HREQ assertion.	$(4.0 \times T_C) + 5.0$	Note 11	ns
64	Maximum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) assertion to HREQ deassertion	$(3.5 \times T_C) + 5.0$	Note 11	ns

Table 2B-18. Host Interface (HDI16) Timing[1, 2] (Continued)

Number	Characteristics[3]	Expression	Value	Unit

Notes:

1. T_C = 1/ DSPCLK. At 300 MHz, T_C = 3.3 ns
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF
4. The read data strobe is $\overline{\text{HRD}}$/HRD in the dual data strobe mode and $\overline{\text{HDS}}$/HDS in the single data strobe mode.
5. In 64-bit mode, The “last data register” is the register at address $7, which is the last location to be read or written in data transfers. This is RX0/TX0 in the little endian mode (HBE = 0), or RX3/TX3 in the big endian mode (HBE = 1).
6. This timing is applicable only if a read from the “last data register” is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the $\overline{\text{HREQ}}$/HREQ signal.
7. This timing is applicable only if two consecutive reads from one of these registers are executed.
8. The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.
9. The data strobe is host read ($\overline{\text{HRD}}$/HRD) or host write ($\overline{\text{HWR}}$/HWR) in the dual data strobe mode and host data strobe ($\overline{\text{HDS}}$/HDS) in the single data strobe mode.
10. The host request is $\overline{\text{HREQ}}$/HREQ in the single host request mode and $\overline{\text{HRRQ}}$/HRRQ and $\overline{\text{HTRQ}}$/HTRQ in the double host request mode. $\overline{\text{HRRQ}}$/HRRQ is deasserted only when HOTX fifo is empty, $\overline{\text{HTRQ}}$/HTRQ is deasserted only if HORX fifo is full (treat as level Host Request).
11. Compute the value using the expression.

Figure 2B-8 and **Figure 2B-9** show HDI16 read signal timing. **Figure 2B-10** and **Figure 2B-11** show HDI16 write signal timing.

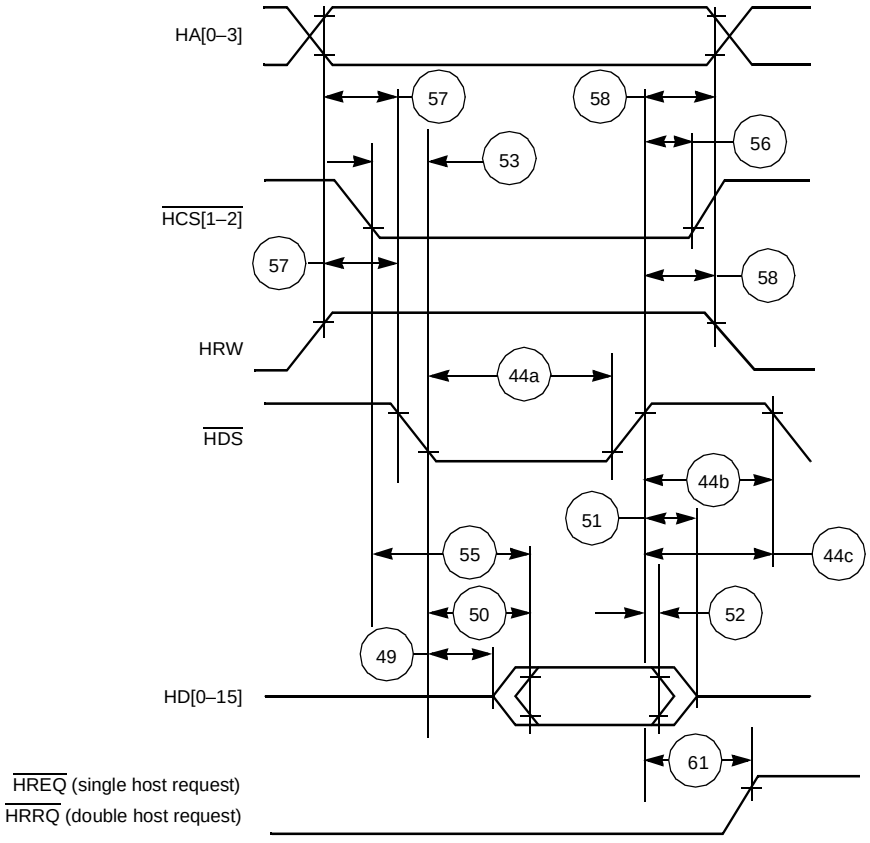


Figure 2B-8. Read Timing Diagram, Single Data Strobe

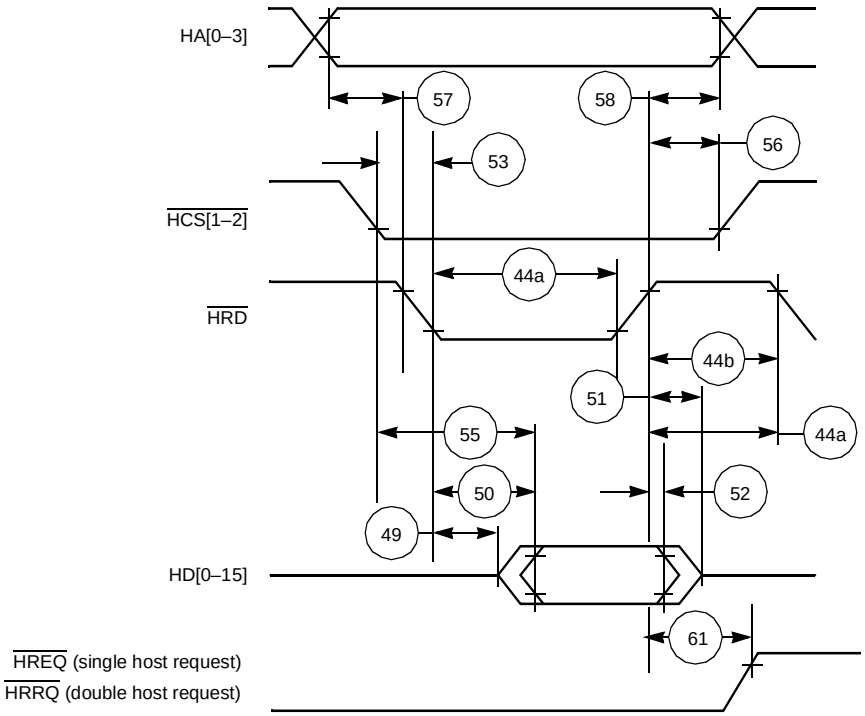


Figure 2B-9. Read Timing Diagram, Double Data Strobe

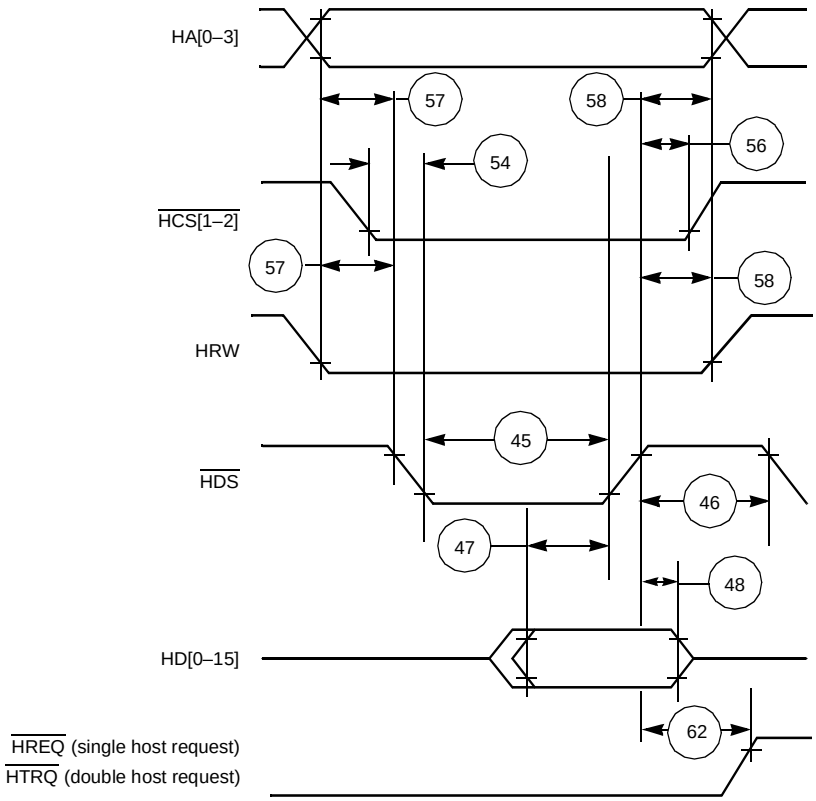


Figure 2B-10. Write Timing Diagram, Single Data Strobe

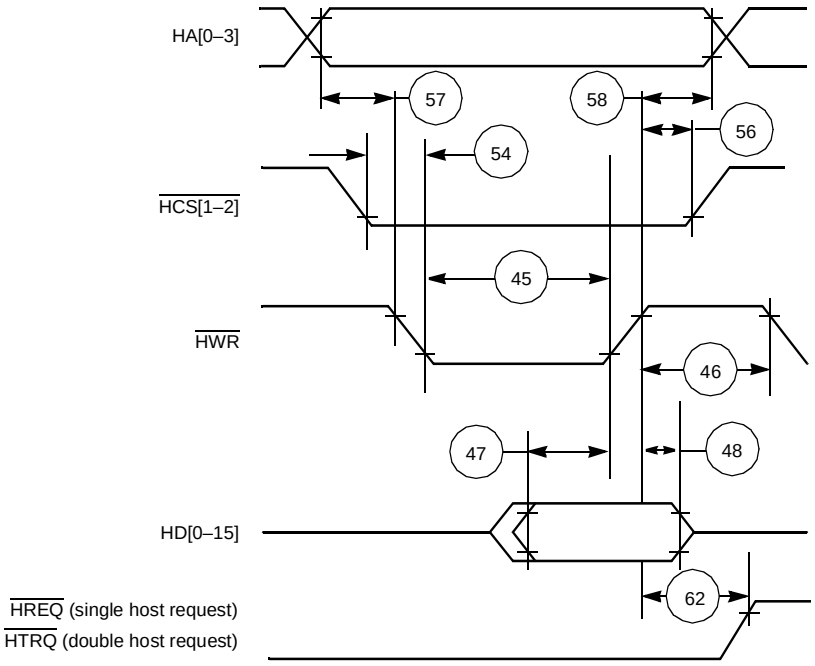


Figure 2B-11. Write Timing Diagram, Double Data Strobe

Figure 2B-12 shows Host DMA read timing.

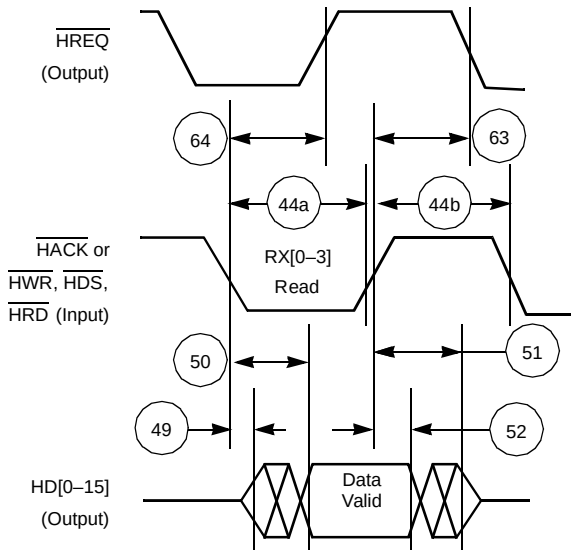


Figure 2B-12. Host DMA Read Timing Diagram

Figure 2B-13 shows Host DMA write timing.

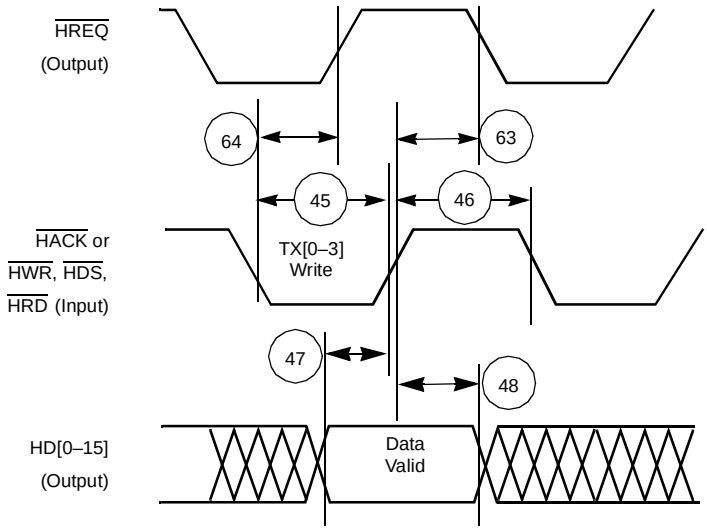


Figure 2B-13. Host DMA Write Timing Diagram

2B.7.5 CPM Timings

Table 2B-19. CPM Input Characteristics

No.	Characteristic	Typical	Unit
16	FCC input setup time before low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 10 5	 ns ns
17	FCC input hold time after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 0 3	 ns ns
18	SCC/SMC/SPI/I^2C input setup time before low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 20 5	 ns ns
19	SCC/SMC/SPI/I^2C input hold time after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 0 5	 ns ns
20	TDM input setup time before low-to-high serial clock transition	20	ns
21	TDM input hold time after low-to-high serial transition	20	ns
22	PIO/TIMER/DMA input setup time before low-to-high serial clock transition	10	ns
23	PIO/TIMER/DMA input hold time after low-to-high serial clock transition	3	ns
Note:	FCC, SCC, SMC, SPI, I^2C are Non-Multiplexed Serial Interface signals.		

Table 2B-20. CPM Output Characteristics

No.	Characteristic	Min	Max	Unit
36	FCC output delay after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial input clock)	 0 2	 6 18	 ns ns
38	SCC/SMC/SPI/I^2C output delay after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial input clock)	 0 0	 20 30	 ns ns
40	TDM output delay after low-to-high serial clock transition	5	35	ns
42	PIO/TIMER/DMA output delay after low-to-high serial clock transition	1	14	ns
Note:	FCC, SCC, SMC, SPI, I^2C are Non-Multiplexed Serial Interface signals.			

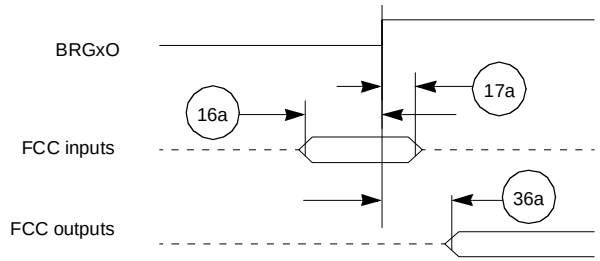


Figure 2B-14. FCC Internal Clock Diagram

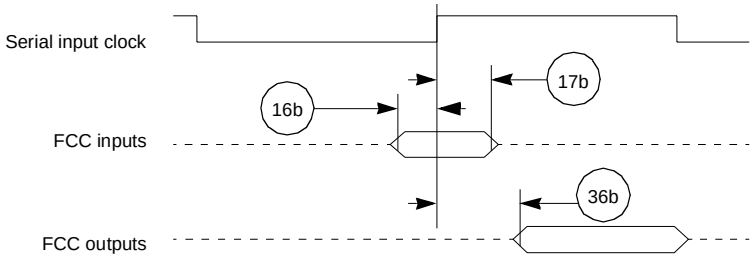


Figure 2B-15. FCC External Clock Diagram

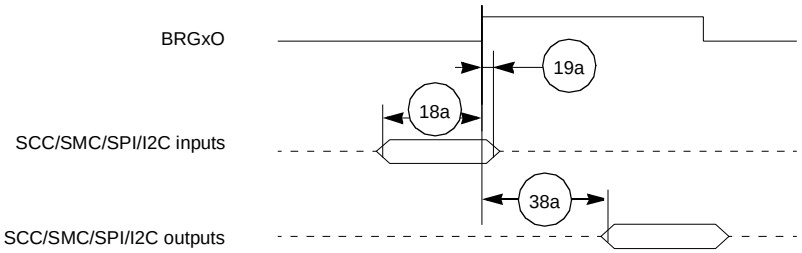


Figure 2B-16. SCC/SMC/SPI/I^2C Internal Clock Diagram

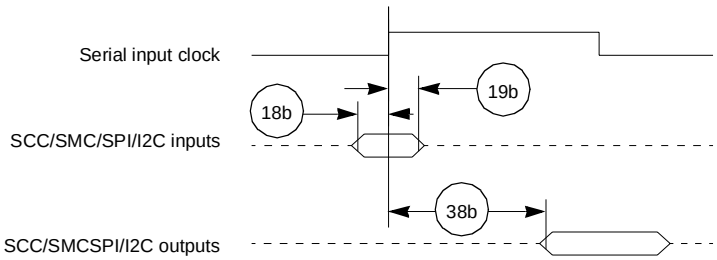


Figure 2B-17. SCC/SMC/SPI/I^{2}C External Clock Diagram

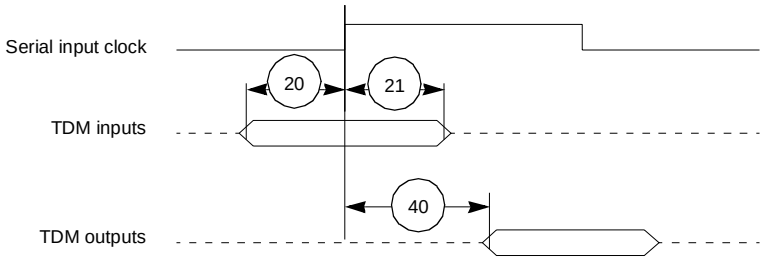


Figure 2B-18. TDM Signal Diagram

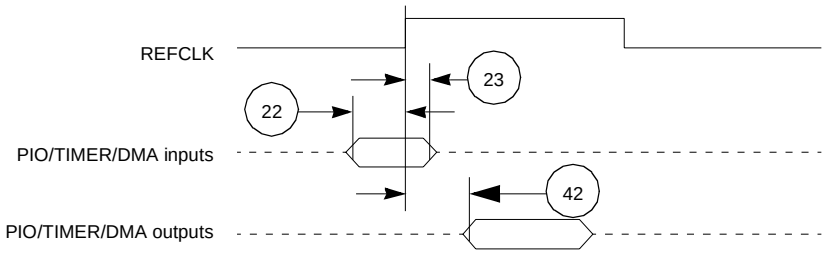


Figure 2B-19. PIO, Timer, and DMA Signal Diagram

Note: The timing values listed are preliminary and refer to minimum system timing requirements. Actual implementation requires conformance to the specific protocol requirements. Refer to **Chapter 1** to identify the specific input and output signals associated with the referenced internal controllers and supported communication protocols. For example, FCC1 supports ATM/Utopia operation in slave mode, multi-PHY master direct polling mode, and multi-PHY master multiplexed polling mode and each of these modes supports its own set of signals; the direction (input or output) of some of the shared signal names depends on the selected mode.

2B.7.6 JTAG Signals

Table 2B-21. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
500	TCK frequency of operation	0.0	40.0	MHz
501	TCK cycle time	25.0	—	ns
502	TCK clock pulse width measured at 1.6 V	12.5	—	ns
503	TCK rise and fall times	0.0	3.0	ns
508	TMS, TDI data set-up time	6.0	—	ns
509	TMS, TDI data hold time	3.0	—	ns
510	TCK low to TDO data valid	0.0	15.0	ns
511	TCK low to TDO high impedance	0.0	5.0	ns
512	$\overline{\text{TRST}}$ assert time	100.0	—	ns
513	$\overline{\text{TRST}}$ set-up time to TCK low	40.0	—	ns

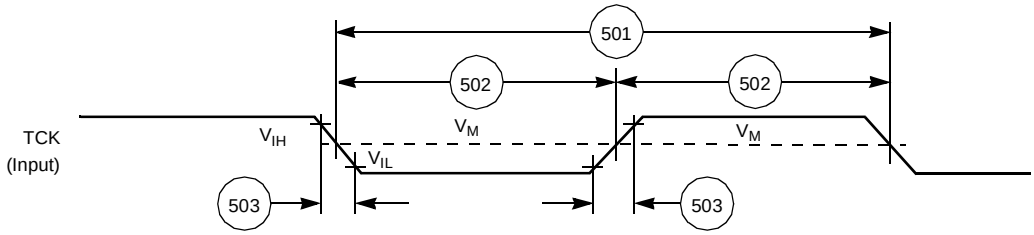


Figure 2B-20. Test Clock Input Timing Diagram

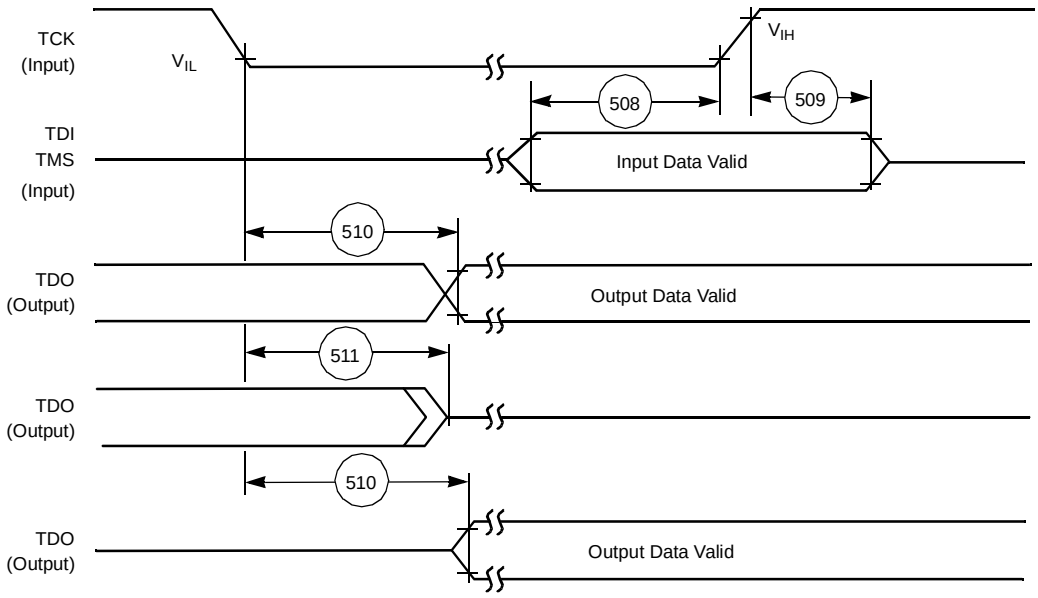


Figure 2B-21. Test Access Port Timing Diagram

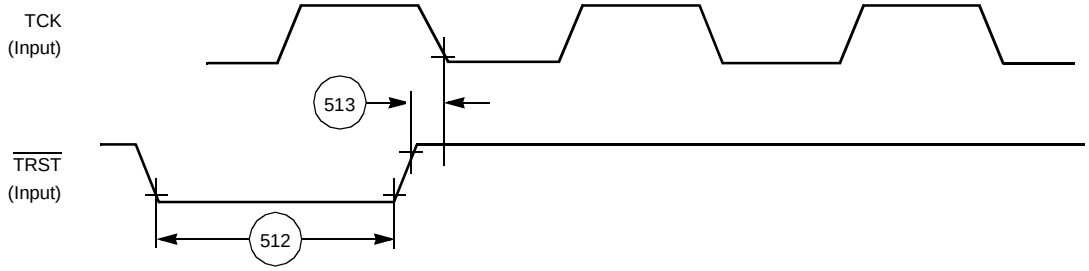


Figure 2B-22. $\overline{\text{TRST}}$ Timing Diagram

Chapter 3

Packaging

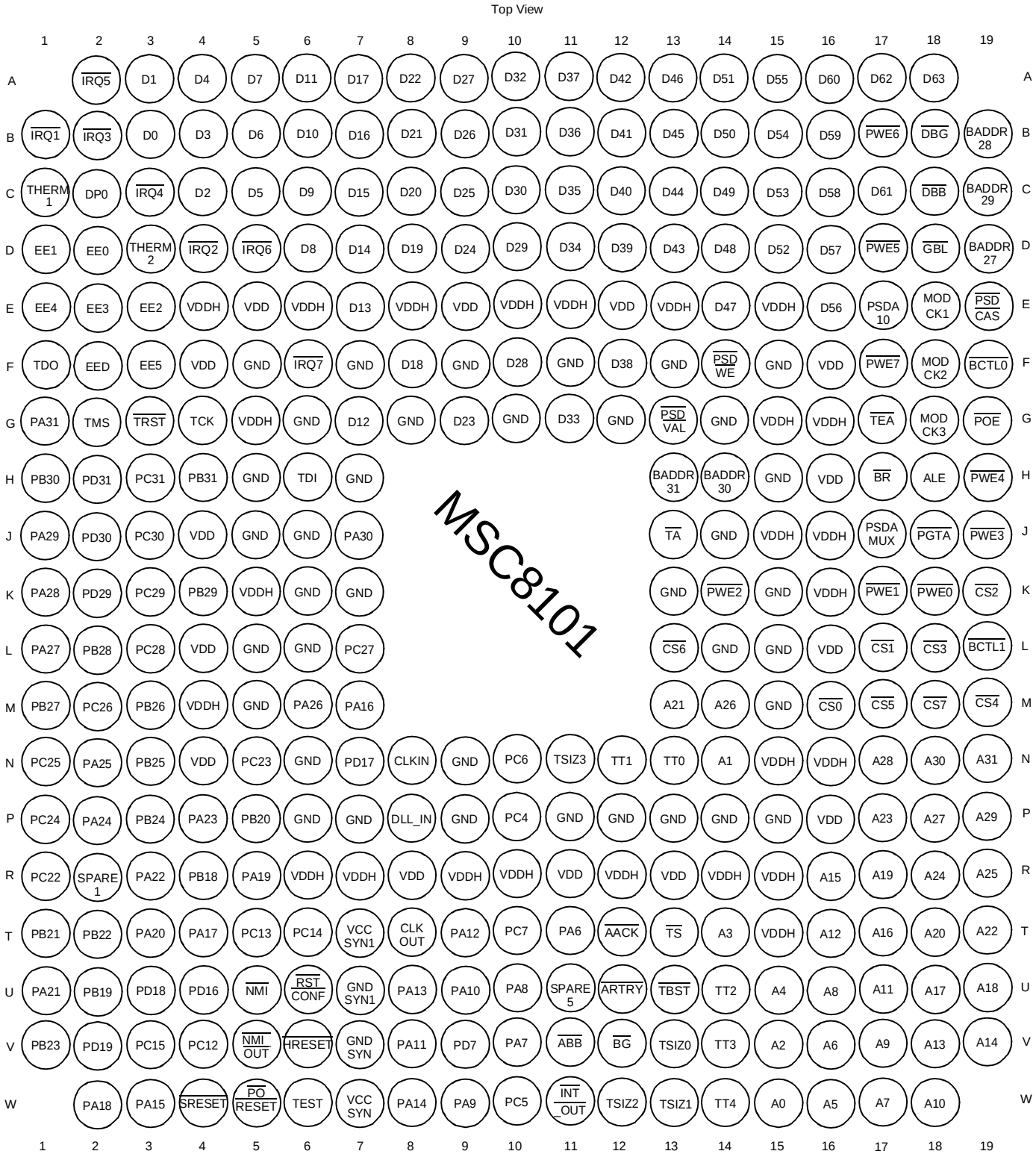
3.1 Pin-Out and Package Information

This sections provides information about the MSC8101 package, including diagrams of the package pinouts and tables showing how the signals discussed in **Chapter 1** are allocated. The MSC8101 is available in a 332-pin lidded Flip Chip-Plastic Ball Grid Array (FC-PBGA).

3.2 FC-PBGA Package Description

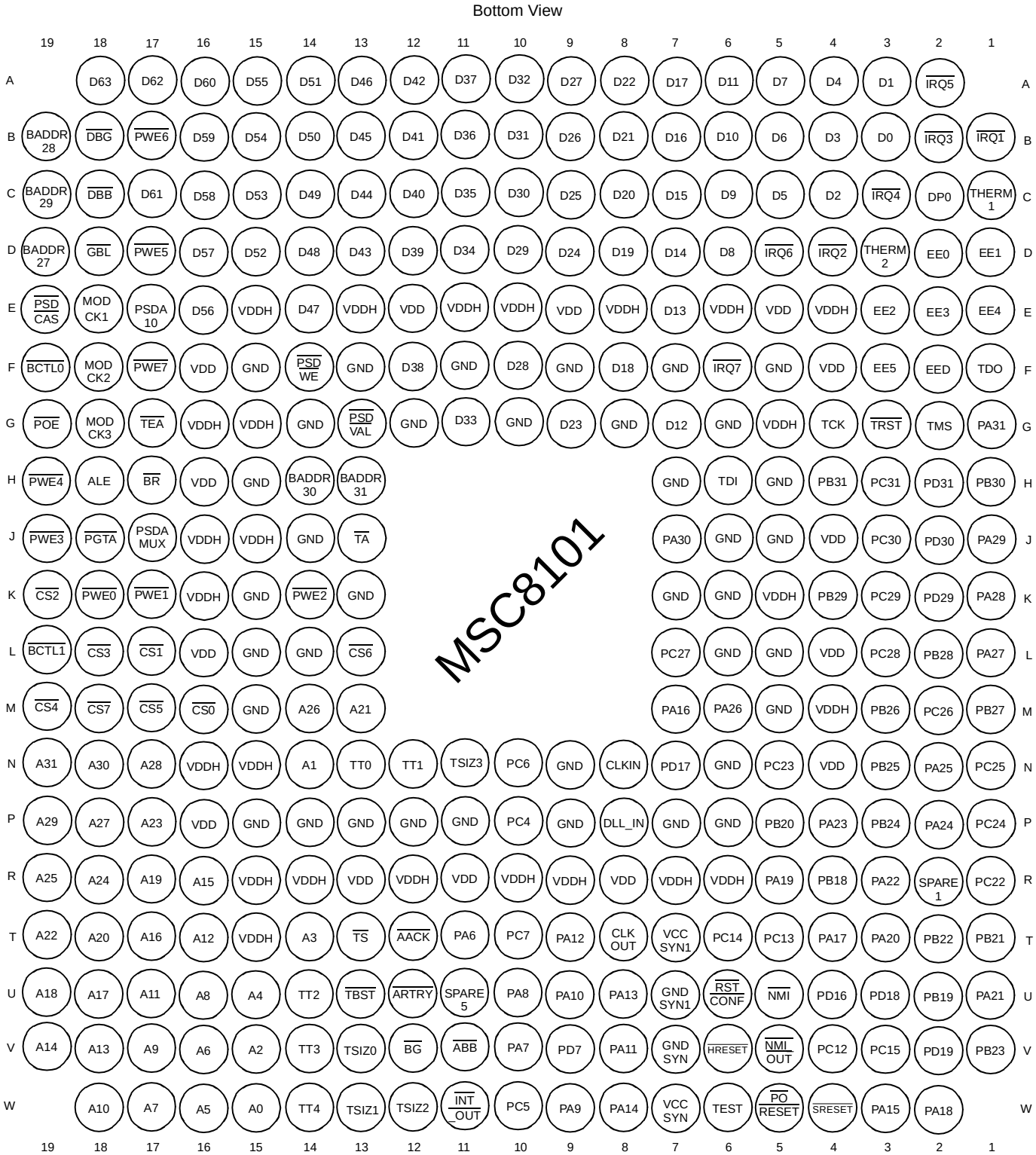
Figure 3-1 and **Figure 3-2** show top and bottom views of the FC-PBGA package, including pinouts. **Table 3-1** lists the MSC8101 signals alphabetically by signal name. Connections with multiple names are listed individually by each name. Signals with programmable polarity are shown both as signals which are asserted low (default) and high (i.e., NAME/NAME). **Table 3-2** lists the signals numerically by pin number. Each pin number is listed once with the various signals that are multiplexed to it. For simplicity, signals with programmable polarity are shown in this table only with their default name (asserted low).

Note: There are two types of lidded FC-PBGA packages used with the MSC8101 with slightly different height dimensions. See **Section 3.3** for details.



Note: Signal names in this figure are the default signals after reset, except for signals C2, C19, D1, D2, D18, E1, F3, H13, H14, and W11 which show the second configuration signal name.

Figure 3-1. MSC8101 Flip Chip Plastic Ball Grid Array (FC-PBGA), Top View



Note: Signal names in this figure are the default signals after reset, except for signals C2, C19, D1, D2, D18, E1, F3, H13, H14, and W11 which show the second configuration signal name.

Figure 3-2. MSC8101 Flip Chip Plastic Ball Grid Array (FC-PBGA), Bottom Vie

Table 3-1. MSC8101 Signal Listing By Name

Signal Name	Number
A0	W15
A1	N14
A2	V15
A3	T14
A4	U15
A5	W16
A6	V16
A7	W17
A8	U16
A9	V17
A10	W18
A11	U17
A12	T16
A13	V18
A14	V19
A15	R16
A16	T17
A17	U18
A18	U19
A19	R17
A20	T18
A21	M13
A22	T19
A23	P17
A24	R18
A25	R19
A26	M14
A27	P18
A28	N17
A29	P19
A30	N18
A31	N19
$\overline{\text{AACK}}$	T12

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
$\overline{\text{ABB}}$	V11
ALE	H18
$\overline{\text{ARTRY}}$	U12
BADDR27	D19
BADDR28	B19
BADDR29	C19
BADDR30	H14
BADDR31	H13
$\overline{\text{BCTL0}}$	F19
$\overline{\text{BCTL1}}$	L19
BG	V12
BNKSEL0	E18
BNKSEL1	F18
BNKSEL2	G18
$\overline{\text{BR}}$	H17
BRG1O	H3
BRG1O	V2
BRG2O	J3
BRG2O	N7
BRG3O	K3
BRG4O	L3
BRG5O	L7
BRG6O	M2
BRG7O	N1
BRG8O	P1
BTM0	E1
BTM1	F3
$\overline{\text{CD}}$ for FCC1	N10
$\overline{\text{CD}}$ for FCC2	P10
$\overline{\text{CD}}$/RENA for SCC1	T6
$\overline{\text{CD}}$/RENA for SCC2	V4
CLK1	H3
CLK2	J3

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
CLK3	K3
CLK4	L3
CLK5	L7
CLK6	M2
CLK7	N1
CLK8	P1
CLK9	N5
CLK10	R1
CLKIN	N8
CLKOUT	T8
COL for FCC1	G1
COL for FCC2	M1
CRS for FCC1	J7
CRS for FCC2	M3
$\overline{\text{CS0}}$	M16
$\overline{\text{CS1}}$	L17
$\overline{\text{CS2}}$	K19
$\overline{\text{CS3}}$	L18
$\overline{\text{CS4}}$	M19
$\overline{\text{CS5}}$	M17
$\overline{\text{CS6}}$	L13
$\overline{\text{CS7}}$	M18
$\overline{\text{CTS}}$ for FCC1	T10
$\overline{\text{CTS}}$ for FCC2	W10
$\overline{\text{CTS}}$/CLSN for SCC1	K3
$\overline{\text{CTS}}$/CLSN for SCC1	V3
$\overline{\text{CTS}}$/CLSN for SCC2	L3
$\overline{\text{CTS}}$/CLSN for SCC2	T5
D0	B3
D1	A3
D2	C4
D3	B4
D4	A4

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
D5	C5
D6	B5
D7	A5
D8	D6
D9	C6
D10	B6
D11	A6
D12	G7
D13	E7
D14	D7
D15	C7
D16	B7
D17	A7
D18	F8
D19	D8
D20	C8
D21	B8
D22	A8
D23	G9
D24	D9
D25	C9
D26	B9
D27	A9
D28	F10
D29	D10
D30	C10
D31	B10
D32	A10
D33	G11
D34	D11
D35	C11
D36	B11
D37	A11

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
D38	F12
D39	D12
D40	C12
D41	B12
D42	A12
D43	D13
D44	C13
D45	B13
D46	A13
D47	E14
D48	D14
D49	C14
D50	B14
D51	A14
D52	D15
D53	C15
D54	B15
D55	A15
D56	E16
D57	D16
D58	C16
D59	B16
D60	A16
D61	C17
D62	A17
D63	A18
$\overline{\text{DACK1}}$	N5
$\overline{\text{DACK2}}$	N1
$\overline{\text{DACK3}}$	D5
$\overline{\text{DACK4}}$	F6
$\overline{\text{DBB}}$	C18
$\overline{\text{DBG}}$	B18
DBREQ	D2

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
DLLIN	P8
DP0	C2
DP1	B1
DP2	D4
DP3	B2
DP4	C3
DP5	A2
DP6	D5
DP7	F6
$\overline{\text{DRACK1}}/\overline{\text{DONE1}}$	H2
$\overline{\text{DRACK2}}/\overline{\text{DONE2}}$	J2
DREQ1	R1
DREQ2	P1
DREQ3	C3
DREQ4	A2
EE0	D2
EE1	D1
EE2	E3
EE3	E2
EE4	E1
EE5	F3
EED	F2
$\overline{\text{EXT\_BG2}}$	B1
$\overline{\text{EXT\_BG3}}$	C3
$\overline{\text{EXT\_BR2}}$	C2
$\overline{\text{EXT\_BR3}}$	B2
$\overline{\text{EXT\_DBG2}}$	D4
$\overline{\text{EXT\_DBG3}}$	A2
EXT1	H3
EXT2	N5
$\overline{\text{GBL}}$	D18
GND	F11
GND	F13

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
GND	F15
GND	F5
GND	F7
GND	F9
GND	G10
GND	G12
GND	G14
GND	G6
GND	G8
GND	H15
GND	H5
GND	H7
GND	J14
GND	J5
GND	J6
GND	K13
GND	K15
GND	K6
GND	K7
GND	L14
GND	L15
GND	L5
GND	L6
GND	M15
GND	M5
GND	N6
GND	N9
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P6

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
GND	P7
GND	P9
GND_{SYN}	V7
GND_{SYN1}	U7
H8BIT	B16
HA0	D14
HA1	C14
HA2	B14
HA3	A14
$\overline{HACK}$/HACK	E16
$\overline{HCS1}$/HCS1	D15
$\overline{HCS2}$/HCS2	A16
HD0	A10
HD1	G11
HD2	D11
HD3	C11
HD4	B11
HD5	A11
HD6	F12
HD7	D12
HD8	C12
HD9	B12
HD10	A12
HD11	D13
HD12	C13
HD13	B13
HD14	A13
HD15	E14
HDDS	C16
$\overline{HDS}$/HDS	B15
HDSP	D16
HPE	D1
$\overline{HRD}$/HRD	C15

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
$\overline{\text{HREQ}}$/HREQ	A15
HRESET	V6
$\overline{\text{HRRQ}}$/HRRQ	E16
HRW	C15
$\overline{\text{HTRQ}}$/HTRQ	A15
$\overline{\text{HWR}}$/HWR	B15
$\overline{\text{INT\_OUT}}$	W11
$\overline{\text{IRQ1}}$	B1
$\overline{\text{IRQ1}}$	D18
$\overline{\text{IRQ2}}$	C19
$\overline{\text{IRQ2}}$	D4
$\overline{\text{IRQ2}}$	V11
$\overline{\text{IRQ3}}$	B2
$\overline{\text{IRQ3}}$	C18
$\overline{\text{IRQ3}}$	H14
$\overline{\text{IRQ4}}$	C3
$\overline{\text{IRQ5}}$	A2
$\overline{\text{IRQ5}}$	H13
$\overline{\text{IRQ6}}$	D5
$\overline{\text{IRQ7}}$	F6
$\overline{\text{IRQ7}}$	W11
L1RSYNC for SI1 TDMA1	T11
L1RSYNC for SI2 TDMB2	K4
L1RSYNC for SI2 TDMC2	P3
L1RSYNC for SI2 TDMD2	P5
L1RXD for SI1 TDMA1 Serial	U10
L1RXD for SI2 TDMB2	H1
L1RXD for SI2 TDMC2	M3
L1RXD for SI2 TDMD2	T2
L1RXD0 for SI1 TDMA1 Nibble	U10
L1RXD1 for SI1 TDMA1 Nibble	T2
L1RXD2 for SI1 TDMA1 Nibble	V1
L1RXD3 for SI1 TDMA1 Nibble	P3

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
L1TSYNC for SI1 TDMA1	V10
L1TSYNC for SI2 TDMB2	L2
L1TSYNC for SI2 TDMC2	N3
L1TSYNC for SI2 TDMD2	T1
L1TXD for SI1 TDMA1 Serial	W9
L1TXD for SI2 TDMB2	H4
L1TXD for SI2 TDMC2	M1
L1TXD for SI2 TDMD2	V1
L1TXD0 for SI1 TDMA1 Nibble	W9
L1TXD1 for SI1 TDMA1 Nibble	P5
L1TXD2 for SI1 TDMA1 Nibble	T1
L1TXD3 for SI1 TDMA1 Nibble	N3
LIST1 for SI1	R1
LIST1 for SI2	T10
LIST2 for SI1	T6
LIST2 for SI2	N10
LIST3 for SI1	V4
LIST3 for SI2	W10
LIST4 for SI1	T5
LIST4 for SI2	P10
MODCK1	E18
MODCK2	F18
MODCK3	G18
MSNUM0	N2
MSNUM1	P2
MSNUM2	U8
MSNUM3	T9
MSNUM4	V8
MSNUM5	U9
$\overline{\text{NMI}}$	U5
$\overline{\text{NMI\_OUT}}$	V5
PA6	T11
PA7	V10

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
PA8	U10
PA9	W9
PA10	U9
PA11	V8
PA12	T9
PA13	U8
PA14	W8
PA15	W3
PA16	M7
PA17	T4
PA18	W2
PA19	R5
PA20	T3
PA21	U1
PA22	R3
PA23	P4
PA24	P2
PA25	N2
PA26	M6
PA27	L1
PA28	K1
PA29	J1
PA30	J7
PA31	G1
PB18	R4
PB19	U2
PB20	P5
PB21	T1
PB22	T2
PB23	V1
PB24	P3
PB25	N3
PB26	M3

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
PB27	M1
PB28	L2
PB29	K4
PB30	H1
PB31	H4
$\overline{\text{PBS0}}$	K18
$\overline{\text{PBS1}}$	K17
$\overline{\text{PBS2}}$	K14
$\overline{\text{PBS3}}$	J19
$\overline{\text{PBS4}}$	H19
$\overline{\text{PBS5}}$	D17
$\overline{\text{PBS6}}$	B17
$\overline{\text{PBS7}}$	F17
PC4	P10
PC5	W10
PC6	N10
PC7	T10
PC12	V4
PC13	T5
PC14	T6
PC15	V3
PC22	R1
PC23	N5
PC24	P1
PC25	N1
PC26	M2
PC27	L7
PC28	L3
PC29	K3
PC30	J3
PC31	H3
PD7	V9
PD16	U4

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
PD17	N7
PD18	U3
PD19	V2
PD29	K2
PD30	J2
PD31	H2
PGPL0	E17
PGPL1	F14
PGPL2	G19
PGPL3	E19
PGPL4	J18
PGPL5	J17
$\overline{\text{PGTA}}$	J18
$\overline{\text{POE}}$	G19
$\overline{\text{PORESET}}$	W5
$\overline{\text{PPBS}}$	J18
PSDA10	E17
PSDAMUX	J17
$\overline{\text{PSDCAS}}$	E19
$\overline{\text{PSDDQM0}}$	K18
$\overline{\text{PSDDQM1}}$	K17
$\overline{\text{PSDDQM2}}$	K14
$\overline{\text{PSDDQM3}}$	J19
$\overline{\text{PSDDQM4}}$	H19
$\overline{\text{PSDDQM5}}$	D17
$\overline{\text{PSDDQM6}}$	B17
$\overline{\text{PSDDQM7}}$	F17
$\overline{\text{PSDRAS}}$	G19
$\overline{\text{PSDVAL}}$	G13
$\overline{\text{PSDWE}}$	F14
PUPMWAIT	J18
$\overline{\text{PWE0}}$	K18
$\overline{\text{PWE1}}$	K17

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
$\overline{\text{PWE2}}$	K14
$\overline{\text{PWE3}}$	J19
$\overline{\text{PWE4}}$	H19
$\overline{\text{PWE5}}$	D17
$\overline{\text{PWE6}}$	B17
$\overline{\text{PWE7}}$	F17
Reserved	A17
Reserved	A18
Reserved	C2
Reserved	C17
Reserved	C19
Reserved	H14
Reserved	H13
$\overline{\text{RSTCONF}}$	U6
$\overline{\text{RTS}}$ for FCC1	J7
$\overline{\text{RTS}}$ for FCC2	L2
$\overline{\text{RTS}}$/TENA for SCC1	K2
$\overline{\text{RTS}}$/TENA for SCC2	L2
RX_DV for FCC1	L1
RX_DV for FCC2	H1
RX_ER for FCC1	M6
RX_ER for FCC2	L2
RXADDR0 for FCC1 UTOPIA 8	T6
RXADDR1 for FCC1 UTOPIA 8	V4
RXADDR2 for FCC1 UTOPIA 8	N10
RXADDR2/RXCLAV1 for FCC1 UTOPIA 8	N10
RXADDR3 for FCC1 UTOPIA 8	K2
RXADDR4 for FCC1 UTOPIA 8	U3
RXCLAV for FCC1 UTOPIA 8	M6
RXCLAV0 for FCC1 UTOPIA 8	M6
RXCLAV2 for FCC1 UTOPIA 8	K2
RXCLAV3 for FCC1 UTOPIA 8	V4
RXD for FCC1 transparent/HDLC serial	T4

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
RXD for FCC2 transparent/HDLC serial	T1
RXD for SCC1	H2
RXD for SCC2	H4
RXD0 for FCC1 MII/HDLC nibble	T4
RXD0 for FCC1 UTOPIA 8	U9
RXD0 for FCC2 MII/HDLC nibble	T1
RXD1 for FCC1 MII/HDLC nibble	M7
RXD1 for FCC1 UTOPIA 8	V8
RXD1 for FCC2 MII/HDLC nibble	P5
RXD2 for FCC1 MII/HDLC nibble	W3
RXD2 for FCC1 UTOPIA 8	T9
RXD2 for FCC2 MII/HDLC nibble	U2
RXD3 for FCC1 MII/HDLC nibble	W8
RXD3 for FCC1 UTOPIA 8	U8
RXD3 for FCC2 MII/HDLC nibble	R4
RXD4 for FCC1 UTOPIA 8	W8
RXD5 for FCC1 UTOPIA 8	W3
RXD6 for FCC1 UTOPIA 8	M7
RXD7 for FCC1 UTOPIA 8	T4
$\overline{\text{RXENB}}$ for FCC1	K1
RXPRTY for FCC1 UTOPIA 8	N7
RXSOC for FCC1	L1
SCL	R4
SDA	U2
SMRXD for SMC1	P10
SMRXD for SMC2	U10
$\overline{\text{SMSYN}}$ for SMC1	V9
$\overline{\text{SMSYN}}$ for SMC2	V10
SMTXD for SMC1	W10
SMTXD for SMC2	W9
SMTXD for SMC2	V3
SPARE1	R2
SPARE5	U11

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
SPICLK	U3
SPIMISO	U4
SPIMOSI	N7
$\overline{\text{SPISEL}}$	V2
$\overline{\text{SRESET}}$	W4
$\overline{\text{TA}}$	J13
$\overline{\text{TBST}}$	U13
TC0	E18
TC1	F18
TC2	G18
TCK	G4
TDI	H6
TDO	F1
$\overline{\text{TEA}}$	G17
TEST	W6
$\overline{\text{TGATE1}}$	H3
$\overline{\text{TGATE2}}$	L7
THERM1	C1
THERM2	D3
TIN1/$\overline{\text{TOUT2}}$	L3
TIN2	K3
TIN3/$\overline{\text{TOUT4}}$	P1
TIN4	N1
TMCLK	M2
TMS	G2
$\overline{\text{TOUT1}}$	J3
$\overline{\text{TOUT3}}$	M2
$\overline{\text{TRST}}$	G3
$\overline{\text{TS}}$	T13
TSIZ0	V13
TSIZ1	W13
TSIZ2	W12
TSIZ3	N11

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
TT0	N13
TT1	N12
TT2	U14
TT3	V14
TT4	W14
TX_EN for FCC1 MII	K1
TX_EN for FCC2 MII	K4
TX_ER for FCC1 MII	J1
TX_ER for FCC2 MII	H4
TXADDR0 for FCC1 UTOPIA 8	V3
TXADDR1 for FCC1 UTOPIA 8	T5
TXADDR2 for FCC1 UTOPIA 8	T10
TXADDR2 for FCC1 UTOPIA 8	T10
TXADDR3 for FCC1 UTOPIA 8	V9
TXADDR4 for FCC1 UTOPIA 8	V2
TXCLAV for FCC1 UTOPIA 8	J7
TXCLAV0 for FCC1 UTOPIA 8	J7
TXCLAV1 for FCC1 UTOPIA 8	T10
TXCLAV2 for FCC1 UTOPIA 8	V9
TXCLAV3 for FCC1 UTOPIA 8	V2
TXD for FCC1 transparent/HDLC serial	W2
TXD for FCC2 transparent/HDLC serial	T2
TXD for SCC1	J2
TXD for SCC2	H1
TXD0 for FCC1 MII/HDLC nibble	W2
TXD0 for FCC1 UTOPIA 8	N2
TXD0 for FCC2 MII/HDLC nibble	T2
TXD1 for FCC1 MII/HDLC nibble	R5
TXD1 for FCC1 UTOPIA 8	P2
TXD1 for FCC2 MII/HDLC nibble	V1
TXD2 for FCC1 MII/HDLC nibble	T3
TXD2 for FCC1 UTOPIA 8	P4
TXD2 for FCC2 MII/HDLC nibble	P3

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
TXD3 for FCC1 MII/HDLC nibble	U1
TXD3 for FCC1 UTOPIA 8	R3
TXD3 for FCC2 MII/HDLC nibble	N3
TXD4 for FCC1 UTOPIA 8	U1
TXD5 for FCC1 UTOPIA 8	T3
TXD6 for FCC1 UTOPIA 8	R5
TXD7 for FCC1 UTOPIA 8	W2
$\overline{\text{TXENB}}$ for FCC1	G1
TXPRTY for FCC1 UTOPIA 8	U4
TXSOC for FCC1	J1
V_{CCSYN}	W7
V_{CCSYN1}	T7
V_{DD}	E12
V_{DD}	E5
V_{DD}	E9
V_{DD}	F16
V_{DD}	F4
V_{DD}	H16
V_{DD}	J4
V_{DD}	L16
V_{DD}	L4
V_{DD}	N4
V_{DD}	P16
V_{DD}	R11
V_{DD}	R13
V_{DD}	R8
V_{DDH}	E10
V_{DDH}	E11
V_{DDH}	E13
V_{DDH}	E15
V_{DDH}	E4
V_{DDH}	E6
V_{DDH}	E8

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
V_{DDH}	G15
V_{DDH}	G16
V_{DDH}	G5
V_{DDH}	J15
V_{DDH}	J16
V_{DDH}	K16
V_{DDH}	K5
V_{DDH}	M4
V_{DDH}	N15
V_{DDH}	N16
V_{DDH}	R10
V_{DDH}	R12
V_{DDH}	R14
V_{DDH}	R15
V_{DDH}	R6
V_{DDH}	R7
V_{DDH}	R9
V_{DDH}	T15

Table 3-2. MSC8101 Signal Listing by Pin Designator

Number	Signal Name
A2	$\overline{\text{IRQ5}}$ / DP5 / DREQ4 / $\overline{\text{EXT\_DBG3}}$
A3	D1
A4	D4
A5	D7
A6	D11
A7	D17
A8	D22
A9	D27
A10	D32 / HD0
A11	D37 / HD5
A12	D42 / HD10
A13	D46 / HD14
A14	D51 / HA3

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
A15	D55 / $\overline{\text{HREQ}}$ / $\overline{\text{HTRQ}}$
A16	D60 / $\overline{\text{HCS2}}$
A17	D62 / Reserved
A18	D63 / Reserved
B1	$\overline{\text{IRQ1}}$ / DP1 / $\overline{\text{EXT\_BG2}}$
B2	$\overline{\text{IRQ3}}$ / DP3 / $\overline{\text{EXT\_BR3}}$
B3	D0
B4	D3
B5	D6
B6	D10
B7	D16
B8	D21
B9	D26
B10	D31
B11	D36 / HD4
B12	D41 / HD9
B13	D45 / HD13
B14	D50 / HA2
B15	D54 / $\overline{\text{HDS}}$ / $\overline{\text{HWR}}$
B16	D59 / H8BIT
B17	$\overline{\text{PWE6}}$ / $\overline{\text{PSDDQM6}}$ / $\overline{\text{PBS6}}$
B18	$\overline{\text{DBG}}$
B19	BADDR28
C1	THERM1
C2	Reserved / DP0 / $\overline{\text{EXT\_BR2}}$
C3	$\overline{\text{IRQ4}}$ / DP4 / DREQ3 / $\overline{\text{EXT\_BG3}}$
C4	D2
C5	D5
C6	D9
C7	D15
C8	D20
C9	D25
C10	D30
C11	D35 / HD3
C12	D40 / HD8
C13	D44 / HD12
C14	D49 / HA1
C15	D53 / HRW / $\overline{\text{HRD}}$

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
C16	D58 / HDDS
C17	D61
C18	$\overline{\text{DBB}}$ / $\overline{\text{IRQ3}}$
C19	BADDR29 / $\overline{\text{IRQ2}}$
D1	HPE / EE1
D2	DBREQ / EE0
D3	THERM2
D4	$\overline{\text{IRQ2}}$ / DP2 / $\overline{\text{EXT\_DBG2}}$
D5	$\overline{\text{IRQ6}}$ / DP6 / $\overline{\text{DACK3}}$
D6	D8
D7	D14
D8	D19
D9	D24
D10	D29
D11	D34 / HD2
D12	D39 / HD7
D13	D43 / HD11
D14	D48 / HA0
D15	D52 / $\overline{\text{HCS1}}$
D16	D57 / HDSP
D17	$\overline{\text{PWE5}}$ / $\overline{\text{PSDDQM5}}$ / $\overline{\text{PBS5}}$
D18	$\overline{\text{IRQ1}}$ / $\overline{\text{GBL}}$
D19	BADDR27
E1	BTM0 / EE4
E2	EE3
E3	EE2
E4	V_{DDH}
E5	V_{DD}
E6	V_{DDH}
E7	D13
E8	V_{DDH}
E9	V_{DD}
E10	V_{DDH}
E11	V_{DDH}
E12	V_{DD}
E13	V_{DDH}
E14	D47 / HD15
E15	V_{DDH}

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
E16	D56 / $\overline{\text{HACK}}$ / $\overline{\text{HRRQ}}$
E17	PSDA10 / PGPL0
E18	MODCK1 / TC0 / BNKSEL0
E19	$\overline{\text{PSDCAS}}$ / PGPL3
F1	TDO
F2	EED
F3	BTM1 / EE5
F4	V_{DD}
F5	GND
F6	$\overline{\text{IRQ7}}$ / DP7 / $\overline{\text{DACK4}}$
F7	GND
F8	D18
F9	GND
F10	D28
F11	GND
F12	D38 / HD6
F13	GND
F14	$\overline{\text{PSDWE}}$ / PGPL1
F15	GND
F16	V_{DD}
F17	$\overline{\text{PWE7}}$ / $\overline{\text{PSDDQM7}}$ / $\overline{\text{PBS7}}$
F18	MODCK2 / TC1 / BNKSEL1
F19	$\overline{\text{BCTL0}}$
G1	PA31 / FCC1:UTOPIA8:$\overline{\text{TXENB}}$ / FCC1:MII:COL
G2	TMS
G3	$\overline{\text{TRST}}$
G4	TCK
G5	V_{DDH}
G6	GND
G7	D12
G8	GND
G9	D23
G10	GND
G11	D33 / HD1
G12	GND
G13	$\overline{\text{PSDVAL}}$
G14	GND
G15	V_{DDH}

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
G16	V_{DDH}
G17	$\overline{TEA}$
G18	MODCK3 / TC2 / BNKSEL2
G19	$\overline{POE}$ / $\overline{PSDRAS}$ / PGPL2
H1	PB30 / FCC2:MII:RX_DV / SCC2:TXD / TDBM2:L1RXD
H2	PD31 / SCC1:RXD / $\overline{DRACK1}$ / $\overline{DONE1}$
H3	PC31 / BRG1O / CLK1 / $\overline{TGATE1}$
H4	PB31 / FCC2:MII:TX_ER / SCC2:RXD / TDMB2:L1TXD
H5	GND
H6	TDI
H7	GND
H13	Reserved / BADDR31 / $\overline{IRQ5}$
H14	Reserved / BADDR30 / $\overline{IRQ3}$
H15	GND
H16	V_{DD}
H17	$\overline{BR}$
H18	ALE
H19	$\overline{PWE4}$ / $\overline{PSDDQM4}$ / $\overline{PBS4}$
J1	PA29 / FCC1:UTOPIA8:TXSOC / FCC1:MII:TX_ER
J2	PD30 / SCC1:TXD / DMA:$\overline{DRACK2}$/$\overline{DONE2}$
J3	PC30 / EXT1 / BRG2O / CLK2 / $\overline{TOUT1}$
J4	V_{DD}
J5	GND
J6	GND
J7	PA30 / FCC1:UTOPIA8:TXCLAV / FCC1:UTOPIA8:TXCLAV0 / FCC1:MII:CRS / FCC1:HDLC and transparent:$\overline{RTS}$
J13	$\overline{TA}$
J14	GND
J15	V_{DDH}
J16	V_{DDH}
J17	PSDAMUX / PGPL5
J18	$\overline{PGTA}$ / PUPMWAIT / $\overline{PPBS}$ / PGPL4
J19	$\overline{PWE3}$ / $\overline{PSDDQM3}$ / $\overline{PBS3}$
K1	PA28 / FCC1:UTOPIA8:$\overline{RXENB}$ / FCC1:MII:TX_EN
K2	PD29 / FCC1:UTOPIA8:RXADDR3 / FCC1:UTOPIA8:RXCLAV2 / SCC1:$\overline{RTS}$/TENA
K3	PC29 / SCC1:$\overline{CTS}$ / SCC1:CLSN / BRG3O / CLK3 / TIN2
K4	PB29 / FCC2:MII:TX_EN / TDMB2:L1RSYNC

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
K5	V_{DDH}
K6	GND
K7	GND
K13	GND
K14	$\overline{\text{PWE2}}$ / $\overline{\text{PSDDQM2}}$ / $\overline{\text{PBS2}}$
K15	GND
K16	V_{DDH}
K17	$\overline{\text{PWE1}}$ / $\overline{\text{PSDDQM1}}$ / $\overline{\text{PBS1}}$
K18	$\overline{\text{PWE0}}$ / $\overline{\text{PSDDQM0}}$ / $\overline{\text{PBS0}}$
K19	$\overline{\text{CS2}}$
L1	PA27 / FCC1:UTOPIA8:RXSOC / FCC1:MII:RX_DV
L2	PB28 / FCC2:RX_ER / FCC2:HDLC:$\overline{\text{RTS}}$ / SCC2:$\overline{\text{RTS}}$/TENA / TDMB2:L1TSYNC
L3	PC28 / SCC2:$\overline{\text{CTS}}$/CLSN / BRG4O / CLK4 / TIN1/$\overline{\text{TOUT2}}$
L4	V_{DD}
L5	GND
L6	GND
L7	PC27 / CLK5 / BRG5O / $\overline{\text{TGATE2}}$
L13	$\overline{\text{CS6}}$
L14	GND
L15	GND
L16	V_{DD}
L17	$\overline{\text{CS1}}$
L18	$\overline{\text{CS3}}$
L19	$\overline{\text{BCTL1}}$
M1	PB27 / FCC2:MII:COL / TDMC2:L1TXD
M2	PC26 / TMCLK / BRG6O / CLK6 / $\overline{\text{TOUT3}}$
M3	PB26 / FCC2:MII:CRS / TDMC2:L1RXD
M4	V_{DDH}
M5	GND
M6	PA26 / FCC1:UTOPIA8:RXCLAV / FCC1:UTOPIA8:RXCLAV0 / FCC1:MII:RX_ER
M7	PA16 / FCC1:UTOPIA8:RXD6 / FCC1:MII and HDLC nibble:RXD1
M13	A21
M14	A26
M15	GND
M16	$\overline{\text{CS0}}$
M17	$\overline{\text{CS5}}$
M18	$\overline{\text{CS7}}$

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
M19	$\overline{CS4}$
N1	PC25 / DMA:$\overline{DACK2}$ / BRG7O / CLK7 / TIN4
N2	PA25 / FCC1:UTOPIA8:TXD0 / SDMA:MSNUM0
N3	PB25 / FCC2:MII and HDLC nibble:TXD3 / TDMA1:nibble:L1TXD3 / TDMC2:L1TSYNC
N4	V_{DD}
N5	PC23 / EXT2 / DMA:$\overline{DACK1}$ / CLK9
N6	GND
N7	PD17 / FCC1:UTOPIA8:RXPRTY / SPI:SPIMOSI / BRG2O
N8	CLKIN
N9	GND
N10	PC6 / FCC1:UTOPIA8:RXADDR2 / FCC1:UTOPIA8:RXADDR2/RXCLAV1 / FCC1:$\overline{CD}$ / SI2:LIST2
N11	TSIZ3
N12	TT1
N13	TT0
N14	A1
N15	V_{DDH}
N16	V_{DDH}
N17	A28
N18	A30
N19	A31
P1	PC24 / DMA:DREQ2 / BRG8O / CLK8 / TIN3/$\overline{TOUT4}$
P2	PA24 / FCC1:UTOPIA8:TXD1 / SDMA:MSNUM1
P3	PB24 / FCC2:MII and HDLC nibble:TXD2 / TDMA1:nibble:L1RXD3 / TDMC2:L1RSYNC
P4	PA23 / FCC1:UTOPIA8:TXD2
P5	PB20 / FCC2:MII and HDLC nibble:RXD1 / TDMA1:nibble:L1TXD1 / TDMD2:L1RSYNC
P6	GND
P7	GND
P8	DLLIN
P9	GND
P10	PC4 / FCC2:$\overline{CD}$ / SMC1:SMRXD / SI2:LIST4
P11	GND
P12	GND
P13	GND
P14	GND
P15	GND

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
P16	V_{DD}
P17	A23
P18	A27
P19	A29
R1	PC22 / SI1:LIST1 / DREQ1 / CLK10
R2	SPARE1
R3	PA22 / FCC1:UTOPIA8:TXD3
R4	PB18 / FCC2:MII and HDLC nibble:RXD3 / I^2C:SCL
R5	PA19 / FCC1:UTOPIA8:TXD6 / FCC1:MII and HDLC nibble:TXD1
R6	V_{DDH}
R7	V_{DDH}
R8	V_{DD}
R9	V_{DDH}
R10	V_{DDH}
R11	V_{DD}
R12	V_{DDH}
R13	V_{DD}
R14	V_{DDH}
R15	V_{DDH}
R16	A15
R17	A19
R18	A24
R19	A25
T1	PB21 / FCC2:MII and HDLC nibble:RXD0 / FCC2:transparent and HDLC serial:RXD /TDMA1:nibble:L1TXD2 / TDMD2:L1TSYNC
T2	PB22 / FCC2:MII and HDLC nibble TXD0 / FCC2:transparent and HDLC serial TXD /TDMA1:nibble L1RXD1 / TDMD2:L1RXD
T3	PA20 / FCC1:UTOPIA8 TXD5 / FCC1:MII and HDLC nibble TXD2
T4	PA17 / FCC1:UTOPIA8 RXD7 / FCC1:MII and HDLC nibble RXD0 / FCC1:transparent and HDLC serial RXD
T5	PC13 / FCC1:UTOPIA8:TXADDR1 / SCC2:$\overline{\text{CTS}}$/CLSN / SI1:LIST4
T6	PC14 / FCC1:UTOPIA8:RXADDR0 / SCC1:$\overline{\text{CD}}$/RENA / SI1:LIST2
T7	V_{CCSYN1}
T8	CLKOUT
T9	PA12 / FCC1:UTOPIA8:RXD2 / SDMA:MSNUM3
T10	PC7 / FCC1:UTOPIA8:TXADDR2 / FCC1:UTOPIA8:TXADDR2/TXCLAV1 / FCC1:$\overline{\text{CTS}}$ / SI1:LIST1
T11	PA6 / TDMA1:L1RSYNC

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

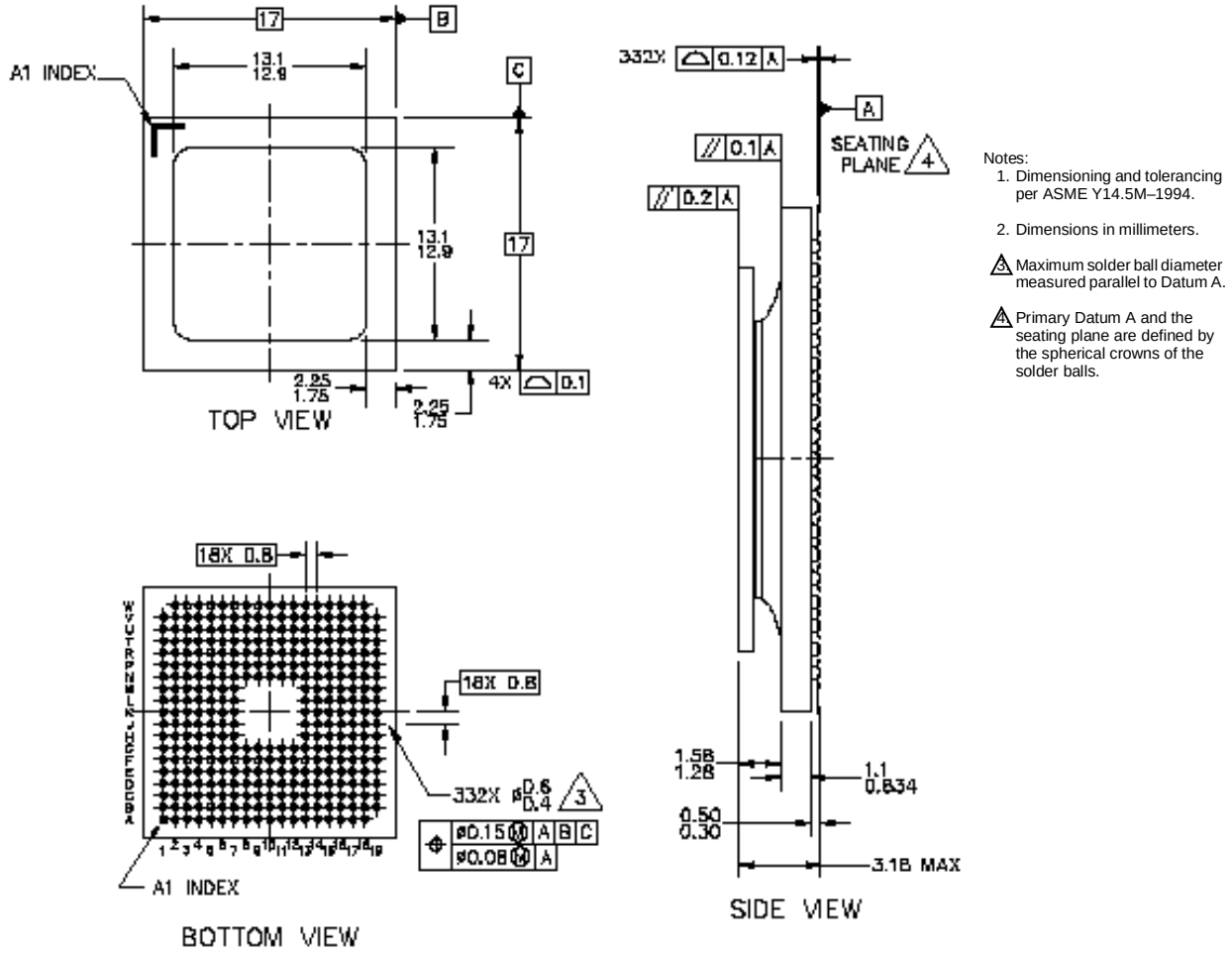
Number	Signal Name
T12	$\overline{\text{AACK}}$
T13	$\overline{\text{TS}}$
T14	A3
T15	V_{DDH}
T16	A12
T17	A16
T18	A20
T19	A22
U1	PA21 / FCC1:TXD4 / FCC1:MII and HDLC nibble TXD3
U2	PB19 / FCC2:MII and HDLC nibble RXD2 / I^2C:SDA
U3	PD18 / FCC1:UTOPIA8:RXADDR4 / FCC1:UTOPIA8:RXCLAV3 / SPI:SPICLK
U4	PD16 / FCC1:UTOPIA8:TXPRTY / SPI:SPIMISO
U5	$\overline{\text{NMI}}$
U6	$\overline{\text{RSTCONF}}$
U7	GND_{SYN1}
U8	PA13 / FCC1:UTOPIA8:RXD3 / SDMA:MSNUM2
U9	PA10 / FCC1:UTOPIA8:RXD0 / SDMA:MSNUM5
U10	PA8 / SMC2:SMRXD / TDMA1:serial L1RXD / TDMA1:nibble L1RXD0
U11	SPARE5
U12	$\overline{\text{ARTRY}}$
U13	$\overline{\text{TBST}}$
U14	TT2
U15	A4
U16	A8
U17	A11
U18	A17
U19	A18
V1	PB23 / FCC2:MII and HDLC nibble:TXD1 / TDMA1:nibble:L1RXD2 / TDMD2:L1TXD
V2	PD19 / FCC1:UTOPIA8:TXADDR4 / FCC1:UTOPIA:TXCLAV3 / SPI:$\overline{\text{SPISEL}}$ / BRG1O
V3	PC15 / FCC1:UTOPIA8:TXADDR0 / SCC1:$\overline{\text{CTS}}$/CLSN / SMC2:SMTXD
V4	PC12 / FCC1:UTOPIA8:RXADDR1 / SCC2:$\overline{\text{CD}}$/RENA / SI1:LIST3
V5	$\overline{\text{NMI\_OUT}}$
V6	$\overline{\text{HRESET}}$
V7	GND_{SYN}
V8	PA11 / FCC1:UTOPIA8:RXD1 / SDMA:MSNUM4
V9	PD7 / FCC1:UTOPIA8:TXADDR3 / FCC1:UTOPIA8:TXCLAV2 / SMC1:$\overline{\text{SMSYN}}$

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
V10	PA7 / SMC2:$\overline{\text{SMSYN}}$ / TDMA1:L1TSYNC
V11	$\overline{\text{ABB}}$ / $\overline{\text{IRQ2}}$
V12	$\overline{\text{BG}}$
V13	TSIZ0
V14	TT3
V15	A2
V16	A6
V17	A9
V18	A13
V19	A14
W2	PA18 / FCC1:UTOPIA8:TXD7 / FCC1:MII and HDLC nibble:TXD0 / FCC1:transparent and HDLC serial:TXD
W3	PA15 / FCC1:UTOPIA8:RXD5 / FCC1:MII and HDLC nibble:RXD2
W4	$\overline{\text{SRESET}}$
W5	$\overline{\text{PORESET}}$
W6	TEST
W7	V_{CCSYN}
W8	PA14 / FCC1:UTOPIA8 RXD4 / FCC1:MII and HDLC nibble:RXD3
W9	PA9 / SMC2:SMTXD / TDMA1:serial:L1TXD /TDMA1:nibble:L1TXD0
W10	PC5 / FCC2:$\overline{\text{CTS}}$ / SMC1:SMTXD / SI2:LIST3
W11	$\overline{\text{IRQ7}}$ / $\overline{\text{INT\_OUT}}$
W12	TSIZ2
W13	TSIZ1
W14	TT4
W15	A0
W16	A5
W17	A7
W18	A10

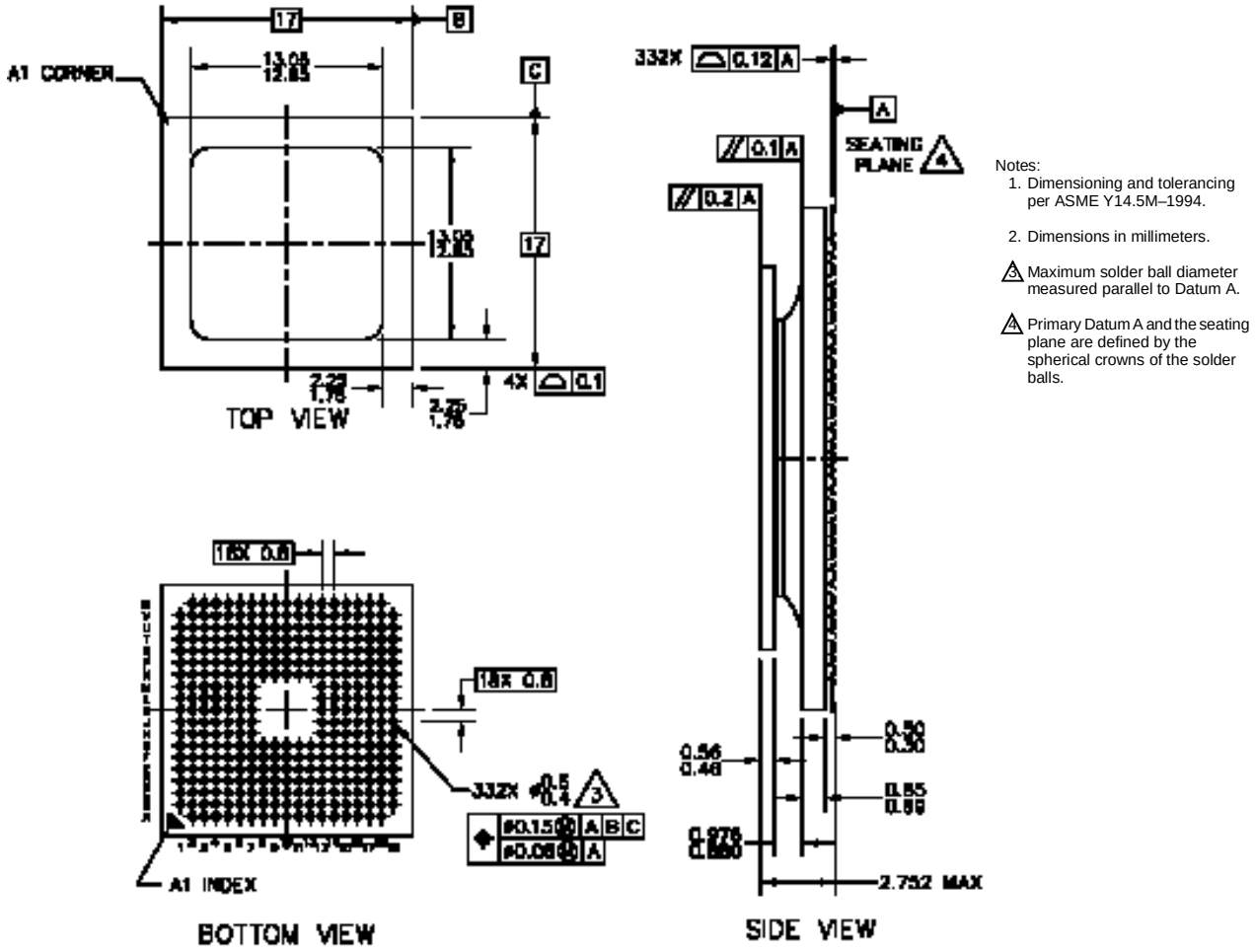
3.3 Lidded FC-PBGA Package Mechanical Drawings

There are two types of packages used with the MSC8101. The package shown in **Figure 3-3** is used with pre-production MSC8101 devices using mask set 2K42A and all devices using mask set 1K87M. Final production MSC8101 devices with mask set 2K42A use the package shown in **Figure 3-4**.



CASE 1473-01

Figure 3-3. Case 1473-01 Mechanical Information, 332-pin Lidded FC-PBGA Package (mask set 1K87M devices and mask set 2K42A pre-production devices)



CASE 1495-01

Figure 3-4. Case 1495-01 Mechanical Information, 332-pin Lidded FC-PBGA Package (mask set 2K42A production devices)

Chapter 4

Design Considerations

4.1 Thermal Design Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the following:

Equation 1: $T_J = T_A + (P_D \bullet \theta_{JA})$

where

T_A = ambient temperature °C

θ_{JA} = package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$ in W

$P_{INT} = I_{DD} \times V_{DD}$ in W—chip internal power

$P_{I/O}$ = power dissipation on output pins in W—user determined

The user should set T_A and P_D such that T_J does not exceed the maximum operating conditions. In case T_J is too high, the user should either lower the ambient temperature or the power dissipation of the chip.

4.2 Electrical Design Considerations

The input voltage must not exceed the I/O supply V_{DDH} by more than 2.5 V at any time, including during power-on reset. In turn, V_{DDH} can exceed V_{DD}/V_{CCSYN} by more than 3.3 V during power-on reset, but for no more than 100 ms. V_{DDH} should not exceed V_{DD}/V_{CCSYN} by more than 2.1 V during normal operation. V_{DD}/V_{CCSYN} must not exceed V_{DDH} by more than 0.4 V at any time, including during power-on reset. Therefore the recommendation is to use “bootstrap” diodes between the power rails, as shown in **Figure 4-1.**.

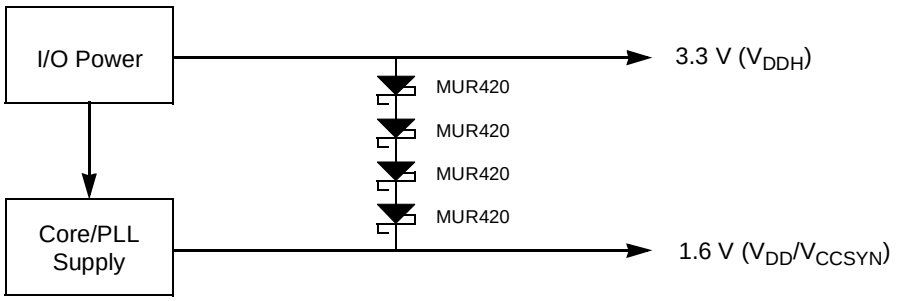


Figure 4-1. Bootstrap Diodes for Power-Up Sequencing

Select the bootstrap diodes such that a nominal V_{DD}/V_{CCSYN} is sourced from the V_{DDH} power supply until the V_{DD}/V_{CCSYN} power supply becomes active. In **Figure 4-1.**, four MUR420 Schottky barrier diodes are connected in series; each has a forward voltage (V_F) of 0.6 V at high currents, so these diodes provide a 2.4 V drop, maintaining 0.9 V on the 1.6 V power line. Once the core/PLL power supply stabilizes at 1.6 V, the bootstrap diodes will be reverse biased with negligible leakage current. The V_F should be effective at the current levels required by the processor. Do not use diodes with a nominal V_F that drops too low at high current.

4.3 Power Considerations

The internal power dissipation consists of three components:

$$P_{INT} = P_{CORE} + P_{SIU} + P_{CPM}$$

Power dissipation depends on the operating frequency of the different portions of the chip. For the 2K42A mask set, **Table 2A-5** provides typical power values at the specified operating frequencies. For the 1K87M mask set, **Table 2B-5** provides typical power values at the specified operating frequencies. To determine the typical power dissipation for a given set of frequencies, use the following equations:

$$P_{CORE}(f) = ((P_{CORE} - P_{LCO})/f_{CORE}) \times f_{COREA} + P_{LCO}$$
$$P_{CPM}(f) = ((P_{CPM} - P_{LCP})/f_{CPM}) \times f_{CPMA} + P_{LCP}$$
$$P_{SIU}(f) = ((P_{SIU} - P_{LSI})/f_{SIU}) \times f_{SIUA} + P_{LSI}$$

Where:

- f_{CORE} is the core frequency, f_{SIU} is the SIU frequency, and f_{CPM} is the CPM frequency specified in **Table 2A-5** or **Table 2B-5** in MHz
- f_{COREA} is the actual core frequency, F_{SIUA} is the actual SIU frequency, and F_{CPMA} is the actual CPM frequency in MHz
- P_{LCO}, P_{LSI}, and P_{LCP} are the leakage power values specified in **Table 2A-5** or **Table 2B-5**
- All power numbers are in mW
- Power consumption is assumed to be linear with frequency. The first part of each equation computes a mw/MHz value that is then scaled based on the actual frequency used.

To determine a total power dissipation in a specific application, you must add the power values derived from the above set of equations to the value derived for I/O power consumption using the following equation for each output pin:

Equation 2: $P = C \times V_{DDH}^2 \times f \times 10^{-3}$

Where: P = power in mW, C = load capacitance in pF, f = output switching frequency in MHz.

For an application in which external data memory is used in a 32-bit single bus mode and no other outputs are active, the core runs at 200 MHz, the CPM runs at 100 MHz and the SIU runs at 50 MHz, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every second cycle with 10% of address pins switching.
- External data memory writes occurs once every eight cycles with 50% of data pins switching.
- Each address and data pin has a 30 pF total load at the pin.
- The application operates at V_{DDH} = 3.3 V.

Since the address pins switch once at every second cycle, the address pins frequency is a quarter of the bus frequency (that is, 25 MHz).

For the same reason the data pins frequency is 3.125 MHz.

Table 4-1. Power Dissipation

Pins	# of pins switching	× C	× V_{DDH}^2	× f × 10^{-3}	Power in mW
Address	4	× 30	× 3.3^2	× 12.5×10^{-3}	16.25
Data, $\overline{HRD}$, $\overline{HRW}$	34	× 30	× 3.3^2	× 3.125×10^{-3}	34.75
CLKOUT	1	× 30	× 3.3^2	× 50×10^{-3}	16
Total $P_{I/O}$					67

Calculating internal power (from **Table 2B-5** values):

P_{CORE} (200) = (($P_{CORE} - P_{LCO}$)/300) × 200 + P_{LCO} =((350 – 3) / 300 × 200 + 3 = 234
P_{CPM} (100) = (($P_{CPM} - P_{LCP}$) / 200) × 100 + P_{LCP} = ((320 – 6) / 200) × 100 + 6 = 163
P_{SIU} (50) = (($P_{SIU} - P_{LSI}$) / 100) × 50 + P_{LSI} = ((80 – 2) / 100) × 50 + 2 = 41
$P_{INT} = P_{CORE}(200) + P_{CPM}(100) + P_{SIU}(50)$ = 234 + 163 + 41 = 438
$P_D = P_{INT} + P_{I/O}$ = 438 + 67 = 505

Maximum allowed ambient temperature is:

$T_A = T_J - (PD \times \theta_{JA})$

4.4 Layout Practices

Each V_{CC} and V_{DD} pin on the MSC8101 should be provided with a low-impedance path to the board's power supply. Similarly, each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC}, V_{DD}, and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MSC8101 have fast rise and fall times. Printed circuit board (PCB) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PCB trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC}, V_{DD}, and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

There are 2 pairs of PLL supply pins: V_{CCSYN}-GND_{SYN} and V_{CCSYN1}-GND_{SYN1}. Each pair supplies one PLL. To ensure internal clock stability, filter the power to the V_{CCSYN} and V_{CCSYN1} inputs with a circuit similar to the one in **Figure 4-2.**. To filter as much noise as possible, place the circuit as close as possible to V_{CCSYN} and V_{CCSYN1}. The 0.01-µF capacitor should be closest to V_{CCSYN} and V_{CCSYN1}, followed by the 10-µF capacitor, the 10-nH inductor, and finally the 10-Ω resistor to V_{DD}. These traces should be kept short and direct.

GND_{SYN} and GND_{SYN1} should be provided with an extremely low impedance path to ground and should be bypassed to V_{CCSYN} and V_{CCSYN1}, respectively, by a 0.01-µF capacitor located as close as possible to the chip package. The user should also bypass GND_{SYN} and GND_{SYN1} to V_{CCSYN} and V_{CCSYN1} with a 0.01-µF capacitor as closely as possible to the chip package

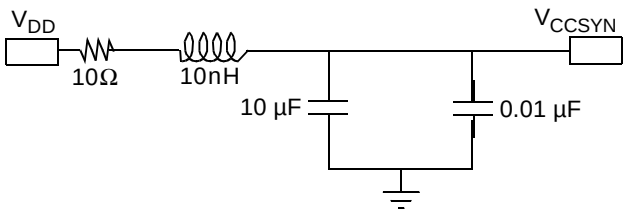


Figure 4-2. VCCSYN and VCCSYN1 Bypass

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Ordering Information

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Mask Set	Core Frequency (MHz)	Order Number
MSC8101	1.6 V core 3.3 V I/O	Lidded Flip Chip Plastic Ball Grid Array (FC-PBGA)	332	2K42A	250	MSC8101M1250C
					275	MSC8101M1375C
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					275	TBD
					300	TBD

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