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The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M64897GP**PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC****DESCRIPTION**

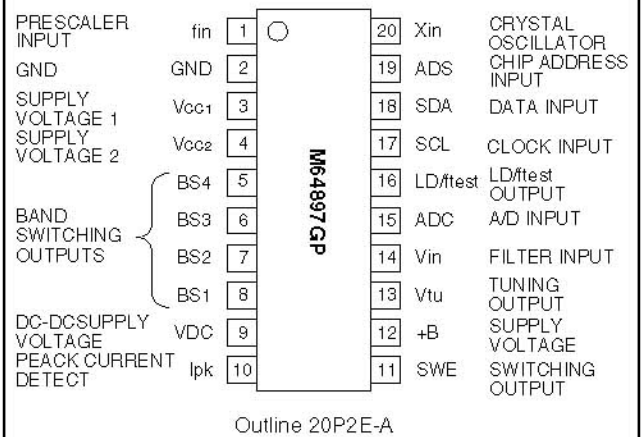
The M64897GP is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR/PC using I²C BUS control. It contains the prescaler with operating up to 1.3GHz, 4 band drivers and DC-DC converter for Tuning voltage.

FEATURES

- Built-in DC-DC converter for Tuning voltage
- 4 integrated PNP band drivers (I_o=30mA, V_{sat}=0.2V typ@V_{cc1} to 10V)
- Built-in prescaler with input amplifier (f_{max}=1.3GHz)
- PLL lock/unlock status display out put (Built-in pull up resistor)
- X tal 4MHz is used to realize 3 type of tuning steps (Divider ratio 1/512, 1/640, 1/1024)
- Software compatible with M64894
- Built-in Power on reset system
- Small Package (SSOP)

APPLICATION

PC, TV, VCR tuners

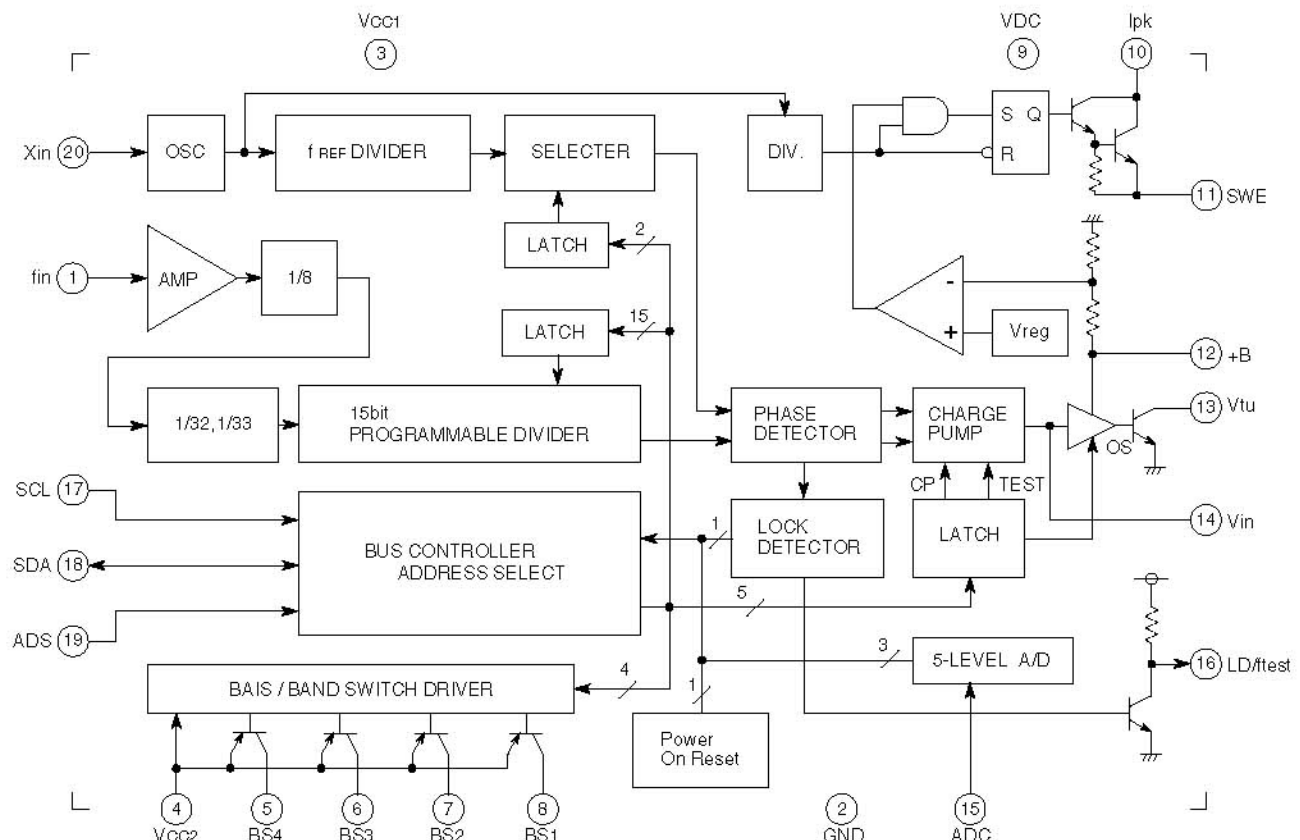
PIN CONFIGURATION (TOP VIEW)**RECOMMENDED OPERATING CONDITION**

Supply voltage range.....V_{cc1}=4.5 to 5.5V

V_{cc2}=V_{cc1} to 10V

Rated supply voltage.....V_{cc1}=5V

V_{cc2}=V_{cc1}

BLOCK DIAGRAM

PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC**DESCRIPTION OF PIN**

Pin No.	Symbol	Pin name	Function
1	f in	Prescaler input	Input for the VCO frequency.
2	GND	GND	Ground to 0V.
3	Vcc1	Power supply voltage 1	Power supply voltage terminal. 5.0V 0.5V
4	Vcc2	Power supply voltage 2	Power supply for band switching, Vcc1 to 10V
5	BS4	Band switching outputs	PNP open collector method is used. When the band switching data is "H", the output is ON. When it is "L", the output is OFF.
6	BS3		
7	BS2		
8	BS1		
9	VDC	DC-DC power supply voltage	DC-DC power supply voltage terminal. 5.0V 0.5V
10	l _{pk}	Peak current detect	When potential difference with VDC terminal becomes more than 0.33V by current limiting detector of DC-DC converter, the listing rises with off.
11	SWE	Switching output	DC-DC converter oscillator output.
12	+B	Power supply voltage	Power supply voltage for turning voltage.
13	V _{tu}	Tuning output	This supplies the tuning voltage.
14	V _{in}	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f _{1/N}) is ahead compared to the reference frequency (f _{REF}), the "source" current state becomes active. If it is behind, the "sink" current becomes active. If the phases are the same, the high impedance state becomes active.
15	LD/test	Lock detect /Test port	Lock detector output. When loop of phase locked loop locked it, it rises with "H" level in "L" level or unlock. In control byte data input, the programmable freq. divider output and reference freq. output is selected by the test mode.
16	ADC	AD converter input	A/D conversion of the input voltage.
17	SCL	Clock input	Data is read into the shift register when the clock signal falls.
18	SDA	Data input	Input for band SW and programmable freq. divider set up. In lead mode, it outputs lock detector output and power down flag and a state of 5 level A/D converter.
19	ADS	Address switching input	Chip address sets it up with the input condition of terminal.
20	X in	This is connected to the crystal oscillator	4.0MHz crystal oscillator is connected.

ABSOLUTE MAXIMUM RATINGS (Ta=-20 °C to +75 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc1	Supply voltage 1	Pin3	6.0	V
Vcc2	Supply voltage 2	Pin4	10.8	V
V _i	Input voltage	Not to exceed Vcc1	6.0	V
V _o	Output voltage	f _{REF} output	6.0	V
V _{BSOFF}	Voltage applied when the band output is OFF		10.8	V
I _{BSON}	Band output current	per 1 band output circuit	40.0	mA
t _{BSON}	ON the time when the band output is ON	40mA per 1 band output circuit 3circuits are pn at same time,	10	sec
P _d	Power dissipation	Ta=75 °C	255	mW
T _{opr}	Operating temperature		-20 to +75	°C
T _{stg}	Storage temperature		-40 to +125	°C

PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC**RECOMMENDED OPERATING CONDITIONS** ($T_a = -20\text{ }^{\circ}\text{C}$ to $+75\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc1	Supply voltage 1	Pin3	4.5 to 5.5	V
Vcc2	Supply voltage 2	Pin4	Vcc1 to 10.0	V
f _{opr1}	Operating frequency (1)	Crystal oscillation circuit	4.0	V
f _{opr2}	Operating frequency (2)		80 to 1300	MHz
I _{BDL}	Band output current 5 to 8	Normally 1 circuit is on. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.	0 to 30	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20\text{ }^{\circ}\text{C}$ to $+75\text{ }^{\circ}\text{C}$, unless otherwise noted, Vcc1=5.0V, Vcc2=9.0V)

Symbol	Parameter		Test pin	Test conditions	Limits			Unit
					Min.	Typ.	Max.	
V _{IH}	Input terminals	"H" input voltage	17 to 18		3.0		V _{CC1} +0.3	V
V _{IL}		"L" input voltage	17 to 18				1.5	V
I _{IH}		"H" input current	17 to 18	V _{CC1} =5.5V, V _i =4.0V			10	μA
I _{IL}		"L" input current	17/18	V _{CC1} =5.5V, V _i =0.4V		-4/-14	-10/-30	μA
V _{OL}	SDA output	"L" output voltage	18	V _{CC1} =5.5V, I _c =3mA			0.4	V
I _{Lo}		Leak current	18	V _{CC1} =5.5V, V _o =5.5V			10	μA
V _{OH}	Lock output	"H" output voltage	16	V _{CC1} =5.5V	5.0			V
V _{OL}		"L" output voltage	16	V _{CC1} =5.5V	-	0.3	0.5	V
V _{BS}	Band SW	output voltage	5 to 8	V _{CC2} =9V, I _o =-30mA	11.6	11.8		V
I _{oIK1}		Leak current	5 to 8	V _{CC2} =9V, Band SW is OFF V _o =0V			-10	μA
V _{toH}	Tuning output	output voltage "H"	13	+B=31V	30.5			V
V _{toL}		output voltage "L"	13	+B=31V		0.2	0.4	V
I _{cpo}	Charge pump	"H" output current	14	V _{CC1} =5.0V, V _o =2.5V		270	370	μA
I _{cpLK}		Leak current	14	V _{CC1} =5.0V, V _o =2.5V			50	nA
I _{CC1}	Supply current 1		3	V _{CC1} =5.5V		20	30	mA
I _{CC2A}	Supply current 2	4 circuits OFF	4	V _{CC2} =9V			0.3	mA
I _{CC2B}		1 circuits ON, Output open	4	V _{CC2} =9V		4.0	6.0	mA
I _{CC2C}		Output current 30mA	4	V _{CC2} =9V, I _o =-30mA		34.0	36.0	mA
DC-DC Converter								
I _{CCdc}	Supply current (action)		9	V _{CC1} =5.5V		1.3	3.0	mA
V _{do}	Output voltage		12	V _{CC1} =5.5V	28	31	35	V
f _{osc}	OSC frequency		11	V _{CC1} =5.5V		571		kHz
V _{ipk}	Current limit detect voltage		10	V _{CC1} =5.5V		330		mV

The typical values are at Vcc1=5.0V, Vcc2=9.0V, T_a=+25 °C.

PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC
SWITCHING CHARACTERISTICS (Ta=-20 °C to +75 °C, unless otherwise noted, Vcc1=5.0V, Vcc2=9.0V)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
f _{opr}	Prescaler operating frequency	1	Vcc1=4.5 to 5.5V Vin=Vinmin to Vinmax	80		1300	MHz
Vin	Operation input voltage	1	Vcc1=4.5 to 5.5V	850 to 100MHz	-24	4	dBm
				100 to 950MHz	-27	4	
				950 to 1300MHz	-15	4	
f _{scl}	Clock pulse frequency	17	Vcc1=4.5 to 5.5V	0		100	kHz
t _{BUF}	Bus free time	18	Vcc1=4.5 to 5.5V	4.7			s
t _{HD_{STA}}	Data hold time	17	Vcc1=4.5 to 5.5V	4			s
t _{LOW}	SCL low hold time	17	Vcc1=4.5 to 5.5V	4.7			s
t _{HIGH}	SCL high hold time	17	Vcc1=4.5 to 5.5V	4			s
t _{SU_{STA}}	Set up time	17, 18	Vcc1=4.5 to 5.5V	4.7			s
t _{HD_{DAT}}	Data hold time	17, 18	Vcc1=4.5 to 5.5V	0			s
t _{SU_{DAT}}	Data set up time	17, 18	Vcc1=4.5 to 5.5V	250			ns
t _R	Rise time	17, 18	Vcc1=4.5 to 5.5V			1000	ns
t _F	Fall time	17, 18	Vcc1=4.5 to 5.5V			300	ns
t _{SU_{STO}}	Set up time	17, 18	Vcc1=4.5 to 5.5V	4			s

PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC**METHOD OF SETTING DATA**

The input information to consist of 2 or data of 4 bytes to lead to Chip Address is received in I²C bus receiver. It shows a definition of bus protocol admitted in the following.

1_STA CA CB BB STO
 2_STA CA D1 D2 STO
 3_STA CA CB BB D1 D2 STO
 4_STA CA D1 D2 CB BB STO

STA : Start condition

STO : Stop condition

CA : Chip address

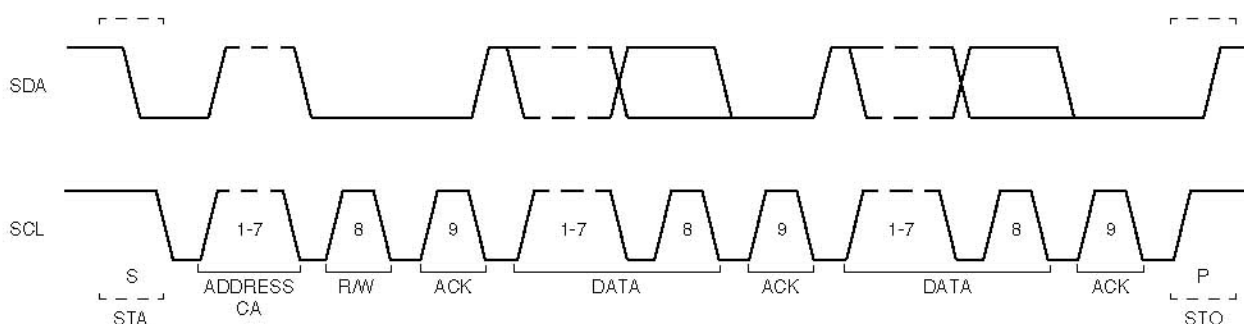
CB : Control data byte

BB : BandS.W. data byte

D1 : Divider data byte

D2 : Divider data byte

The information of 5 bytes necessary for circuit operation is chip address and control data, bandS.W. data of 2 bytes and divider byte of 2 bytes. After the chip address input, 2 or data of 4 bytes are received. Function bit is contained the first and the third data byte to distinguish between divider data and control data, band data, and "0" goes ahead of divider data, and "1" goes ahead of control data, bandS.W. data.

**Write mode format**

Byte	MSB								LSB
Address Byte	1	1	0	0	0	MA1	MA0	0	A
Devier Byte1	0	N14	N13	N12	N11	N10	N9	N8	A
Devier Byte2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Byte1	1	X	T2	T1	T0	Rsa	Rsb	OS	A
Band SW Byte	X	X	X	X	BS4	BS3	BS2	BS1	A

Read mode format

Byte	MSB								LSB
Address Byte	1	1	0	0	0	MA1	MA0	1	A
Status Byte1	POR	FL	X	X	X	A2	A1	A0	A

PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC
DATA CORDING EXAMPLE
Write mode format example

Byte	MSB								LSB	Condition in data setting
Address Byte	1	1	0	0	0	1	1	0	1	ADS input Vcc1
Devier Byte1	0	1	0	0	0	0	0	0	1	Divider ratio N=16544
Devier Byte2	1	0	1	0	0	0	0	0	1	
Control Byte1	1	1	0	0	0	0	1	0	1	fREF divider ratio 1/1024
Band SW Byte	0	0	0	0	1	0	0	0	1	BS4 output ON

$$f_{VCO} = N \cdot 8 \cdot f_{REF}$$

$$= 16544 \cdot 8 \cdot (4\text{MHz}/1024) = 517\text{MHz}$$

Read mode format example (Loop locked)

Byte	MSB								LSB	Condition in device
Address Byte	1	1	0	0	0	1	1	1	1	ADS Applied voltage 0.9 Vcc1 to Vcc1
Status Byte	0	1	1	1	1	0	1	1	1	ADS Applied voltage 0.45 Vcc1 to 0.6 Vcc1

Use data input for "1" so that the data of Read mode and Write mode return ACK signal "0" to micro computer in 9bits of each byte.

TEST MODE DATA SET UP METHOD
Test Mode Bit Set Up

X : Random, 0 or 1. normal "0"

MA1 ,MA0 : Programmable Address Bit

Address input voltage	MA1	MA0
0 to 0.1 Vcc1	0	0
Always valid	0	1
0.4 Vcc1 to 0.6 Vcc1	1	0
0.9 Vcc1 to Vcc1	1	1

N14 to N0 : How to set dividing ratio of the programable the divider

$$\text{Divider ratio} = N14(2^{14} = 16384) + \dots + N0(2^0 = 1)$$

Therefore, the range of divider N is 1,024 to 32,768

Example) $f_{VCO} = f_{REF} \cdot 8 \cdot N$

$$= 3.90625 \cdot 8 \cdot N$$

$$= 31.25 \cdot N \text{ (kHz)}$$

T2, T1, T0 : Setting up for the test mode

T2	T1	T0	Charge pump	12 pin condition	Mode
0	0	X	Normal operation	ADC input	Normal operation
0	1	X	High impedance	ADC input	Test mode
1	1	0	Sink	ADC input	Test mode
1	1	1	Source	ADC input	Test mode
1	0	0	High impedance	fREF output	Test mode
1	0	1	High impedance	f1/N output	Test mode

RSa, RSb : Set up for the reference Frequency divider ratio

RSa	RSb	Divider ratio
1	1	1/512
0	1	1/1024
X	0	1/640

OS : Set up the tuning amplifier

OS	Tuning voltage output	Mode
0	ON	Normal
1	OFF	Test

POR : Power on reset flag. "1" output at reset

FL : Lock detector flag. "1" output at locked, "0" output at unlocked

PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC
A2, A1, A0 : 5level A/D converter output data

ADC input voltage	A2	A1	A0
0.6 V _{CC1} to V _{CC1}	1	0	0
0.45 V _{CC1} to 0.6 V _{CC1}	0	1	1
0.3 V _{CC1} to 0.45 V _{CC1}	0	1	0
0.15 V _{CC1} to 0.3 V _{CC1}	0	0	1
0 to 0.15 V _{CC1}	0	0	0

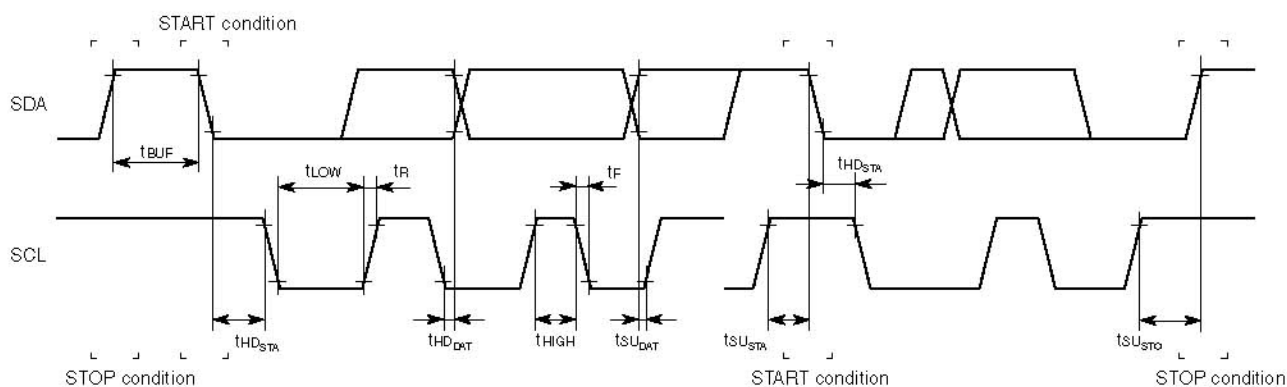
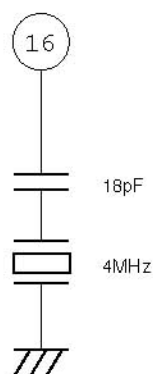
The voltage accuracy allowance range : 0.03 V_{CC1} [V]

Power on reset operation

(Initial state the power is turned ON)

BS4 to BS1 : OFF
 Charge pump : High impedance
 Tuning amplifier : OFF
 Charge pump current : 270 A
 Frequency divider ratio : 1/1024
 Lock detect : H

Charge pump current is replaced by 70 A when locks it by automatic change facility.

TIMING DIAGRAM

CRYSTAL OSCILLATOR CONNECTION DIAGRAM


Crystal oscillator characteristics
 Actual resistance : less than 300
 Load capacitance : 20pF

PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC**APPLICATION EXAMPLE**