

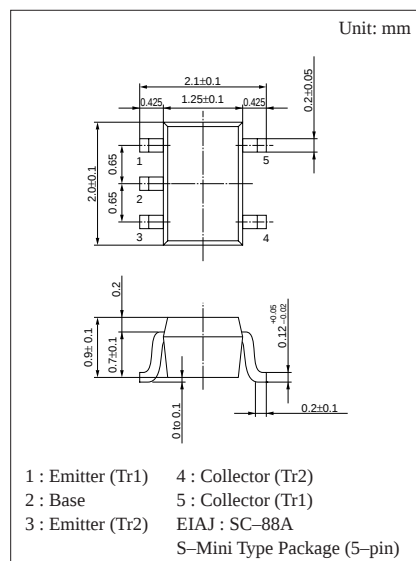
Silicon NPN epitaxial planer transistor

■ Features

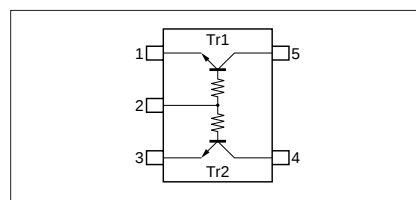
- Two elements incorporated into one package.
(Base-coupled transistors with built-in resistor)
- Reduction of the mounting area and assembly cost by one half.

- UN1210 $\times$ 2 elements

	Parameter	Symbol	Ratings	Unit
Rating of element	Collector to base voltage	V_{CBO}	50	V
	Collector to emitter voltage	V_{CEO}	50	V
	Collector current	I_C	100	mA
Overall	Total power dissipation	P_T	150	mW
	Junction temperature	T_j	150	°C
	Storage temperature	T_{strg}	-55 to +150	°C

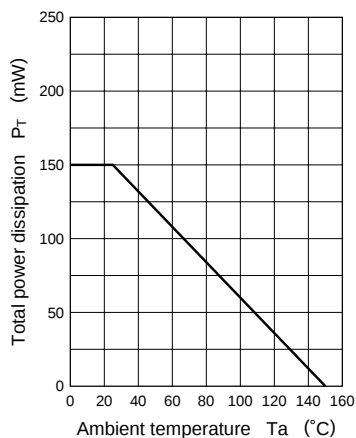
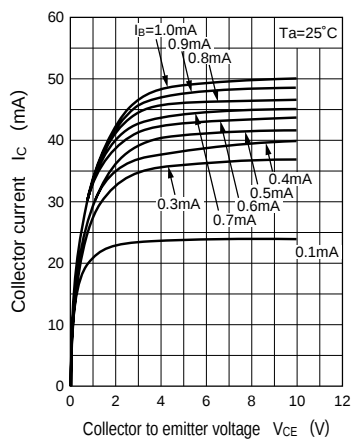
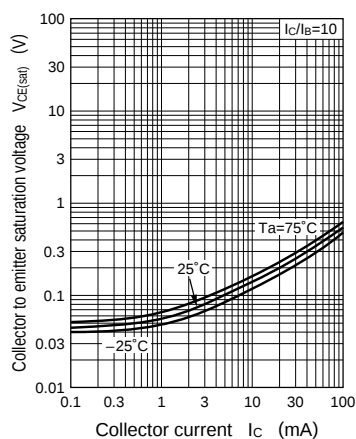
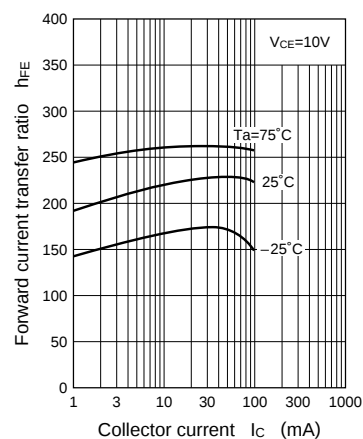
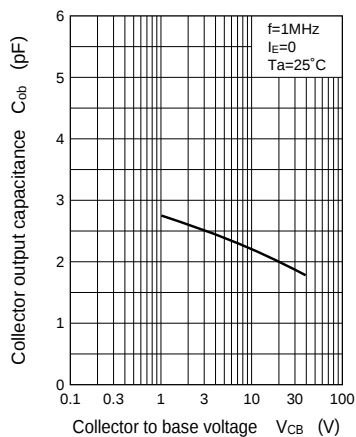
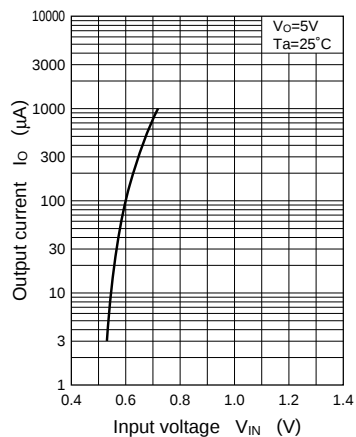


Internal Connection



Parameter	Symbol	Conditions	min	typ	max	Unit
Collector to base voltage	V_{CBO}	$I_C = 10\mu A, I_E = 0$	50			V
Collector to emitter voltage	V_{CEO}	$I_C = 2mA, I_B = 0$	50			V
Collector cutoff current	I_{CBO}	$V_{CB} = 50V, I_E = 0$			0.1	μA
	I_{CEO}	$V_{CE} = 50V, I_B = 0$			0.5	μA
Emitter cutoff current	I_{EBO}	$V_{EB} = 6V, I_C = 0$			0.01	mA
Forward current transfer ratio	h_{FE}	$V_{CE} = 10V, I_C = 5mA$	160		460	
Forward current transfer h_{FE} ratio	$h_{FE} (small/large)^{+1}$	$V_{CE} = 10V, I_C = 5mA$	0.5	0.99		
Collector to emitter saturation voltage	$V_{CE(sat)}$	$I_C = 10mA, I_B = 0.3mA$			0.25	V
Output voltage high level	V_{OH}	$V_{CC} = 5V, V_B = 0.5V, R_L = 1k\Omega$	4.9			V
Output voltage low level	V_{OL}	$V_{CC} = 5V, V_B = 2.5V, R_L = 1k\Omega$			0.2	V
Transition frequency	f_T	$V_{CB} = 10V, I_E = -2mA, f = 200MHz$		150		MHz
Input resistance	R_1		-30%	47	+30%	k Ω

*1 Ratio between 2 elements

$P_T - T_a$  $I_C - V_{CE}$  $V_{CE(sat)} - I_C$  $h_{FE} - I_C$  $C_{ob} - V_{CB}$  $I_O - V_{IN}$  $V_{IN} - I_O$ 