- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Parity Error Flag With Parity Generator/Checker**
- **Latch for Storage of the Parity Error Flag**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs**

SN54ABT853 . . . JT PACKAGE
SN74ABT853 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)

```
        ___
 OEA [ 1   24 ] VCC
  A1 [ 2   23 ] B1
  A2 [ 3   22 ] B2
  A3 [ 4   21 ] B3
  A4 [ 5   20 ] B4
  A5 [ 6   19 ] B5
  A6 [ 7   18 ] B6
  A7 [ 8   17 ] B7
  A8 [ 9   16 ] B8
 ERR [ 10  15 ] PARITY
 CLR [ 11  14 ] OEB
 GND [ 12  13 ] LE
```

SN54ABT853 . . . FK PACKAGE
(TOP VIEW)

```
        A2 A1 OEA NC VCC B1 B2
         4  3  2  1 28 27 26
   A3 [ 5              25 ] B3
   A4 [ 6              24 ] B4
   A5 [ 7              23 ] B5
   NC [ 8              22 ] NC
   A6 [ 9              21 ] B6
   A7 [ 10             20 ] B7
   A8 [ 11             19 ] B8
         12 13 14 15 16 17 18
        ERR CLR GND NC LE OEB PARITY
```

NC – No internal connection

description

The 'ABT853 8-bit to 9-bit parity transceivers are designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error ($\overline{ERR}$) output indicates whether or not an error in the B data has occurred. The output-enable ($\overline{OEA}$ and $\overline{OEB}$) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT853 transceivers provide true data at their outputs.
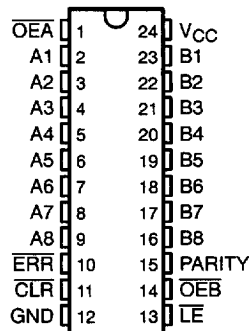
A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the $\overline{ERR}$ flag. The parity-error output can be passed, sampled, stored, or cleared from the latch using the latch-enable ($\overline{LE}$) and clear ($\overline{CLR}$) control inputs. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.
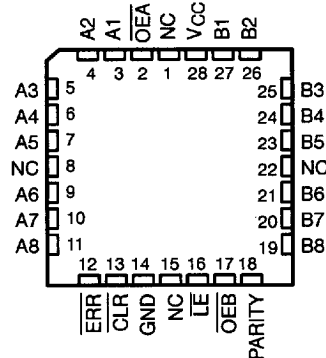
The SN74ABT853 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT853 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT853 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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SN54ABT853, SN74ABT853
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS198A – FEBRUARY 1991 – REVISED JULY 1994

FUNCTION TABLE

| INPUTS						OUTPUTS AND I/Os				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	LE	AI Σ OF H	Bi† Σ OF H	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	X	L	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	NC	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error flag register
H	H	H	X	X		Z	Z	Z	NC	Isolation§ (parity check)
		L	H	X	X				H	
		X	L	L Odd					H	
		X	L	H Even					L	
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume the $\overline{ERR}$ output was previously high.
§ In this mode, the $\overline{ERR}$ output (when clocked) shows inverted parity of the A bus.

logic symbol¶
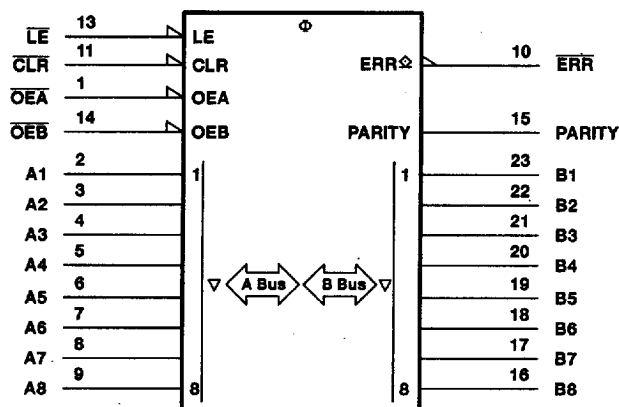
¶ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.
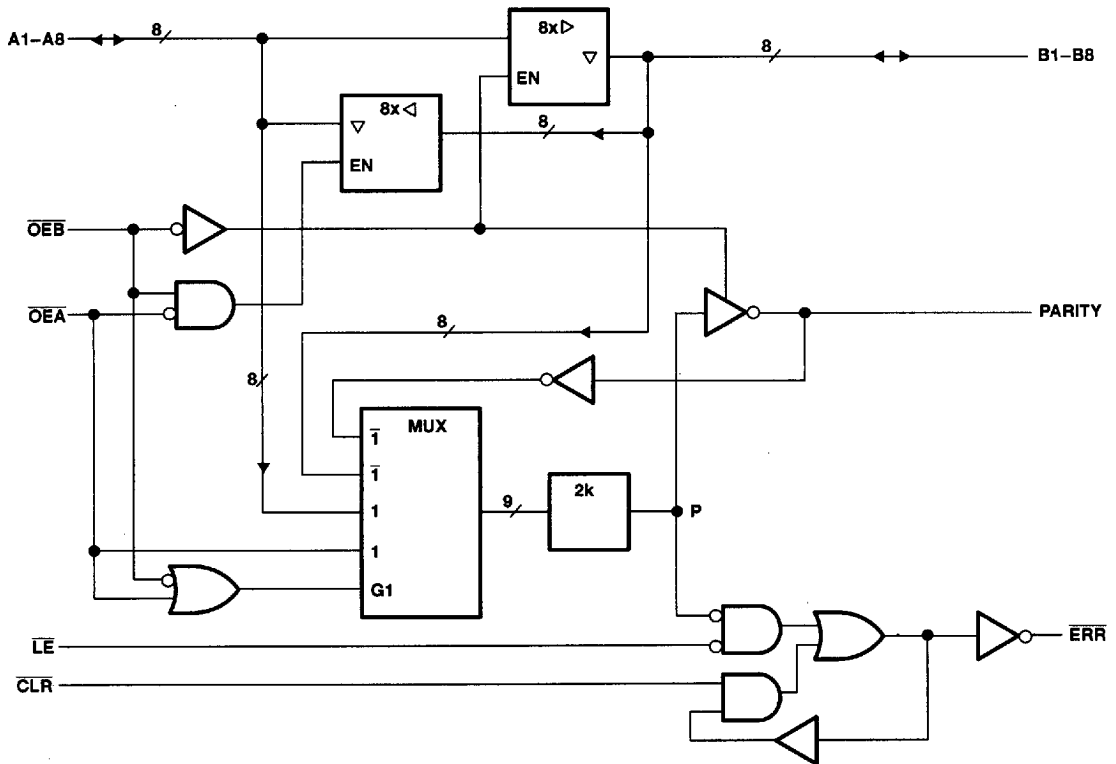
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logic diagram (positive logic)

PRODUCT PREVIEW

ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT $\overline{ERR}$	FUNCTION
$\overline{CLR}$	$\overline{LE}$	POINT P	$\overline{ERR}_{n-1}$ †		
L	L	L	X	L	Pass
		H		H	
H	L	L	X	L	Sample
		X	L	L	
		H	H	H	
L	H	X	X	H	Clear
H	H	X	L	L	Store
			H	H	

† The state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, $\overline{LE}$, or point P.

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SN54ABT853, SN74ABT853
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

PRODUCT PREVIEW

error-flag waveforms

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O .... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT853 .... 96 mA
SN74ABT853 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package .... 0.65 W
DW package .... 1.7 W
NT package .... 1.3 W
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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recommended operating conditions (see Note 3)

			SN54ABT853 MIN	SN54ABT853 MAX	SN74ABT853 MIN	SN74ABT853 MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_{OH}	High-level output voltage	$\overline{ERR}$		5.5		5.5	V
I_{OH}	High-level output current	Except $\overline{ERR}$		−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$ MIN	$T_A = 25°C$ TYP†	$T_A = 25°C$ MAX	SN54ABT853 MIN	SN54ABT853 MAX	SN74ABT853 MIN	SN74ABT853 MAX	UNIT
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2		−1.2		−1.2	V
V_{OH}	All outputs except $\overline{ERR}$	$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA	2.5			2.5		2.5		V
		$V_{CC} = 5$ V,	$I_{OH} = -3$ mA	3			3		3		
		$V_{CC} = 4.5$ V	$I_{OH} = -24$ mA	2			2				
			$I_{OH} = -32$ mA	2*					2		
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 24$ mA			0.55		0.55			V
			$I_{OL} = 64$ mA			0.55*				0.55	
I_{OH}	$\overline{ERR}$	$V_{CC} = 4.5$ V,	$V_{OH} = 5.5$ V								µA
I_I	Control inputs	$V_{CC} = 5.5$ V,	$V_I = V_{CC}$ or GND			±1		±1		±1	µA
	A or B ports					±100		±100		±100	
I_{IL}	A or B ports	$V_{CC} = 0$,	$V_I = $ GND			−50		−50		−50	µA
I_{OZH}‡		$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			50		50		50	µA
I_{OZL}‡		$V_{CC} = 5.5$ V,	$V_O = 0.5$ V			−50		−50		−50	µA
I_{off}		$V_{CC} = 0$,	V_I or $V_O \leq 4.5$ V			±100				±100	µA
I_{CEX}		$V_{CC} = 5.5$ V,	$V_O = 5.5$ V	Outputs high		50		50		50	µA
I_O§		$V_{CC} = 5.5$ V,	$V_O = 2.5$ V	−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	A or B ports	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high	1		250		250		250	µA
			Outputs low	24		30		30		30	mA
			Outputs disabled	0.5		250		250		250	µA
ΔI_{CC}¶		$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND				50		50		50	µA
C_i	Control inputs	$V_I = 2.5$ V or 0.5 V									pF
C_{io}	A or B ports	$V_O = 2.5$ V or 0.5 V									pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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