

Quad 2-input OR gate

74LVC32

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages upto 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC00 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC32 provides the 2-input OR function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level

L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	$C_L = 50 \text{ pF}$ $V_{CC} = 3.3 \text{ V}$	3.3	ns
C_i	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	50	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_i = \text{GND to } V_{CC}$

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC32D	14	SO	plastic	SO14/SOT108A
74LVC32DB	14	SSOP	plastic	SSOP14/SOT337
74LVC32PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

Quad 2-input OR gate

74LVC32

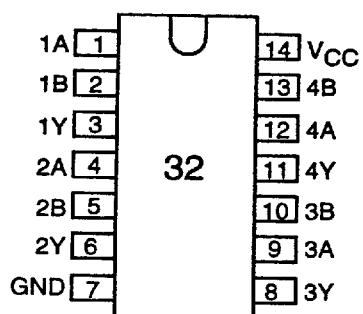


Fig.1 Pin configuration.

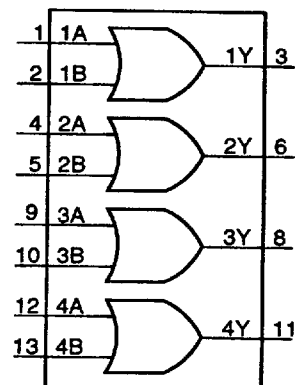


Fig.2 Logic symbol.

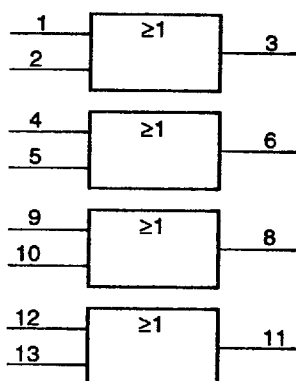


Fig.3 IEC Logic symbol.

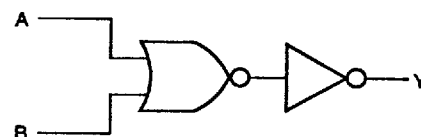


Fig.4 Logic diagram (one gate).

Quad 2-input OR gate

74LVC32

DC CHARACTERISTICS FOR 74LVC32

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

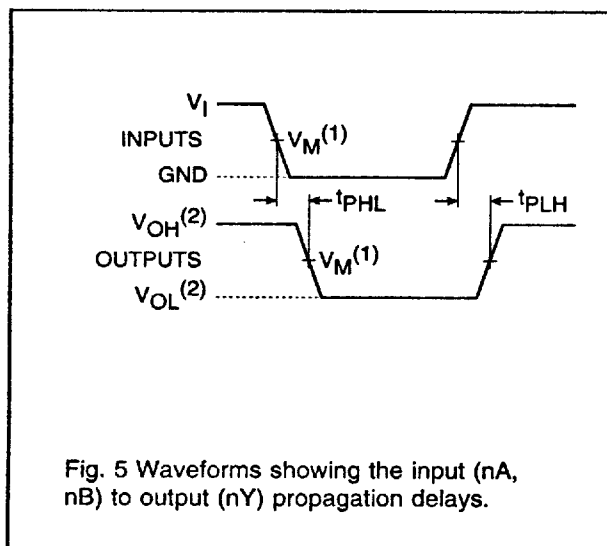
AC CHARACTERISTICS FOR 74LVC32

GND = 0 V; $t_i = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V _{cc} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	—	20	—	ns	1.2	Fig.5
		1.5	4.0	6.5		2.7	
		1.5	3.5*	6.0		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS



- Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
 (2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

