

Dual/Quad Micropower, 260 μ W C-Load Picoampere Bias Current JFET Input Op Amps

FEATURES

- **Input Bias Current:**
 2pA Max (LT1462A)
 20pA Max (LT1462, LT1463)
- **Supply Current per Amplifier: 45 μ A Max**
- Unity-Gain Stable for C-Load™ Up to 10nF
- Input Common Mode Range Includes Positive Rail
- Guaranteed Specs with ± 5 V, ± 15 V Supplies
- Gain Bandwidth Product: 175kHz Typ
- Slew Rate: 0.13V/ μ s Typ
- Guaranteed Matching Specifications
- Standard Pinout: SO-8, SO-14 Package

APPLICATIONS

- Battery-Powered Systems
- Photocurrent Amplifiers
- Low Frequency, Micropower Active Filters
- Low Droop Track-and-Hold Circuits

DESCRIPTION

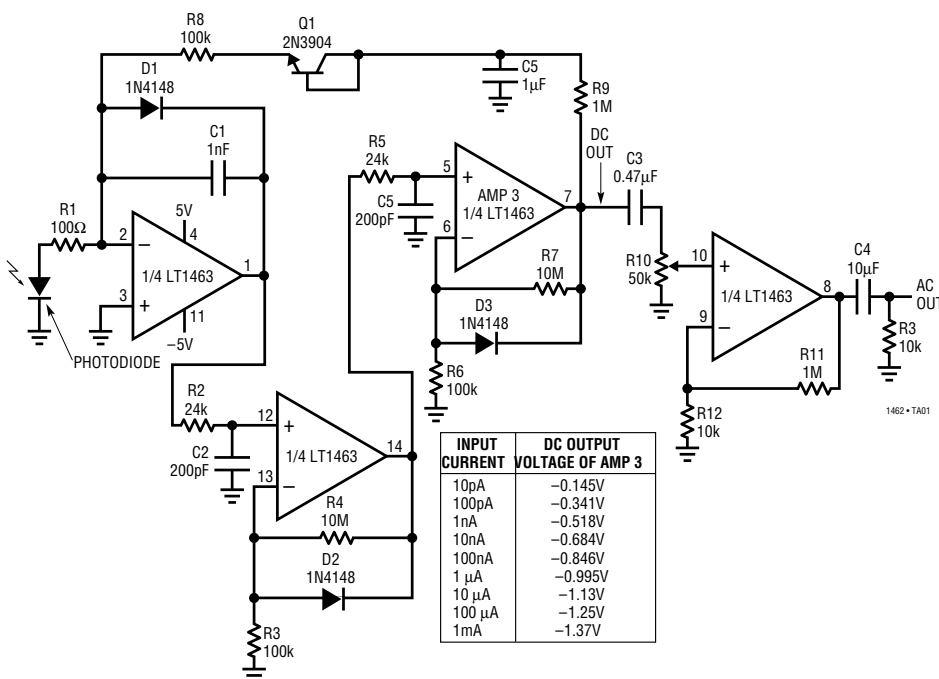
The LT[®]1462 (dual) and LT1463 (quad) are the first micropower op amps (45 μ A max per amp) to offer picoampere input bias currents (1pA typ) and unity gain stability for capacitive loads up to 10nF. The output can swing a 10k load to within 1.5V of either supply, just like op amps that require an order of magnitude more supply current. This unique combination of performance makes the LT1462/LT1463 ideal over a wide range of input and output impedances.

In the design and testing of the LT1462/LT1463, particular emphasis has been placed on optimizing performance in the low cost SO-8 (dual) and 14-lead SO package (quad) for ± 15 V and ± 5 V supplies. The input common mode range includes the positive rail. Slew rate (0.08V/ μ s min) and gain bandwidth product (125kHz min) are 100% tested. A full set of matching specifications is also provided.

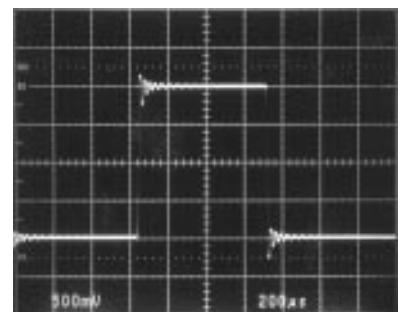
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 C-Load is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

Low Power Logging Amplifier



Small-Signal Response, $C_L = 10$ nF



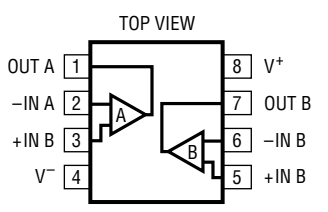
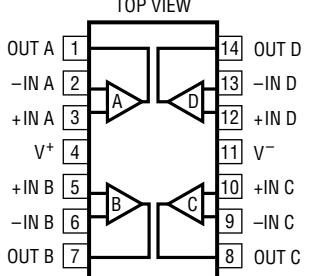
$A_V = 1$
 $V_S = \pm 5$ V, ± 15 V
 $C_L = 10$ nF

ABSOLUTE MAXIMUM RATINGS

Supply Voltage $\pm 20V$
 Differential Input Voltage $\pm 40V$
 Input Current 20mA
 Output Short-Circuit Duration Indefinite
 Operating Temperature Range $-40^{\circ}C$ to $85^{\circ}C$

Specified Temperature Range $-40^{\circ}C$ to $85^{\circ}C$
 Maximum Junction Temperature $150^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Lead Temperature (Soldering, 10 sec) $300^{\circ}C$

PACKAGE/ORDER INFORMATION

 N8 PACKAGE 8-LEAD PDIP S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 130^{\circ}C/W$ (N) $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 190^{\circ}C/W$ (S)	ORDER PART NUMBER	 N PACKAGE 14-LEAD PDIP S PACKAGE 14-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 110^{\circ}C/W$ (N) $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$ (S)
	LT1462ACN8 LT1462ACS8 LT1462CN8 LT1462CS8	
	S8 PART MARKING	
	1462 1462A	
		ORDER PART NUMBER
		LT1463CN LT1463CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^{\circ}C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1462AC			LT1462C/LT1463C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$V_S = \pm 5V$ $V_S = \pm 15V$	0.4 0.6	0.8 2.0		0.4 0.6	0.8 2.0		mV mV
I_{OS}	Input Offset Current	$V_S = \pm 5V$ $V_S = \pm 15V$	0.3 0.5	1.2 2.0		0.5 15			pA pA
I_B	Input Bias Current	$V_S = \pm 5V$ $V_S = \pm 15V$	± 0.5 ± 1	± 2.0 ± 3.0		± 1 ± 20			pA pA
e_n	Input Noise Voltage	0.1Hz to 10Hz	2			2			μV_{p-p}
	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 1000Hz$	92 76			92 76			$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Input Noise Current Density	$f_0 = 10Hz$, 1kHz (Note 3)	0.5			0.5			$fA/\sqrt{Hz}$
CMRR	Common Mode Rejection Ratio	$V_{CM} = -12.5V$ to $15V$	76	89		74	89		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 20V$	81	90		78	90		dB
R_{IN}	Input Resistance—Differential Common Mode Common Mode	$V_{CM} = -12.5V$ to $8V$ $V_{CM} = 8V$ to $15V$	10^{12} 10^{12} 10^{11}			10^{12} 10^{12} 10^{11}			Ω Ω Ω
C_{IN}	Input Capacitance		3			3			pF
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 10k$ $V_S = \pm 5V$, $V_O = \pm 2V$, $R_L = 10k$	100 50	600 200		100 50	600 200		V/mV V/mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1462AC			LT1462C/LT1463C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OUT}	Output Voltage Swing	$R_L = 10k$	± 13.5	± 13.7		± 13.5	± 13.7		V
		$R_L = 2k$	± 11.0	± 12.4		± 11.0	± 12.4		V
		$V_S = \pm 5V$, $R_L = 2k$	± 3.5	± 3.7		± 3.5	± 3.7		V
I_O	Output Current		± 13	± 17		± 13	± 17		mA
SR	Slew Rate	$R_L = 10k$ (Note 4)	0.08	0.13		0.08	0.13		V/ μs
GBW	Gain Bandwidth Product	$f = 10kHz$	125	175		125	175		kHz
I_S	Supply Current per Amplifier	$V_S = \pm 5V$		28	45		28	45	μA
				26	43		26	43	μA
	Channel Separation	$f = 10Hz$, $V_O = \pm 10V$, $R_L = 10k$		132			132		dB
V_{OS}	Offset Voltage Match (Note 7)	$V_S = \pm 5V$		0.5	1.3		0.5	1.3	mV
		$V_S = \pm 15V$		0.8	3.0		0.8	3.0	mV
ΔI_B^+	Noninverting Bias Current Match (Note 7)	$V_S = \pm 5V$		0.4	3.0				pA
		$V_S = \pm 15V$		0.5	4.0		0.5	20	pA
$\Delta CMRR$	Common Mode Rejection Match	(Notes 5, 7)	74	85		72	85		dB
$\Delta PSRR$	Power Supply Rejection Match	(Notes 5, 7)	78	88		76	88		dB

$V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1462AC			LT1462C/LT1463C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$V_S = \pm 5V$	●		0.5	1.4		0.5	1.4	mV
		$V_S = \pm 15V$	●		0.9	2.8		0.9	2.8	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 6)	●		7	20		7	20	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●		10	50		25	450	pA
I_B	Input Bias Current		●		60	150		150	750	pA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -12V$ to $15V$	●	75	88		72	88		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 20V$	●	80	89		76	89		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 10k$	●	90	600		90	600		V/mV
		$V_S = \pm 5V$, $V_O = \pm 2V$, $R_L = 2k$	●	45	140		45	140		V/mV
I_O	Output Current		●	± 11	± 14		± 11	± 14		mA
V_{OUT}	Output Voltage Swing	$R_L = 10k$	●	± 13.4	± 13.6		± 13.4	± 13.6		V
		$R_L = 2k$	●	± 10.5	± 12.1		± 10.5	± 12.1		V
		$V_S = \pm 5V$, $R_L = 2k$	●	± 3.4	± 3.6		± 3.4	± 3.6		V
SR	Slew Rate	$R_L = 10k$ (Note 4)	●	0.075	0.128		0.075	0.128		V/ μs
GBW	Gain Bandwidth Product	$f = 10kHz$	●	100	140		100	140		kHz
I_S	Supply Current per Amplifier	$V_S = \pm 5V$	●		31	45		31	45	μA
			●		28	43		28	43	μA
V_{OS}	Offset Voltage Match (Note 7)	$V_S = \pm 5V$	●		0.7	2.0		0.7	2.0	mV
		$V_S = \pm 15V$	●		0.9	3.5		0.9	3.5	mV
ΔI_B^+	Noninverting Bias Current Match (Note 7)		●		5	40		35	500	pA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1462AC			LT1462C/LT1463C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
$\Delta CMRR$	Common Mode Rejection Match	(Notes 5, 7)	●	73	84		70	84		dB
$\Delta PSRR$	Power Supply Rejection Match	(Notes 5, 7)	●	77	87		74	87		dB

$V_S = \pm 15V$, $V_{CM} = 0V$, $-40^\circ C \leq T_A \leq 85^\circ C$ (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1462AC			LT1462C/LT1463C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$V_S = \pm 5V$ $V_S = \pm 15V$	● ●		0.6 1.0	1.5 3.0		0.6 1.0	1.5 3.0	mV mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 6)	●		7	20		7	20	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●		40	150		60	700	pA
I_B	Input Bias Current		●		200	500		300	2500	pA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -12V$ to $15V$	●	74	87		70	87		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 20V$	●	79	88		74	88		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 10k$ $V_S = \pm 5V$, $V_O = \pm 2V$, $R_L = 2k$	● ●	80 40	500 120		80 40	500 120		V/mV V/mV
I_O	Output Current		●	± 10	± 13		± 10	± 13		mA
V_{OUT}	Output Voltage Swing	$R_L = 10k$ $R_L = 2k$ $V_S = \pm 5V$, $R_L = 2k$	● ● ●	± 13.2 ± 10.0 ± 3.2	± 13.4 ± 11.8 ± 3.4		± 13.2 ± 10.0 ± 3.2	± 13.4 ± 11.8 ± 3.4		V V V
SR	Slew Rate	$R_L = 10k$ (Note 4)	●	0.070	0.126		0.070	0.126		V/ μs
GBW	Gain Bandwidth Product	$f = 10kHz$	●	95	135		95	135		kHz
I_S	Supply Current per Amplifier	$V_S = \pm 5V$	● ●		33 31	50 48		33 31	50 48	μA μA
V_{OS}	Offset Voltage Match (Note 7)	$V_S = \pm 5V$ $V_S = \pm 15V$	● ●		0.8 1.0	2.5 4.0		0.8 1.0	2.5 4.0	mV mV
ΔI_B^+	Noninverting Bias Current Match (Note 7)		●		20	100		70	800	pA
$\Delta CMRR$	Common Mode Rejection Match	(Notes 5, 7)	●	72	83		68	83		dB
$\Delta PSRR$	Power Supply Rejection Match	(Notes 5, 7)	●	76	86		72	86		dB

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as 60% yield of parameter distributions of individual amplifiers, i.e., out of 100 LT1463s (or 100 LT1462s) typically 240 op amps (or 120) will be better than the indicated specification.

Note 2: The LT1462 and LT1463 are designed, characterized and expected to meet these extended temperature limits, but are not tested at $-40^\circ C$ and $85^\circ C$. Guaranteed I grade parts are available, consult factory.

Note 3: Current noise is calculated from the formula: $i_n = (2q i_b)^{1/2}$ where $q = (1.6)(10^{-19})$ coulomb. The noise of source resistors up to 1G swamps the contribution of current noise.

Note 4: Slew rate is measured in $A_V = -1$; input signal is $\pm 7.5V$, output is measured at $\pm 2.5V$.

Note 5: $\Delta CMRR$ and $\Delta PSRR$ are defined as follows:

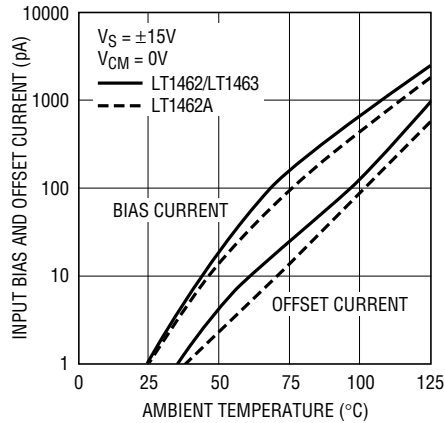
1. CMRR and PSRR are measured in $\mu V/V$ on the individual amplifiers.
2. The difference is calculated between the matching sides in $\mu V/V$.
3. The result is converted to dB.

Note 6: This parameter is not 100% tested.

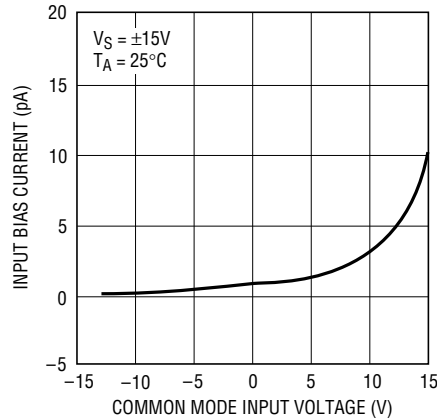
Note 7: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1463; between the two amplifiers on the LT1462.

TYPICAL PERFORMANCE CHARACTERISTICS

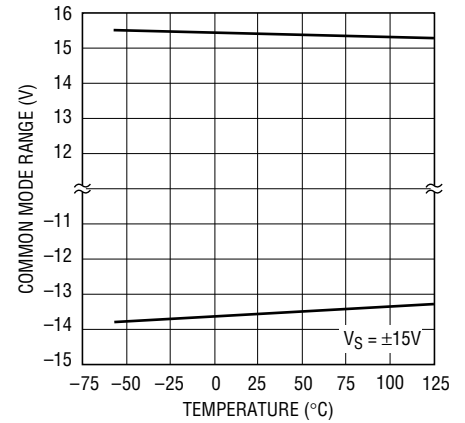
Input Bias and Offset Current vs Temperature



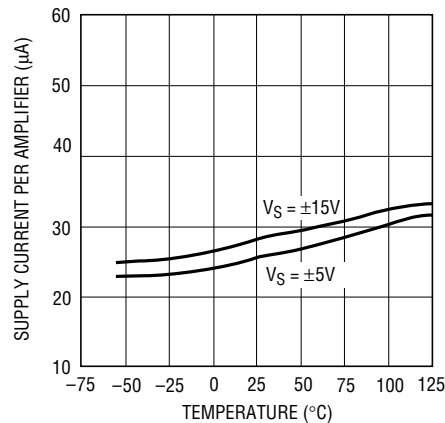
Input Bias Current Over the Common Mode Range



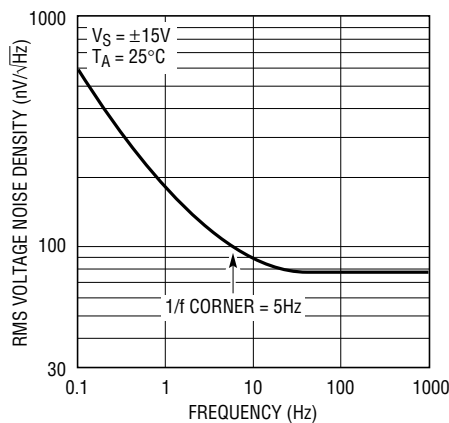
Common Mode Range vs Temperature



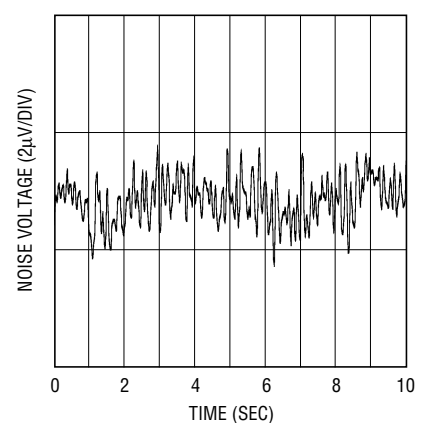
Supply Current vs Temperature



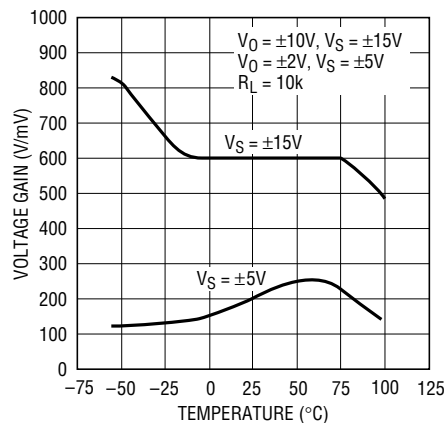
Voltage Noise vs Frequency



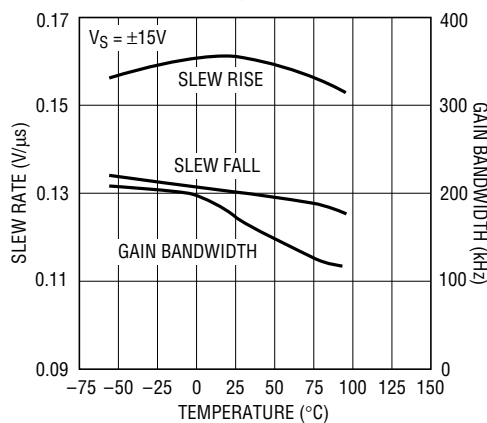
0.1Hz to 10Hz Noise



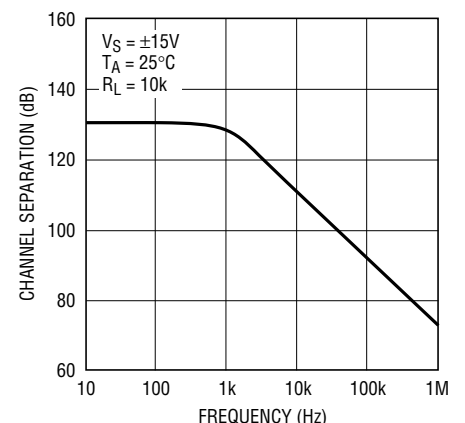
Voltage Gain vs Temperature



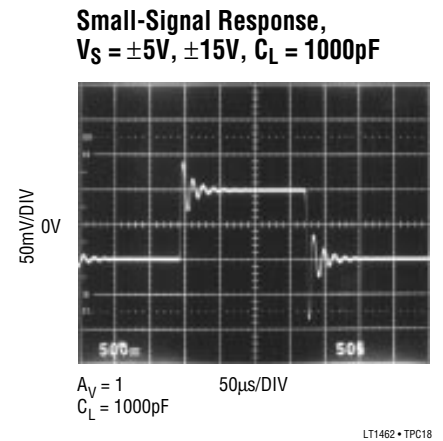
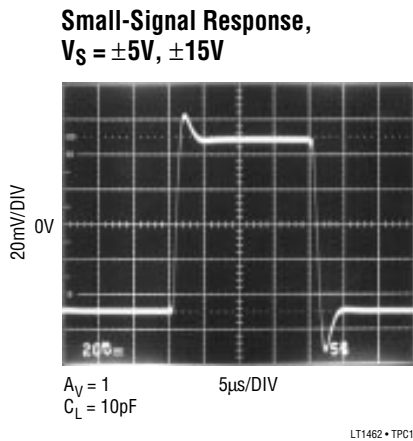
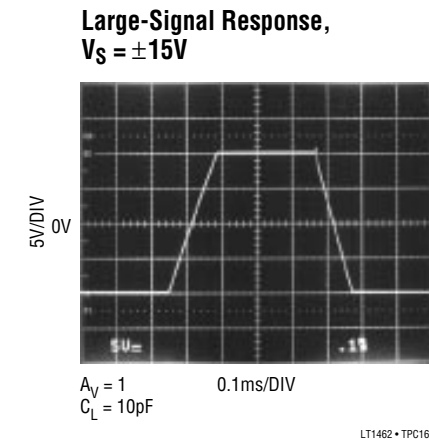
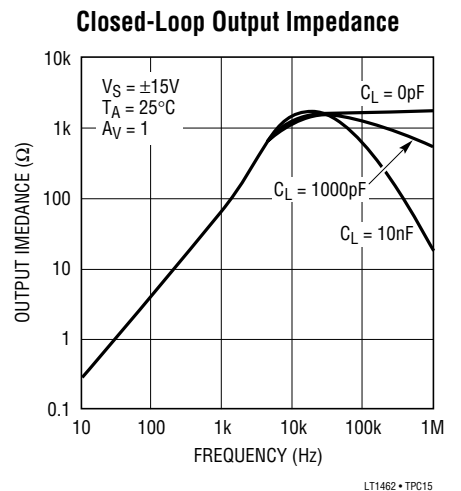
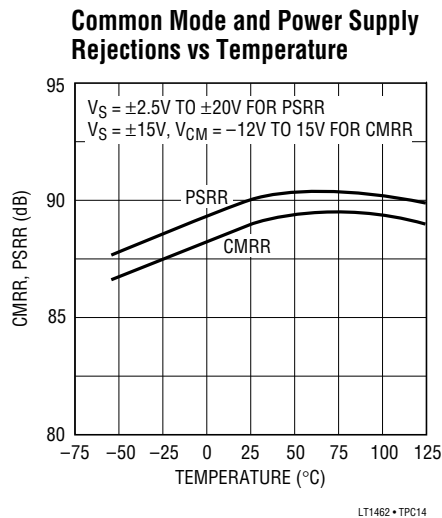
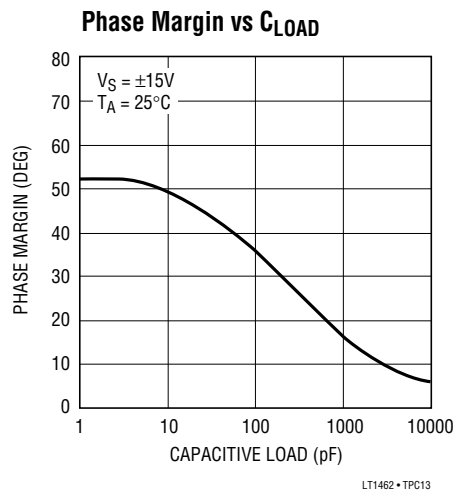
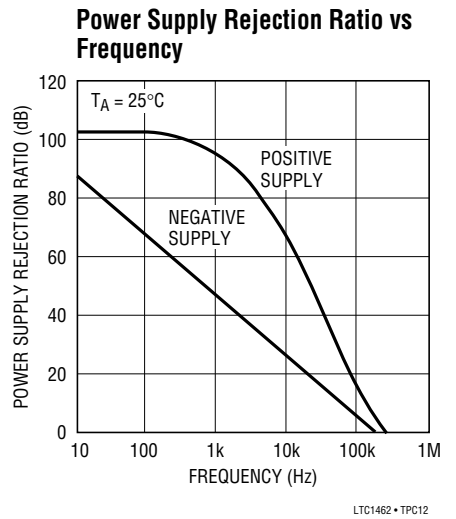
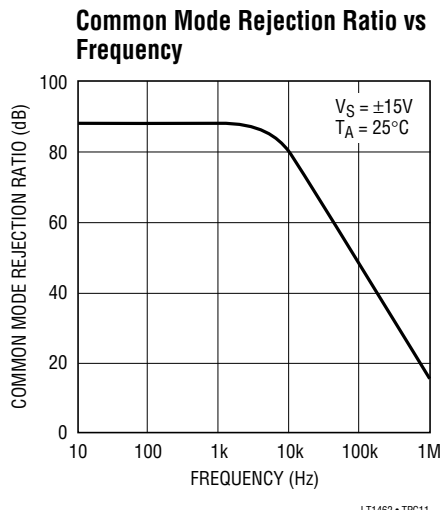
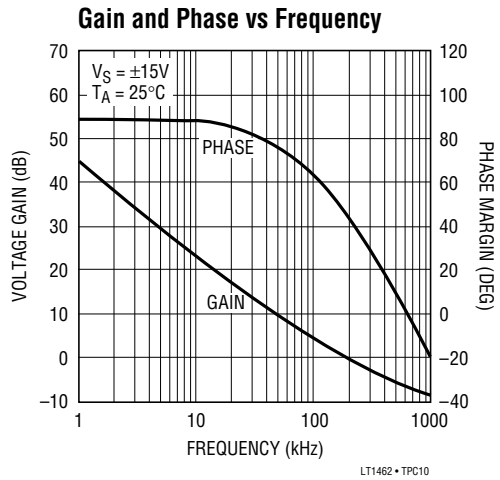
Slew Rate, Gain Bandwidth Product vs Temperature



Channel Separation vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS



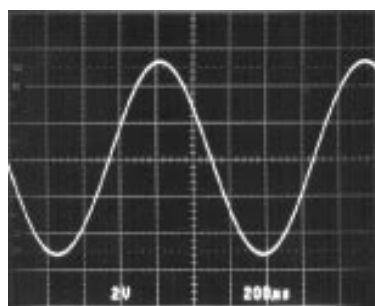
APPLICATIONS INFORMATION

Phase Reversal Protection

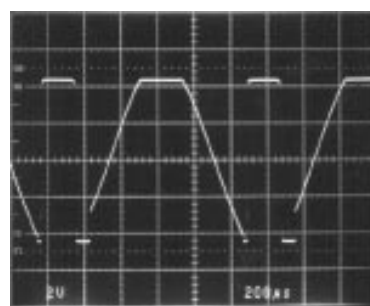
Most industry standard JFET input single, dual and quad op amps exhibit phase reversal at the output when the negative common mode limit at the input is exceeded. Common mode range is at a premium at $\pm 5V$ supplies. The Figures show a $\pm 5.2V$ sine wave input (Figure 1a), the

response of a competing JFET input op amp in the unity-gain follower mode (Figure 1b) and the response of the LT1462/LT1463 (Figure 1c).

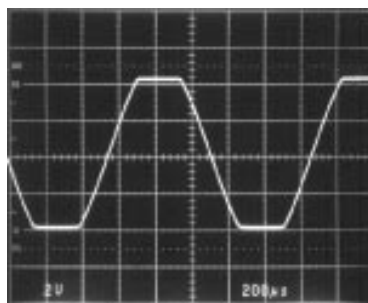
The phase reversal of Figure 1b can cause lock-up in servo systems. The LT1462/LT1463 does not phase-reverse when the common mode input is anywhere within the supplies.



(1a) $\pm 5.2V$ Sine Wave



(1b) Typical JFET Input Op Amp
with $\pm 5V$ Supplies

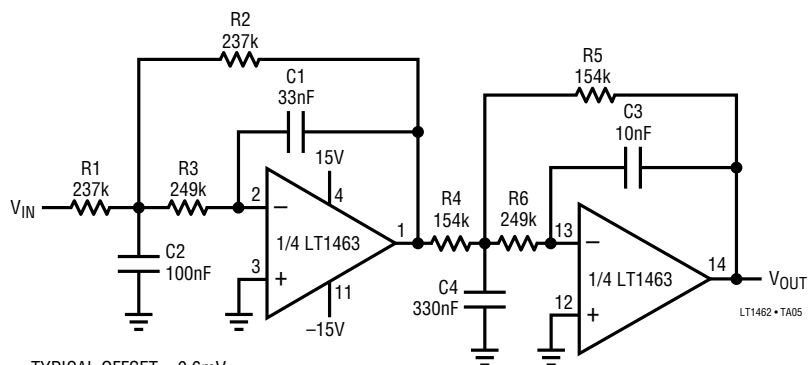


(1c) LT1462/LT1463 Output
with $\pm 5V$ Supplies

Figure 1. Voltage Follower with Input Exceeding the Common Mode Range ($V_S = \pm 5V$)

TYPICAL APPLICATIONS

10Hz 4th Order Chebyshev Lowpass Filter (0.01dB Ripple)



TYPICAL OFFSET $\approx 0.6\text{mV}$

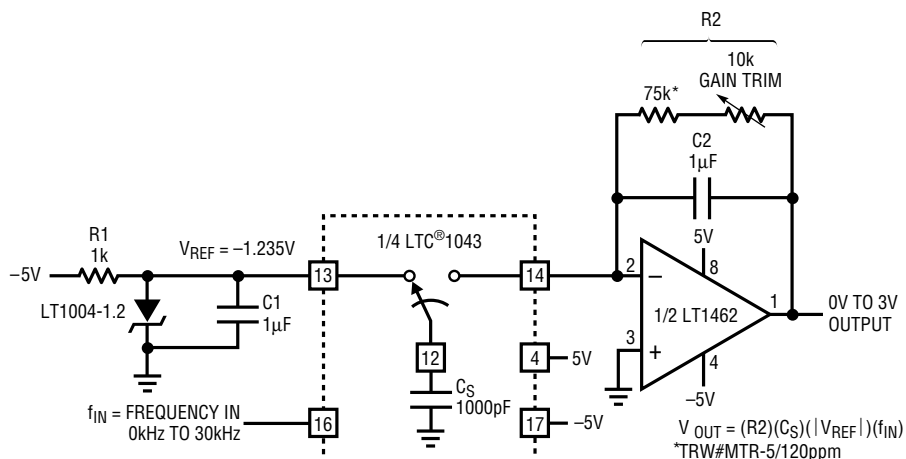
1% TOLERANCES

FOR $V_{IN} = 10\text{V}_{P-P}$, $V_{OUT} = -110\text{dB}$ AT $f > 300\text{Hz}$

$V_{OUT} = -6\text{dB}$ AT $f = 16\text{Hz}$

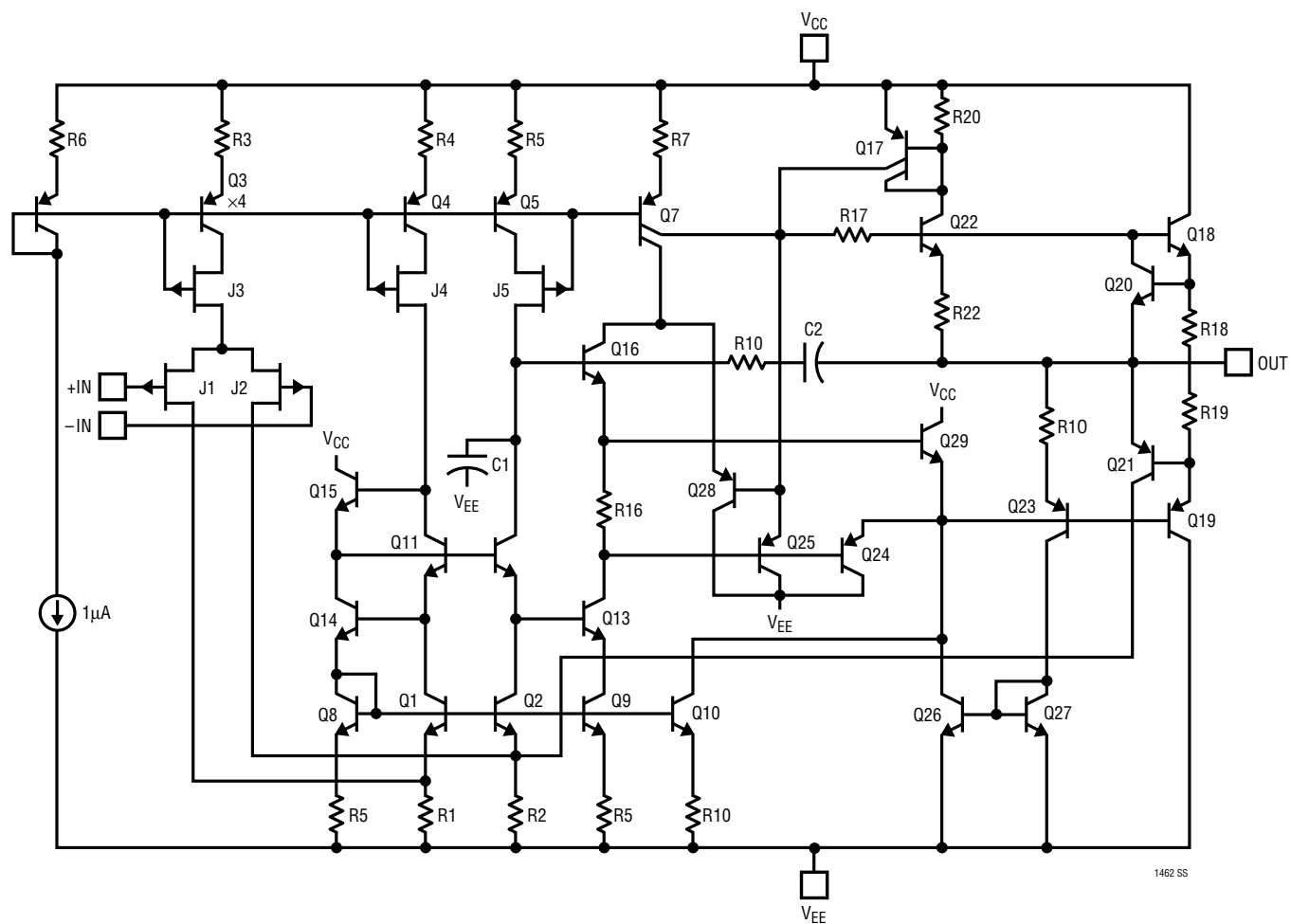
THE LOW INPUT BIAS CURRENTS ALLOW THE USE OF HIGH RESISTOR VALUES

Micropower 0.026% Frequency-to-Voltage Converter



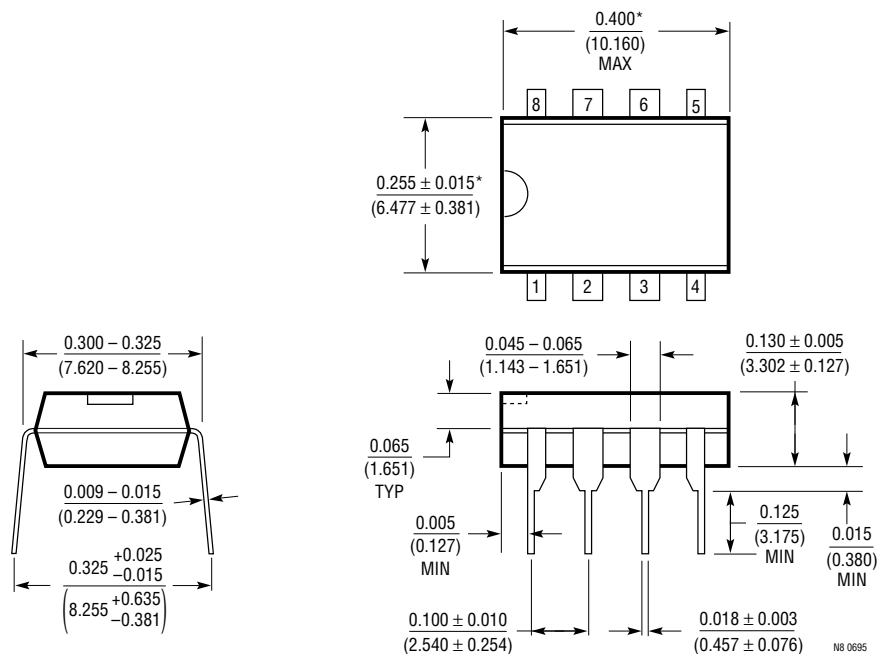
LT1462 • TA04

SIMPLIFIED SCHEMATIC



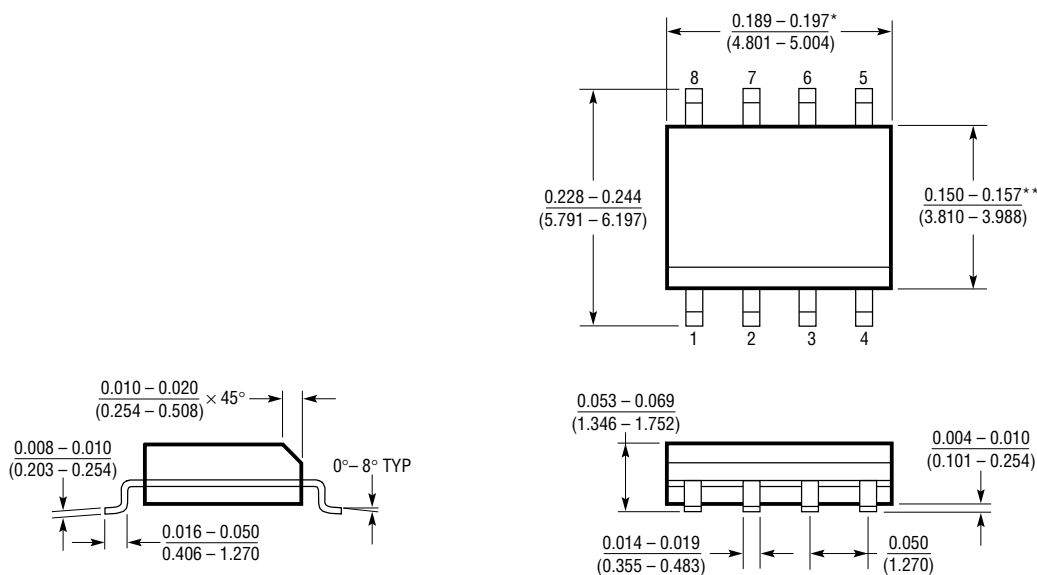
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N8 Package 8-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)

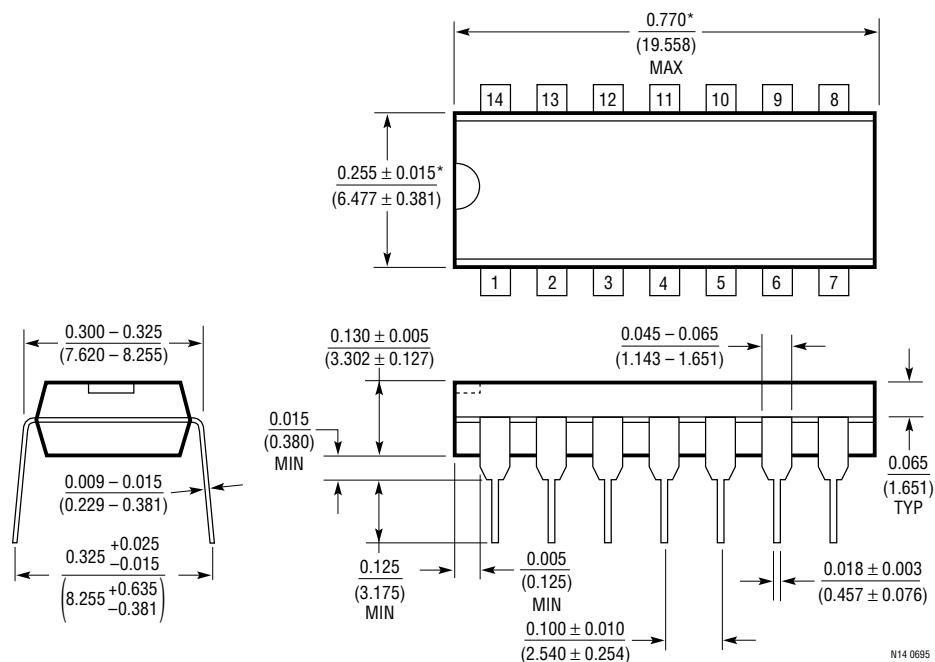


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

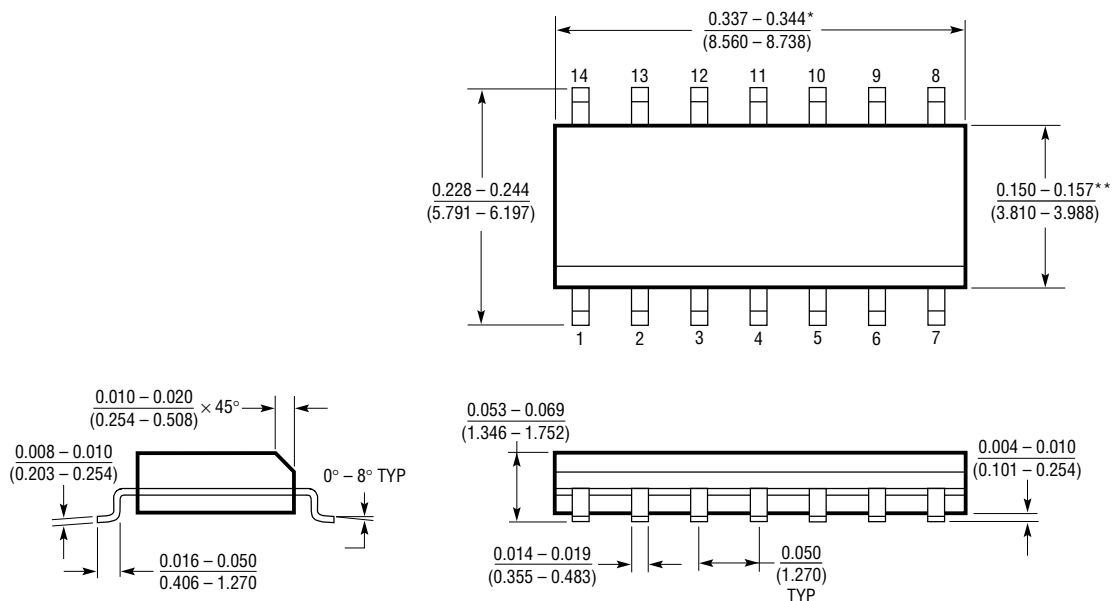
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N Package 14-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S Package 14-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

[illegible]

PART NUMBER	DESCRIPTION	COMMENTS
LT1057	Dual JFET Input, Precision, High Speed Op Amp	Fast Settling Time, 14V/ μ s Slew Rate, 5MHz GBW, 450 μ V $V_{OS(MAX)}$, 50pA $I_{OS(MAX)}$
LT1113	Dual Low Noise, Precision, JFET Input Op Amp	6nV/ $\sqrt{Hz}$ Input Noise Voltage Density, 480pA I_B , 6.3MHz GBW
LT1169	Dual Low Noise, Picoampere Bias Current, JFET Input Op Amp	20pA I_B , 8nV/ $\sqrt{Hz}$ e_n , 5.3MHz GBW, 1.5pF Input Capacitance
LT1457	Dual Precision JFET Input Op Amp C-Load	Drives 10,000pF Capacitive Load, 450 μ V $V_{OS(MAX)}$, 4 μ V/ $^{\circ}C$ Drift
LT1464/LT1465	Dual/Quad Micropower, C-Load Picoampere Bias Current JFET Input Op Amps	Drive 10nF Capacitive Loads, 1MHz GBW