82527
SERIAL COMMUNICATIONS CONTROLLER CONTROLLER AREA NETWORK PROTOCOL

Automotive

- Supports CAN Specification 2.0
  - Standard Data and Remote Frames
  - Extended Data and Remote Frames
- Programmable Global Mask
  - Standard Message Identifier
  - Extended Message Identifier
- 15 Message Objects of 8-Byte Data Length
  - 14 Tx/Rx Buffers
  - 1 Rx Buffer with Programmable Mask
- Flexible CPU Interface
  - 8-Bit Multiplexed
  - 16-Bit Multiplexed
  - 8-Bit Non-Multiplexed (Synchronous/Asynchronous)
  - Serial Interface
- Programmable Bit Rate
- Programmable Clock Output
- Flexible Interrupt Structure
- Flexible Status Interface
- Configurable Output Driver
- Configurable Input Comparator
- Two 8-Bit Bidirectional I/O Ports
- 44-Lead PLCC Package
- 44-Lead QFP Package
- Pinout Compatibility with the 82526

The 82527 serial communications controller is a highly integrated device that performs serial communication according to the CAN protocol. It performs all serial communication functions such as transmission and reception of messages, message filtering, transmit search, and interrupt search with minimal interaction from the host microcontroller, or CPU.

The 82527 is Intel's first device to support the standard and extended message frames in CAN Specification 2.0 Part B. It has the capability to transmit, receive, and perform message filtering on extended message frames. Due to the backwardly compatible nature of CAN Specification 2.0, the 82527 also fully supports the standard message frames in CAN Specification 2.0 Part A.

The 82527 features a powerful CPU interface that offers flexibility to directly interface to many different CPUs. It can be configured to interface with CPUs using an 8-bit multiplexed, 16-bit multiplexed, or 8-bit non-multiplexed address/data bus for Intel and non-Intel architectures. A flexible serial interface (SPI) is also available when a parallel CPU interface is not required.

The 82527 provides storage for 15 message objects of 8-byte data length. Each message object can be configured as either transmit or receive except for the last message object. The last message object is a receive-only buffer with a special mask design to allow select groups of different message identifiers to be received.

The 82527 also implements a global masking feature for message filtering. This feature allows the user to globally mask any identifier bits of the incoming message. The programmable global mask can be used for both standard and extended messages.

The 82527 PLCC offers hardware, or pinout, compatibility with the 82526. It is pin-to-pin compatible with the 82526 except for pins 9, 30, and 44. These pins are used as chip selects on the 82526 and are used as CPU interface mode selection pins on the 82527.

The 82527 is fabricated using Intel's reliable CHMOS III 5V technology and is available in either 44-lead PLCC or 44-lead QFP for the automotive temperature range (−40°C to +125°C).

July 2004 Order Number: 272250-007

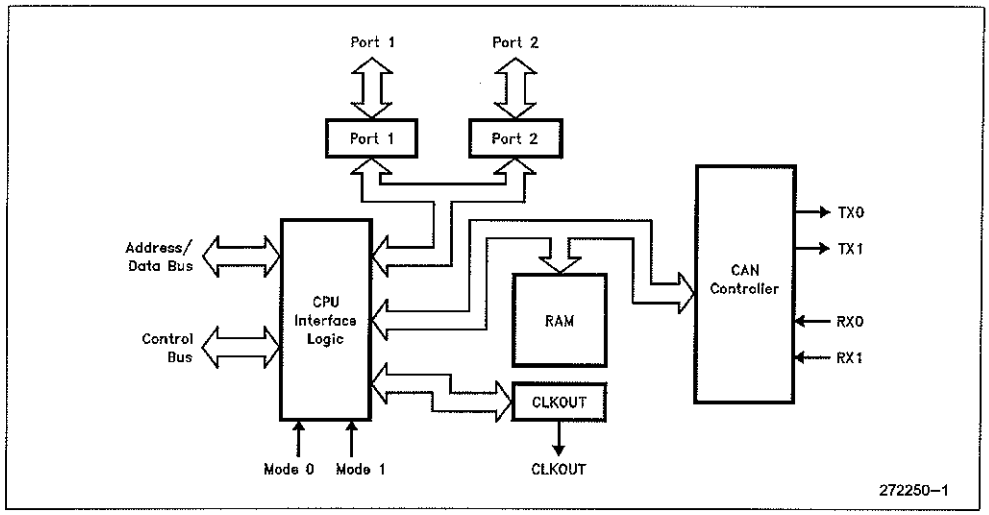

Figure 1 . 82527 Block Diagram

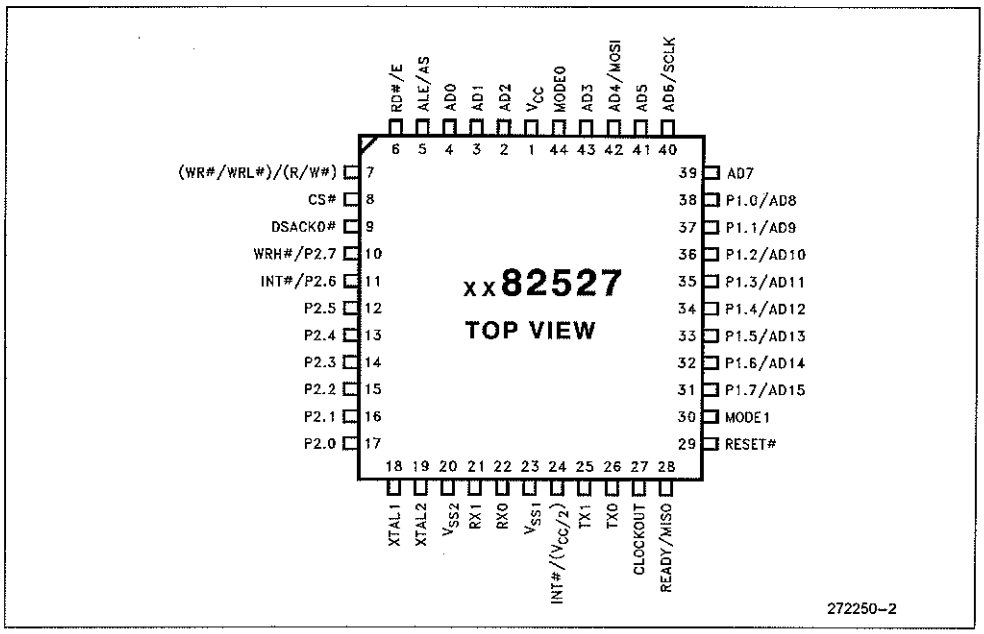

Figure 2 . 44-Pin PLCC Package

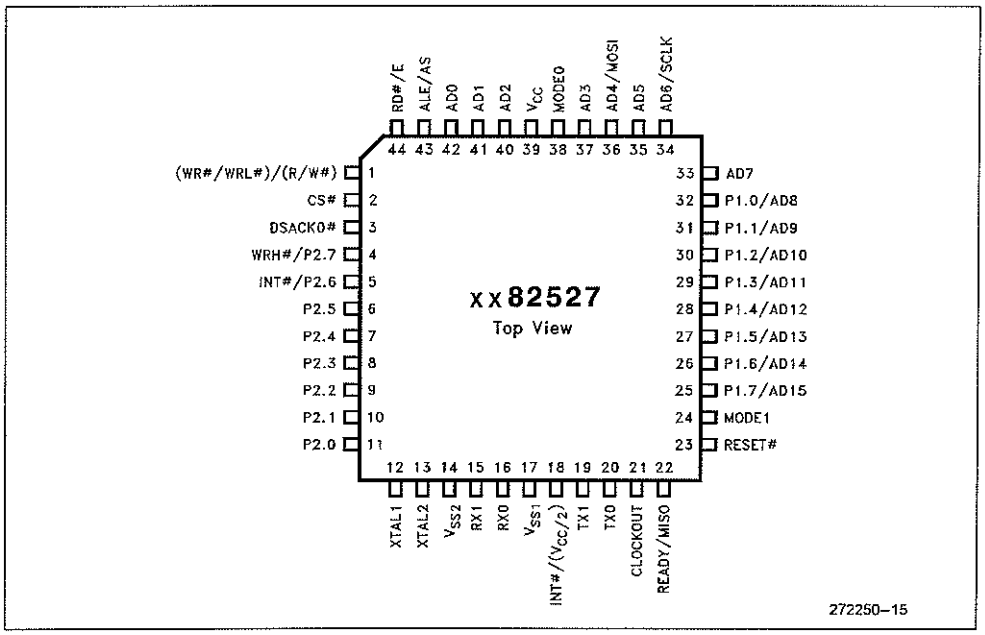

Figure 3. 44-Pin QFP Package

PIN DESCRIPTION

The 82527 pins are described in this section. Table 1 presents the legend for interpreting the pin types.

Table 1. Pin Type Legend

Symbol	Description
I	Input only pin
O	Output only pin
I/O	Pin can be either input or output

PIN DESCRIPTIONS

Pin Name	Pin Type	Pin Description
V_{SS1}	Ground	GROUND connection must be connected externally to a V_{SS} board plane. Provides digital ground.
V_{SS2}	Ground	GROUND connection must be connected externally to a V_{SS} board plane. Provides ground for analog comparator.
V_{CC}	Power	POWER connection must be connected externally to +5V DC. Provides power for entire device.
XTAL1	I	Input for an external clock. XTAL1 (along with XTAL2) are the crystal connections to an internal oscillator.
XTAL2	O	Push-pull output from the internal oscillator. XTAL2 (along with XTAL1) are the crystal connections to an internal oscillator. If an external oscillator is used XTAL2 must be floated, or not be connected. XTAL2 must not be used as a clock output to drive other CPUs.
CLKOUT	O	Programmable clock output. This output may be used to drive the oscillator of the host microcontroller.
RESET#	I	Warm Reset: (V_{CC} remains valid while RESET# is asserted), RESET# must be driven to a valid low level for 1 ms minimum. Cold Reset: (V_{CC} is driven to a valid level while RESET# is asserted), RESET# must be driven low for 1 ms minimum measured from a valid V_{CC} level. No falling edge on the reset pin is required during a cold reset event.
CS#	I	A low level on this pin enables CPU access to the 82527 device.
INT# (V_{CC}/2)	O O	The interrupt pin is an open-drain output to the host microcontroller. V_{CC}/2 is the power supply for the ISO low speed physical layer. The function of this pin is determined by the MUX bit in the CPU Interface Register (Address 02H) as follows: MUX = 1: pin 24 (PLCC) = V_{CC}/2, pin 11 = INT# MUX = 0: pin 24 (PLCC) = INT#
RX0 RX1	I I	Inputs from the CAN bus line(s) to the input comparator. A recessive level is read when RX0 > RX1. A dominant level is read when RX1 > RX0. When the CoBy bit (Bus Configuration register) is programmed as a "1", the input comparator is bypassed and RX0 is the CAN bus line input.
TX0 TX1	O O	Serial data push-pull output to the CAN bus line. During a recessive bit TX0 is high and TX1 is low. During a dominant bit TX0 is low and TX1 is high.

Pin Name	Pin Type	Pin Description
AD0/A0/ICP AD1/A1/CP AD2/A2/CSAS AD3/A3/STE AD4/A4/MOSI AD5/A5 AD6/A6/SCLK AD7/A7	I/O-I-I I/O-I-I I/O-I-I I/O-I I/O-I-I I/O-I I/O-I-I I/O-I	Address/Data bus in 8-bit multiplexed mode. Address bus in 8-bit non-multiplexed mode. Low byte of A/D bus in 16-bit multiplexed mode. In Serial Interface mode, the following pins have the following meaning: AD0: ICP Idle Clock Polarity AD1: CP Clock Phase AD2: CSAS Chip Select Active State AD3: STE Sync Transmit Enable AD6: SCLK Serial Clock Input AD4: MOSI Serial Data Input
AD8/D0/P1.0 AD9/D1/P1.1 AD10/D2/P1.2 AD11/D3/P1.3 AD12/D4/P1.4 AD13/D5/P1.5 AD14/D6/P1.6 AD15/D7/P1.7	I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O	High byte of A/D bus in 16-bit multiplexed mode. Data bus in 8-bit non-multiplexed mode. Low speed I/O port. P1 pins in 8-bit multiplexed mode and serial mode. Port pins have weak pullups until the port is configured by writing to 9FH and AFH.
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6/INT # P2.7/WRH #	I/O I/O I/O I/O I/O I/O I/O-O I/O-I	P2 in all modes. P2.6 is INT# when MUX = 1 and is open-drain. P2.7 is WRH# in 16-bit multiplexed mode.
Mode0 Mode1	I I	These pins select one of the four parallel interfaces. These pins are weakly held low during reset. Mode1 Mode0 0 0 8-bit multiplexed Ð Intel 0 0 Serial Interface mode entered when RD# = 0, WR# = 0 upon reset. 0 1 16-bit multiplexed Ð Intel 1 0 8-bit multiplexed Ð non-Intel 1 1 8-bit non-multiplexed
ALE/AS	I-I	ALE used for Intel modes. AS used for non-Intel modes, except Mode 3 this pin must be tied high.
RD# E	I I	RD# used for Intel modes. E used for non-Intel modes, except Mode 3 Asynchronous this pin must be tied high.
WR#/WRL # R/W #	I I	WR# in 8-bit Intel mode and WRL# in 16-bit Intel mode. R/W # used for non-Intel modes.
READY MISO	O O	READY is an output to synchronize accesses from the host microcontroller to the 82527. READY is an open-drain output to the host microcontroller. MISO is the serial data output for the serial interface mode.
DSACK0#	O	DSACK0# is an open-drain output to synchronize accesses from the host microcontroller to the 82527.