

2SK3378

Silicon N Channel MOS FET High Speed Switching

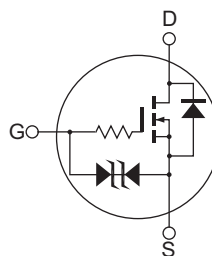
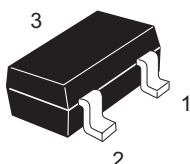
REJ03G1599-0200
(Previous: ADE-208-805)
Rev.2.00
Oct 23, 2007

Features

- Low on-resistance
 $R_{DS} = 2.7 \Omega$ typ. ($V_{GS} = 10 \text{ V}$, $I_D = 50 \text{ mA}$)
 $R_{DS} = 4.7 \Omega$ typ. ($V_{GS} = 4 \text{ V}$, $I_D = 20 \text{ mA}$)
- 4 V gate drive device.
- Small package (CMPAK)

Outline

RENESAS Package code: PTSP0003ZA-A
(Package name: CMPAK®)



1. Source
2. Gate
3. Drain

Note: Marking is EN

*CMPAK is a trademark of Renesas Technology Corp.

Absolute Maximum Rating

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	100	mA
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	400	mA
Body-drain diode reverse drain current	I_{DR}	100	mA
Channel dissipation	P_{ch} ^{Note 2}	300	mW
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Note: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
2. Value on the alumina ceramic board (12.5 x 20 x 0.7 mm)

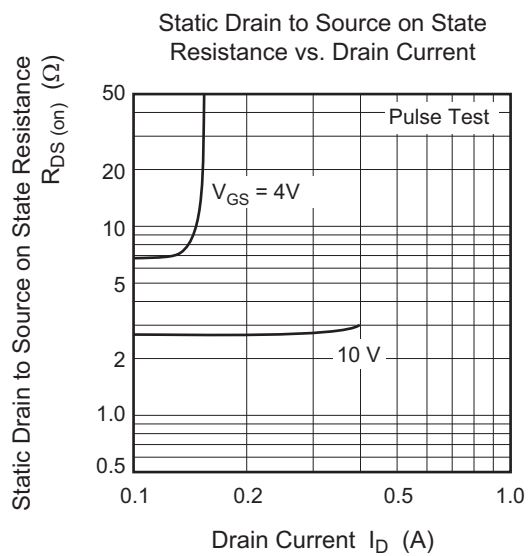
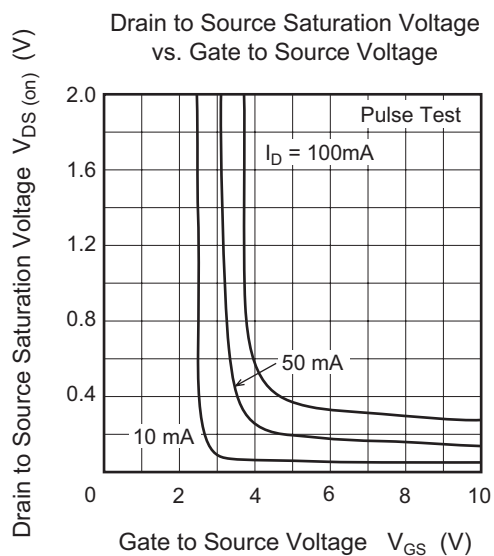
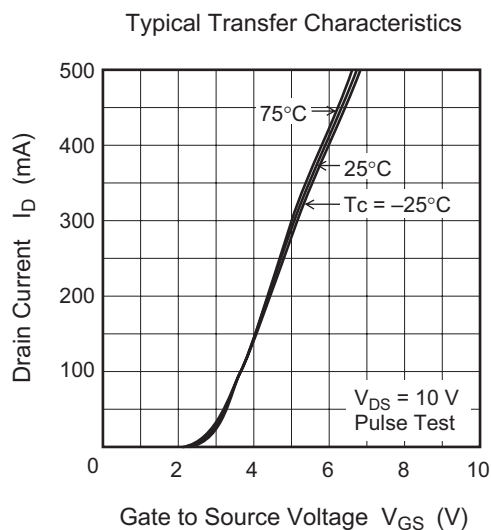
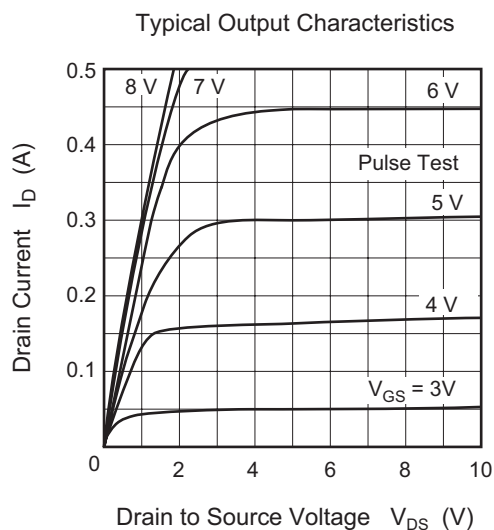
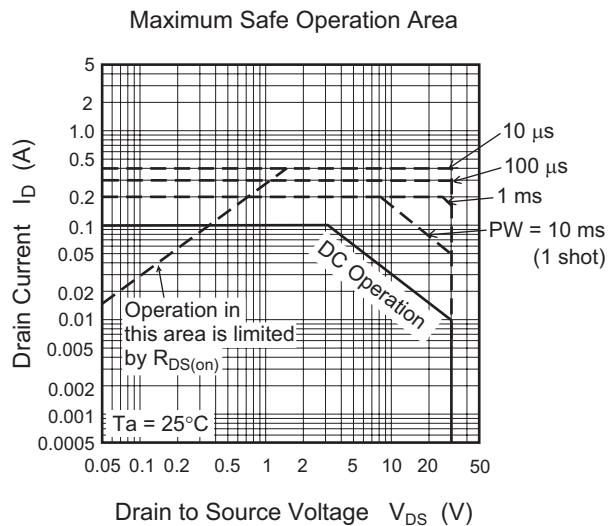
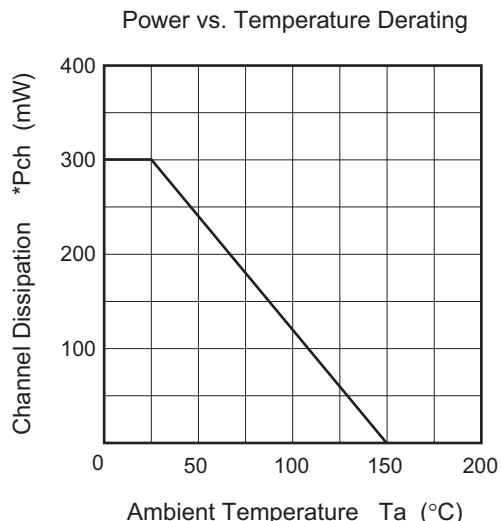
Electrical Characteristics

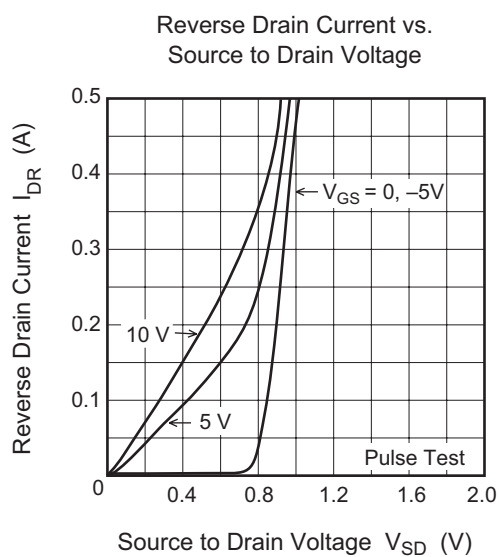
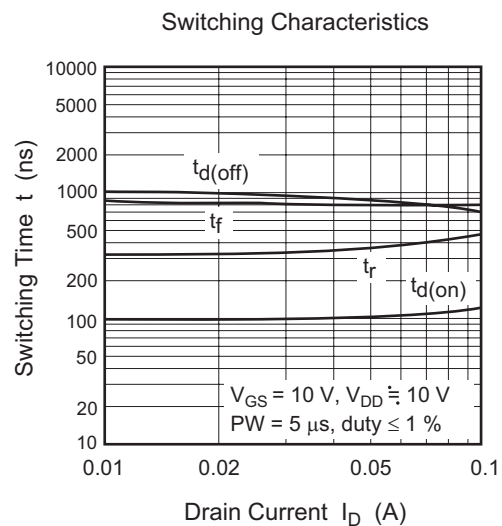
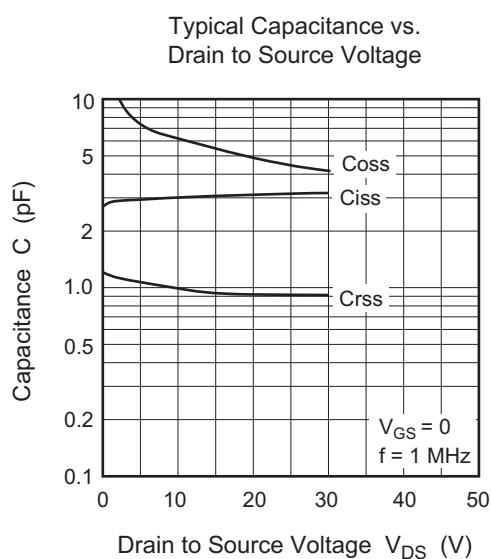
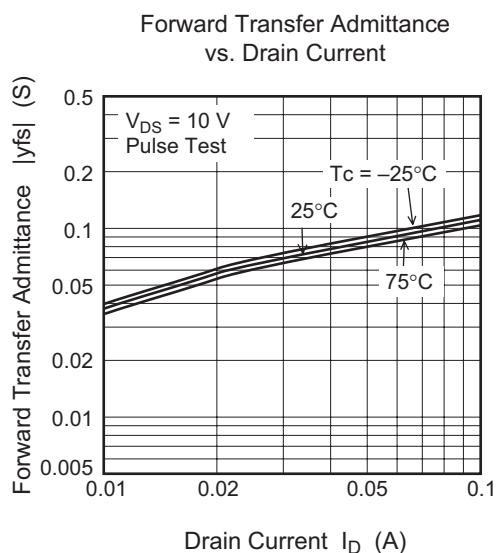
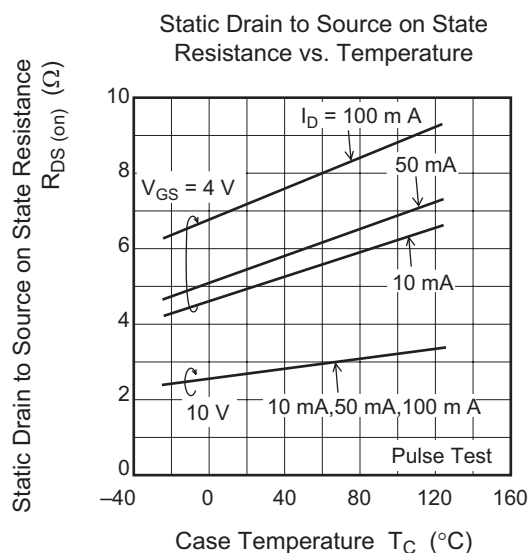
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 100\ \mu A$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\ \mu A$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 5	μA	$V_{GS} = \pm 16\ V$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30\ V$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.3	—	2.3	V	$I_D = 10\ \mu A$, $V_{DS} = 5\ V$
Static drain to source on state resistance	$R_{DS(on)}$	—	2.7	3.5	Ω	$I_D = 50\ mA$, $V_{GS} = 10\ V$ ^{Note 3}
	$R_{DS(on)}$	—	4.7	7.0	Ω	$I_D = 20\ mA$, $V_{GS} = 4\ V$ ^{Note 3}
Forward transfer admittance	$ y_{fs} $	55	85	—	mS	$I_D = 50\ mA$, $V_{DS} = 10\ V$ ^{Note 3}
Input capacitance	C_{iss}	—	3	—	pF	$V_{DS} = 10\ V$ $V_{GS} = 0$ $f = 1\ MHz$
Output capacitance	C_{oss}	—	8	—	pF	
Reverse transfer capacitance	C_{rss}	—	1	—	pF	
Turn-on delay time	$t_{d(on)}$	—	100	—	ns	$I_D = 50\ mA$, $V_{GS} = 10\ V$ $R_L = 200\ \Omega$
Rise time	t_r	—	330	—	ns	
Turn-off delay time	$t_{d(off)}$	—	1150	—	ns	
Fall time	t_f	—	940	—	ns	

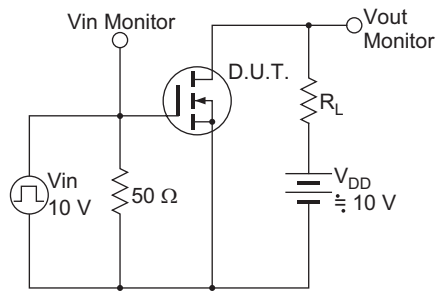
Notes: 3. Pulse test

Main Characteristics

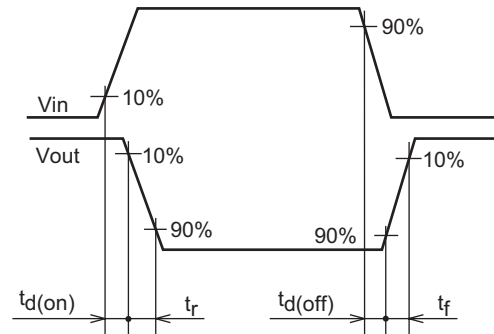




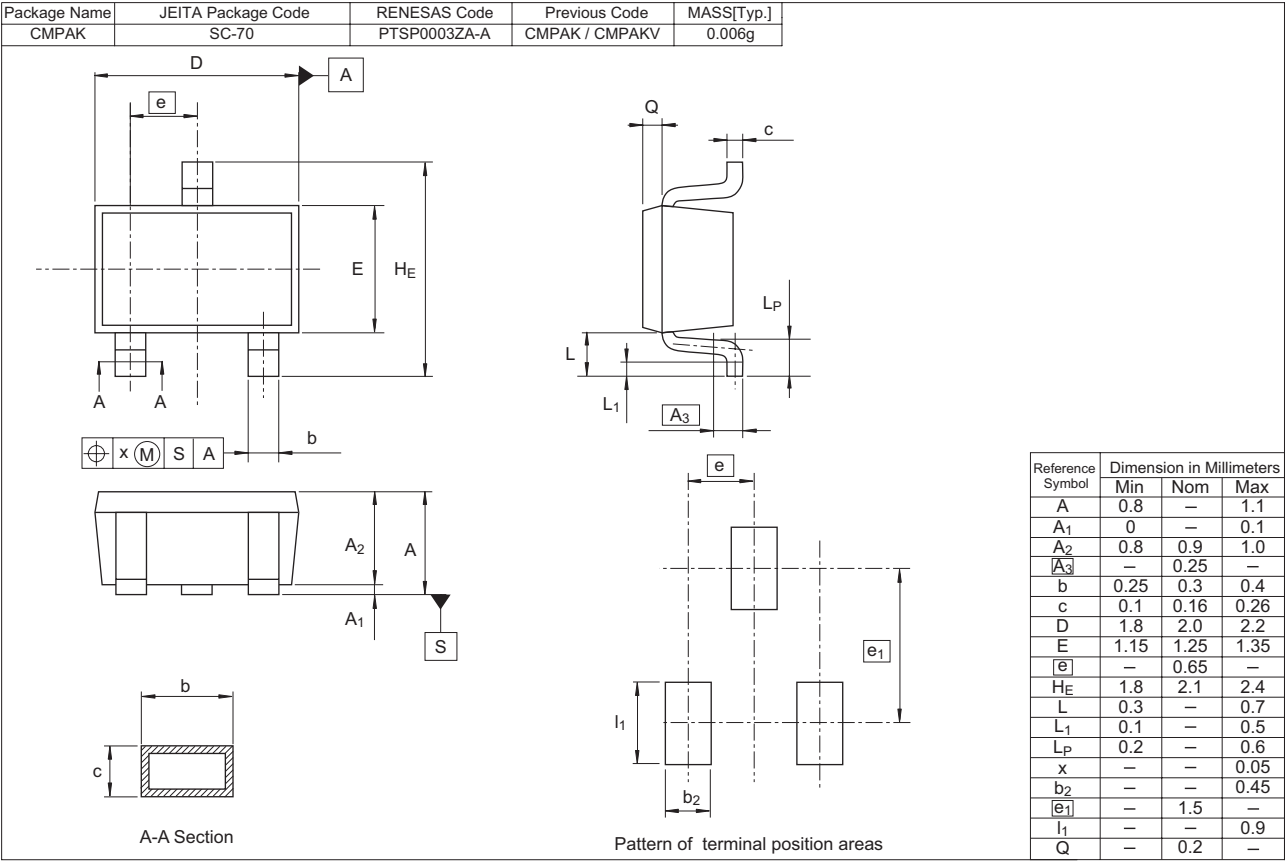
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
2SK3378ENTL-E	3000 pcs	Taping
2SK3378ENTR-E	3000 pcs	Taping

Notes:

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