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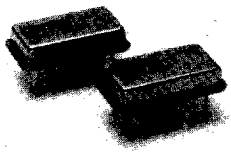


SHC76

SAMPLE/HOLD AMPLIFIER

FEATURES

- FAST (6µs max) ACQUISITION TIME (14-bit)
- APERTURE JITTER: 400ps
- POWER DISSIPATION: 300mW
- COMPATIBLE WITH HIGH RESOLUTION A/D CONVERTERS ADC76, PCM75, AND ADC71

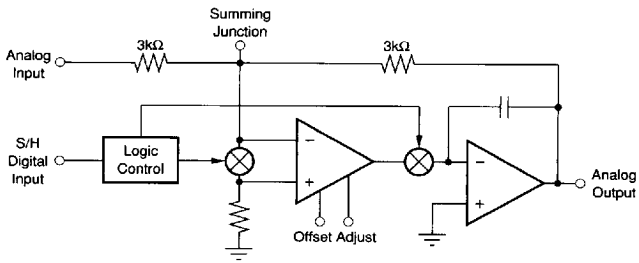
DESCRIPTION

The SHC76 is a fast, high-accuracy hybrid sample/hold circuit suitable for use in high-resolution data acquisition systems.

The SHC76 is complete with internal hold capacitor and incorporates an internal compensation network which minimizes sample-to-hold charge offset. The SHC76 is configured as a unity-gain inverter.

High-resolution converters such as the ADC76 and ADC71 are compatible with SHC76 in forming complete, 14-bit accurate analog-to-digital conversion systems.

The SHC76 comes in a 14-pin single-wide hermetic metal DIP. Power supply requirements are specified from ±14.5V to ±15.5V with guaranteed operation from ±11.4V to ±18V. Input voltage range is ±10V. The SHC76 is available in two temperature ranges: KM, for 0°C to +70°C; and BM, for –25°C to +85°C operation.



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SPECIFICATIONS

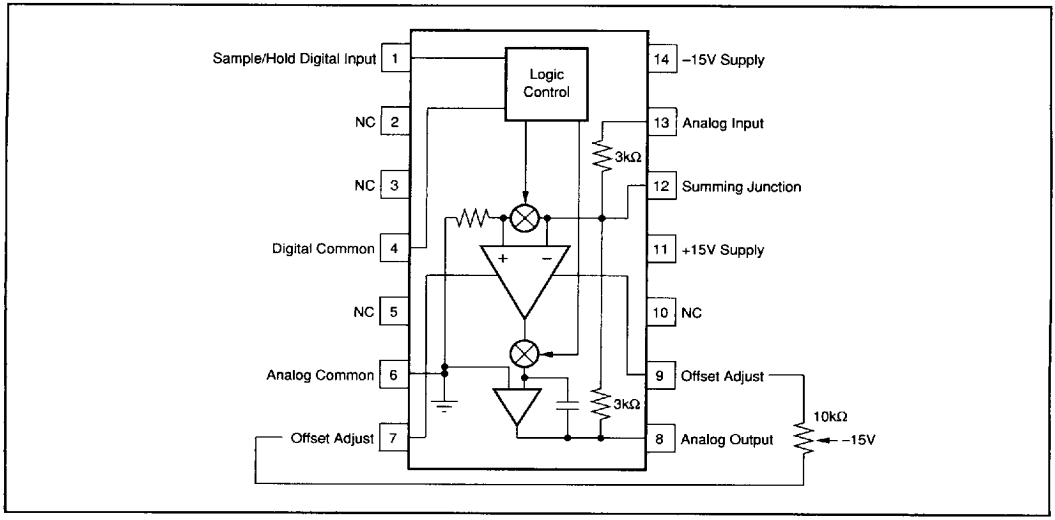
ELECTRICAL

Typical at +25°C, and nominal power supply voltage of ±15V, unless otherwise noted.

PARAMETER	SHC76KM, BM MIN	SHC76KM, BM TYP	SHC76KM, BM MAX	UNITS
ANALOG INPUTS				
Voltage Range	±10			V
Overvoltage, no damage			±15	V
Impedance		3000		Ω
DIGITAL INPUT				
(TTL-Compatible)				
Track Mode, Logic "1"	2		5.5	V
Hold Mode, Logic "0"	0		0.8	V
I_{IH}, V_{IH} = 2.4V			400	µA
I_{IL}, V_{IL} = 0.4V			1000	µA
ANALOG OUTPUT				
Voltage		±10		V
Current		5		mA
Short-Circuit Current		20		mA
Impedance		1		Ω
DC ACCURACY/STABILITY				
Gain		−1.00		V/V
Gain Error		±0.01	±0.02	%
Gain Nonlinearity				
(±10V Output Track)		±0.001		%
Gain Temperature Coefficient		1	5	ppm/°C
Offset Voltage[1]			±3	mV
Output Offset at T_{MIN}, T_{MAX} (Track)		±6		mV
TRACK MODE DYNAMICS				
Freqency Response				
Small Signal (−3dB)		1.5		MHz
Full Power Bandwidth		0.5		MHz
Slew Rate		30		V/µs
Noise in Track Mode				
(DC to 1.0MHz)		200		µVrms
TRACK-TO-HOLD SWITCHING				
Aperture Time		30		ns
Aperture Uncertainty (Jitter)		0.4		ns
Offset Step (Pedestal)		±2	±4	mV
Pedestal at Temperature				
KM Grade		±4		mV
BM Grade		±6		mV
Switching Transient				
Amplitude		200		mV
Settling to 1mV		0.5	2	µs
Settling to 0.3mV		1	3	µs
HOLD MODE DYNAMICS				
Droop Rate		0.1	1	µV/µs
Droop Rate at T_{MAX}			100	µV/µs
Feedthrough Rejection				
(10Vp-p, 20kHz)	74	86		dB
HOLD-TO-TRACK DYNAMICS				
Acquisition Time				
To ±0.01% of 20V		1.5	3	µs
To ±0.003% of 20V		4	6	µs
POWER REQUIREMENTS				
Nominal Voltages for Rated				
Performance	±14.5	±15	±15.5	V
Operating Range[2]	±11.4		±18	V
Power Supply Rejection		100		µV/V
Supply Current: $+V_S$		15	20	mA
$-V_S$		−4	−10	mA
Power Dissipation		300	500	mW
TEMPERATURE RANGE				
Operating: KM Grade	0		+70	°C
BM Grade	−25		+85	°C
Storage	−55		+125	°C

NOTES: (1) Adjustable to zero with external circuit. (2) Operating to derated performance with $V_{IN} < V_S - 5V$.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

Voltage Between $+V_{CC}$ and $-V_{CC}$ Terminals	40V
Input Voltage	Actual Supply Voltage
Differential Input Voltage	±24V
Digital Input Voltage	−0.5V to +5.5V
Output Current Continuous(2)	±20mA
Internal Power Dissipation	500mW
Storage Temperature Range	$-65°C < T_A < +150°C$
Output Short-Circuit Duration(3)	Momentary to Common
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the servicability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. (2) Internal power dissipation may limit output current to less than +20mA. (3) **WARNING: This device cannot withstand even a momentary short circuit to either supply.**

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
SHC76KM	14-Pin Single-Wide, Hermetic Metal DIP	107
SHC76BM	14-Pin Single-Wide, Hermetic Metal DIP	107

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
SHC76KM	14-Pin Single-Wide, Hermetic Metal DIP	0°C to +70°C
SHC76BM	14-Pin Single-Wide, Hermetic Metal DIP	−25°C to +85°C

PIN ASSIGNMENTS

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Digital Input	8	Analog Output
2	No Connection	9	Offset Adjust
3	No Connection	10	No Connection
4	Digital Ground	11	+15V Supply
5	No Connection	12	Summing Junction
6	Analog Ground	13	Analog Input
7	Offset Adjust	14	−15V Supply

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCUSSION OF SPECIFICATIONS

THROUGHPUT NONLINEARITY

This is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by Offset and Gain adjustments.

GAIN ERROR

The difference between the input and output voltage magnitude (in the Sample mode) due to the amplifier gain errors.

DROOP RATE

The voltage decay at the output when in the Hold mode due to storage capacitor and FET switch leakage current and the input bias current of the output amplifier.

FEEDTHROUGH

The amount of output voltage change caused by an input voltage change when the sample/hold is in the Hold mode.

APERTURE DELAY TIME

The time required to switch from Sample-to-Hold. The time is measured from the 50% point of the Hold mode control transition to the time at which the output stops tracking the input.

APERTURE UNCERTAINTY TIME

The nonrepeatibility of aperture delay time.

ACQUISITION TIME

The time required for the sample/hold output to settle within a given error band of its final value when the sample/hold is switched from Hold-to-Sample.

CHARGE OFFSET (PEDESTAL)

The output voltage change that results from charge coupled into the Hold capacitor through the gate capacitance of the switching field effect transistor. This charge appears as an offset at the output.

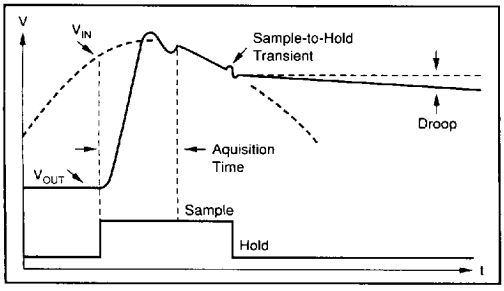


FIGURE 1. Definition of Acquisition Time, Droop and Sample-to-Hold Transient.

SAMPLE-TO-HOLD SWITCHING TRANSIENT

The switching transient which appears on the output when the sample/hold is switched from Sample-to-Hold. Both the magnitude and the settling time of the transient are specified.

SAMPLED DATA ACQUISITION SYSTEM CALCULATIONS

The rated accuracy of an A/D converter in combination with the aperture uncertainty of a sample/hold determine the maximum theoretical input slew rate (frequency) of a given sampled data system.

Sine Wave $f_{MAX} = (2^{-N}\ FSR) \div (2\pi\ A\ t)$
A = max Input Signal Amplitude (peak-to-peak)
FSR = Full-Scale Range of A/D Converter
t = Aperture Uncertainty of S/H (jitter)
N = Number of Bits Accuracy

Given below are the maximum input frequencies of two A/D converters in conjunction with the SHC76:

SHC76 13-bit Sine Wave f_{MAX} =
$(0.000122 \cdot 20V) \div (2 \cdot \pi \cdot 20V \cdot 0.4ns) = 48.6kHz$

SHC76 14-bit Sine Wave f_{MAX} =
$(0.000061 \cdot 20V) \div (2 \cdot \pi \cdot 20V \cdot 0.4ns) = 24.3kHz$

The maximum throughput rate is determined by adding all critical conversion process times together. Throughput rate cannot exceed the maximum input frequency determined by the accuracy and jitter specs without degrading system performance. Two samples per period of a sine wave are required to satisfy the Nyquist sampling theorem. A low-pass filter is required to cut off frequencies higher than the maximum throughput frequency to prevent aliasing errors from occurring.

Throughput f_{MAX} (2 samples) =
1 ÷ [2 (S/H acquisition time + S/H settling time + A/D conversion time)]

Table I is a listing of various A/D throughput rates using the SHC76 S/H amplifier (assuming two samples per period).

CONVERTER	ACCURACY (Bits)	CONVERSION SPEED (µs)	RESOLUTION (Bits)	THROUGHPUT F_{MAX} (kHz)
ADC76KG	14	17	16	19.2
	14	16	15	20.0
	14	15	14	20.8
ADC76JG	13	17	16	23.8
	13	16	15	25.0
	13	15	14	26.3
ADC71KG	14	57	16	7.58
	14	54	15	7.94
	14	50	14	8.47
ADC71JG	13	57	16	8.20
	13	54	15	8.62
	13	50	14	9.26

TABLE I. A/D Converter Throughput Rates.

APPLICATIONS

Figures 2 and 3 show the SHC76 in combination with an ADC76 and ADC71 to provide 14-bit accurate A/D conversion systems.

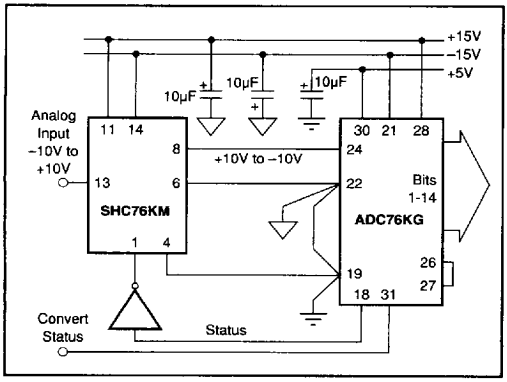


FIGURE 2. A 20kHz A/D Conversion System (14-bit accurate).

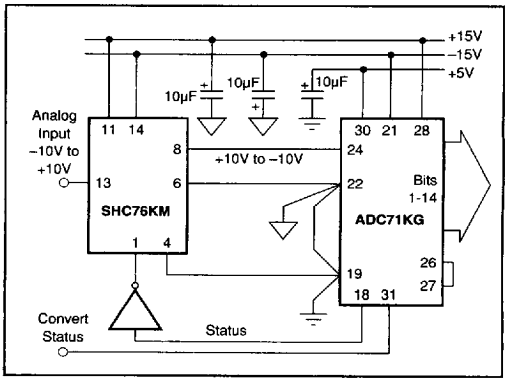


FIGURE 3. A 8.47kHz A/D Conversion System (14-bit accurate).