

FEATURES

- Low Supply Current 1mA Max
- Slew Rate 0.25V/ μ s Min
- Single Supply Operation +5V to +30V
- Low Input Offset Voltage 500 μ V Typ
- Low Input Offset Voltage Drift 10 μ V/ $^{\circ}$ C Max
- High Common-Mode Input Range ... V- to V+ (-1.5V)
- High CMRR 100dB Typ
- High Open-Loop Gain 400V/mV Typ
- Single-Chip Monolithic Construction
- Pin Compatible With LM124, LM324, LM148, and OP-11
- Available in Die Form

ORDERING INFORMATION [†]

$T_A = +25^{\circ}\text{C}$ V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP 14-PIN	PLASTIC	SO	
2.5	OP421BY*	—	—	MIL
2.5	OP421FY	—	—	IND
4.0	OP421CY*	—	—	MIL
4.0	OP421GY	OP421GP	OP421GS	XIND
6.0	OP421HY	OP421HP	OP421HS	XIND

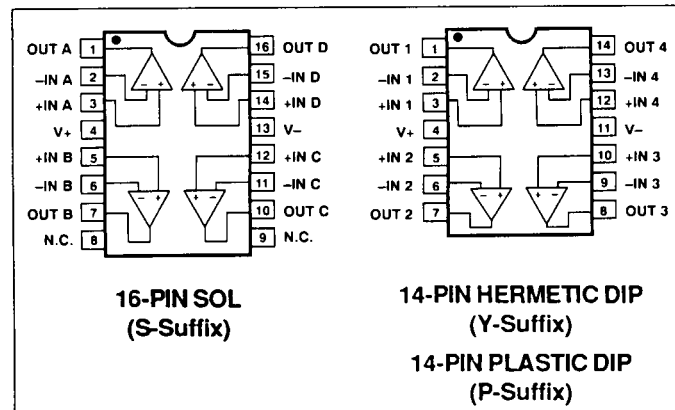
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

[†] Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

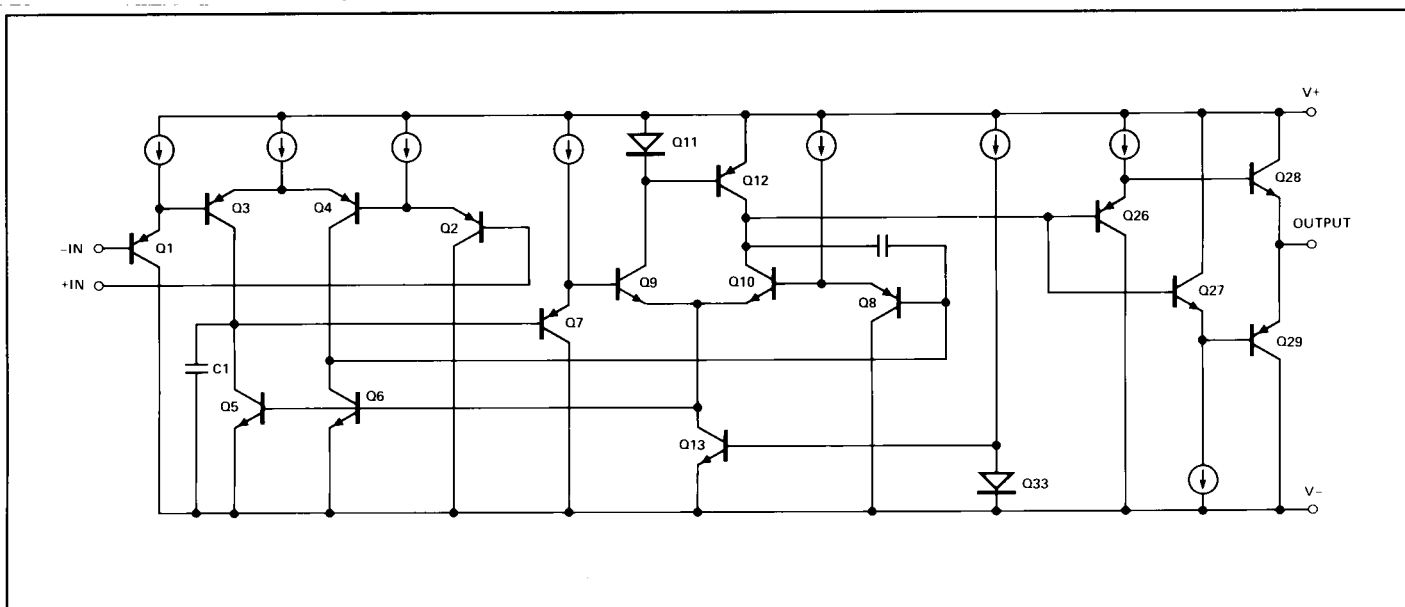
GENERAL DESCRIPTION

The OP-421 quad low-power operational amplifier is a single-chip quad patterned after the OP-21 single operational amplifier. The PNP input stage allows the input common-mode voltage to include V-. Featuring a low power-supply current (150 μ A/section typical at 5V), the OP-421 offers a unique solution for designs requiring a combination of high function density, wide bandwidth, and low-power operation. Applications for the OP-421 include low-power active filters, battery-operated remote line filters, and signal preconditioning amplifiers. In addition, the ever-present problem of crossover distortion in low-power devices is eliminated by a unique double-buffered output section.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/4 Shown)



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous
(One Amplifier Only)	
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Operating Temperature Range	
OP-421BY, OP-421CY	–55°C to +125°C
OP-421FY	–25°C to +85°C
OP-421G, OP421H	–40°C to +85°C

Junction Temperature (T_j) –65°C to +150°C

PACKAGE TYPE	θ_{JA} (Note 2)	θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	99	12	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-421B OP-421F			OP-421C OP-421G			OP-421H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.5	2.5	—	1	4	—	2	6	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.6	5.0	—	2.0	10	—	5.0	20	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	20	50	—	50	80	—	100	150	nA
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$ (Note 1)	—	20	40	—	20	40	—	20	40	nV/ $\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 1)	—	15	30	—	15	30	—	15	30	
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$ (Note 1)	—	0.3	0.6	—	0.3	0.6	—	0.3	0.6	pA/ $\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 1)	—	0.2	0.4	—	0.2	0.4	—	0.2	0.4	
Input Voltage Range	IVR	$V_+ = +5V$, $V_- = 0V$	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	–15/13.5	—	—	–15/13.5	—	—	–15/13.5	—	—	
Common-Mode Rejection Ratio	CMRR	$V_+ = +5V$, $V_- = 0V$, $0V \leq V_{CM} \leq +3.5V$	83	100	—	80	96	—	76	90	—	dB
		$V_S = \pm 15V$, $-15V \leq V_{CM} \leq +13.5V$	83	100	—	80	96	—	76	90	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; & $V_- = 0V$, $V_+ = 5V$ to $30V$	—	10	30	—	20	50	—	30	80	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$	200	400	—	100	200	—	100	200	—	V/mV
Output Voltage Swing	V_O	$V_+ = 5V$, $V_- = 0V$ $R_L = 5k\Omega$	0.7/4.0	—	—	0.8/3.9	—	—	0.9/3.8	—	—	V
		$V_S = \pm 15V$, $R_L = 10k\Omega$	± 14	—	—	± 13.9	—	—	± 13.8	—	—	
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$, $R_L = 10k\Omega$	1.0	1.9	—	1.0	1.9	—	1.0	1.9	—	MHz
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	0.6	1.0	—	0.7	1.5	—	0.9	2.0	mA
		$V_S = \pm 15V$, No Load	—	1.2	1.8	—	1.4	2.3	—	1.8	3.0	
Slew Rate	SR	(Note 1)	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/ μs
Channel Separation	CS	(Note 1)	100	120	—	100	120	—	100	120	—	dB

NOTES:

1. Sample tested.
2. Guaranteed by design.

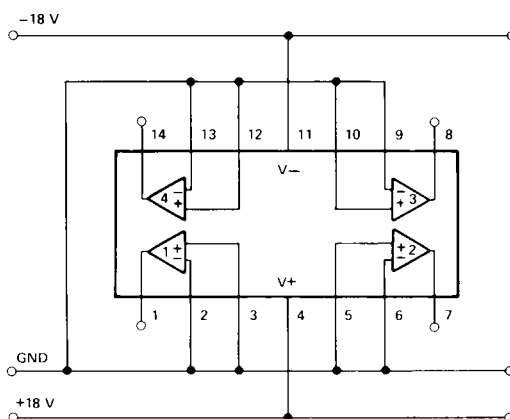
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-421B and OP-421C, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-421F, and $-40^\circ C \leq T_A \leq +85^\circ C$ for OP-421G and OP-421H, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-421B OP-421F			OP-421C OP-421G			OP-421H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}		—	5	10	—	8	15	—	10	15	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	1	3.5	—	1.8	5.5	—	3	7.5	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	1.6	8	—	3.0	15	—	6.0	30	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	25	70	—	60	125	—	140	230	nA
Input Voltage Range	IVR	$V_+ = +5V, V_- = 0V$ $V_S = \pm 15V$	0/3.2 -15/13.2	—	—	0/3.2 -15/13.2	—	—	0/3.2 -15/13.2	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_+ = +5V, V_- = 0V,$ $0V \leq V_{CM} \leq +3.2V$	78	96	—	74	94	—	73	86	—	dB
		$V_S = \pm 15V,$ $-15V \leq V_{CM} \leq +13.2V$	78	96	—	74	94	—	73	86	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; & $V_- = 0V, V_+ = 5V$ to $30V$	—	15	50	—	25	80	—	40	100	$\mu V/V$
			—	15	50	—	25	80	—	40	100	
Large-Signal Voltage Gain	A_{VO}	$V_O = 10V$ $R_L = 20k\Omega$	100	200	—	50	100	—	50	100	—	V/mV
Output Voltage Swing	V_O	$V_+ = 5V, V_- = 0V$ $R_L = 10k\Omega$	0.8/3.9	—	—	0.9/3.8	—	—	1.0/3.7	—	—	V
		$V_S = \pm 15V,$ $R_L = 20k\Omega$	± 13.8	—	—	± 13.7	—	—	± 13.7	—	—	
Supply Current (Four Amplifiers)	I_{SV}	$V_S = \pm 2.5V$, No Load	—	1.2	1.5	—	1.5	2.0	—	2.0	3.0	mA
		$V_S = \pm 15V$, No Load	0.68	2.0	2.5	0.68	2.5	3.2	0.68	3.2	4.0	

NOTE:

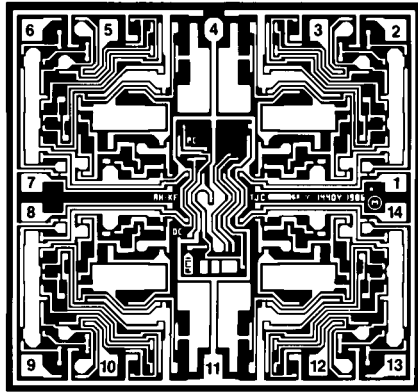
1. Sample tested.

BURN-IN CIRCUIT



OP-421

DICE CHARACTERISTICS



DIE SIZE 0.093 × 0.087 inch, 8091 sq. mils
(2.36 × 2.21 mm, 5.22 sq. mm)

1. OUTPUT 1
2. INVERTING INPUT 1
3. NONINVERTING INPUT 1
4. V⁺
5. NONINVERTING INPUT 2
6. INVERTING INPUT 2
7. OUTPUT 2
8. OUTPUT 3
9. INVERTING INPUT 3
10. NONINVERTING INPUT 3
11. V⁻
12. NONINVERTING INPUT 4
13. INVERTING INPUT 4
14. OUTPUT 4

WAFER TEST LIMITS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-421N LIMIT	OP-421G LIMIT	OP-421GR LIMIT	UNITS
Input Offset Voltage	V _{OS}	V _S = ±2.5V to ±15V	2.5	4	6	mV MAX
Input Offset Current	I _{OS}	V _S = ±2.5V to ±15V	5	10	20	nA MAX
Input Bias Current	I _B	V _S = ±2.5V to ±15V	50	80	150	nA MAX
Input Voltage Range	IVR		-15/13.5	-15/13.5	-15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	V ⁺ = +5V, V ⁻ = 0V 0V ≤ V _{CM} ≤ +3.5V V _S = ±15V, -15V ≤ V _{CM} ≤ +13.5V	83	80	76	dB MIN
Power Supply Rejection Ratio	PSRR	V _S = ±2.5V to ±15V; and V ⁻ = 0V, V ⁺ = +5V to 30V	30	50	80	μV/V MAX
Large-Signal Voltage Gain	A _{VO}	V _O = ±10V R _L = 20kΩ	200	200	100	V/mV MIN
Output Voltage Swing	V _O	V ⁺ = +5V, V ⁻ = 0V, R _L = 5kΩ V _S = ±15V, R _L = 10kΩ	0.7/4.0 ±14	0.8/3.9 ±13.9	0.9/3.8 ±13.8	V MIN
Supply Current (Four Amplifiers)	I _{SY}	V _S = ±2.5V, No Load V _S = ±15V, No Load	1.0 1.8	1.5 2.3	2.0 3.0	mA MAX

NOTE:

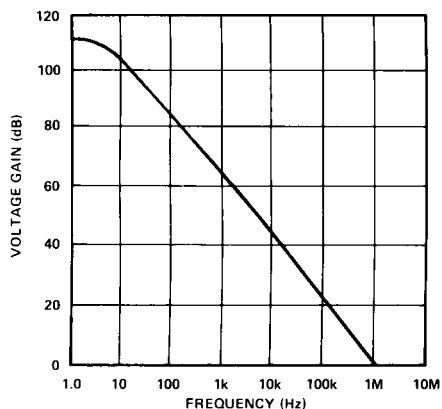
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

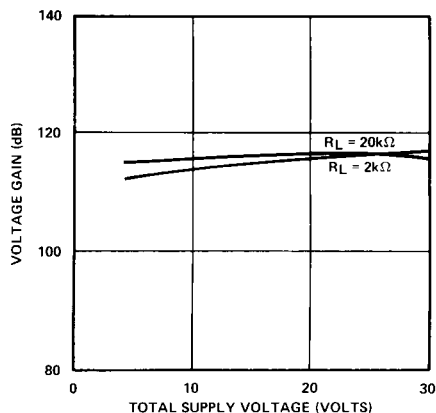
PARAMETER	SYMBOL	CONDITIONS	OP-421N TYPICAL	OP-421G TYPICAL	OP-421GR TYPICAL	UNITS
Input Noise Voltage Density	e _n	f _O = 10Hz f _O = 100Hz	20 15	20 15	20 15	nV/√Hz
Closed-Loop Bandwidth	BW	A _{VCL} = +1.0 R _L = 10kΩ	1.9	1.9	1.9	MHz
Slew Rate	SR		0.5	0.5	0.5	V/μs
Channel Separation	CS		120	120	120	dB

TYPICAL PERFORMANCE CHARACTERISTICS

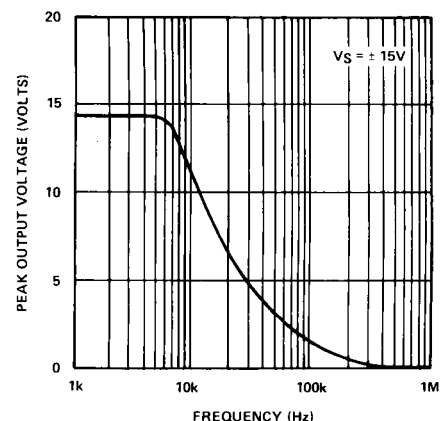
**OPEN-LOOP
FREQUENCY RESPONSE**



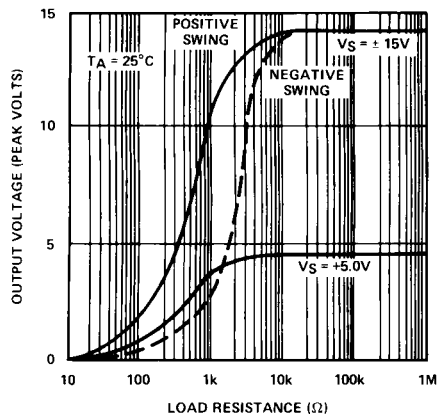
**OPEN-LOOP GAIN
vs POWER SUPPLY VOLTAGE**



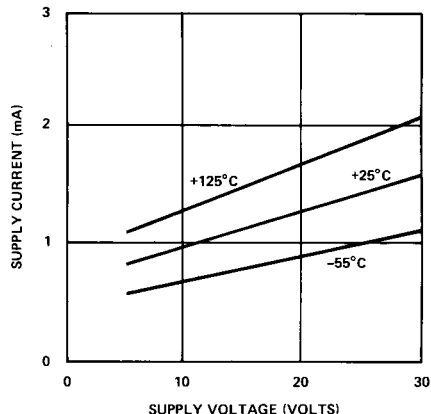
**OUTPUT SWING
vs FREQUENCY**



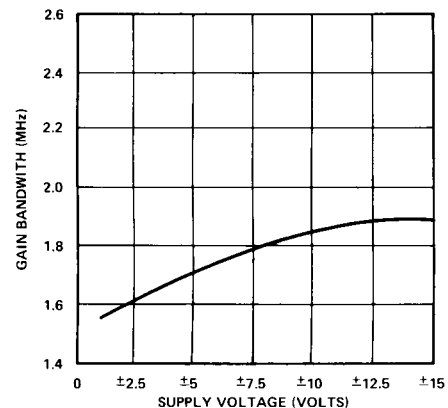
**OUTPUT SWING vs
OUTPUT LOAD**



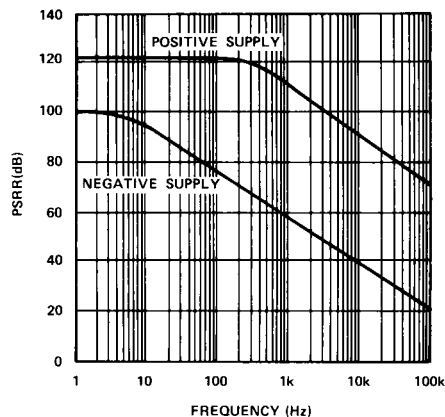
**SUPPLY CURRENT vs
SUPPLY VOLTAGE**



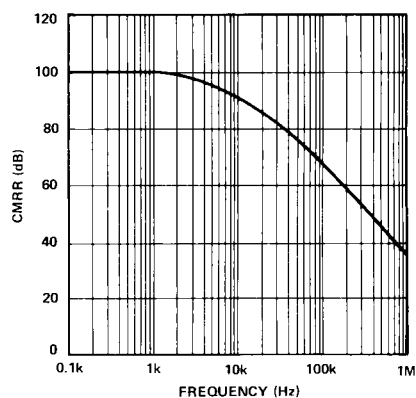
**GAIN BANDWIDTH vs
SUPPLY VOLTAGE**



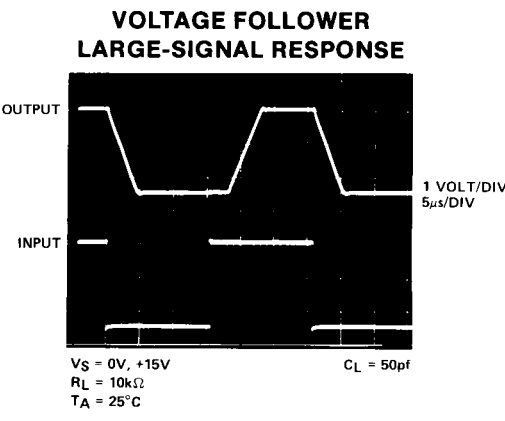
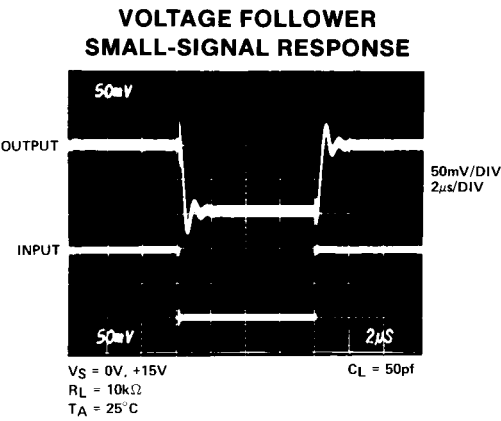
**POWER SUPPLY REJECTION
RATIO vs FREQUENCY**



**COMMON-MODE REJECTION
RATIO vs FREQUENCY**



TYPICAL PERFORMANCE CHARACTERISTICS



NOISE CHARACTERISTICS

