

# IS45C16100 IS45LV16100



## 1M x 16 (16-MBIT) DYNAMIC RAM WITH EDO PAGE MODE

PRELIMINARY INFORMATION  
OCTOBER 2002

### FEATURES

- TTL compatible inputs and outputs; tristate I/O
- Refresh Interval:
  - Auto refresh Mode:* 1,024 cycles /16 ms
  - RAS-Only, CAS-before-RAS (CBR), and Hidden*
  - Self refresh Mode* - 1,024 cycles / 128ms
- JEDEC standard pinout
- Single power supply:
  - 5V  $\pm$  10% (IS45C16100)
  - 3.3V  $\pm$  10% (IS45LV16100)
- Byte Write and Byte Read operation via two  $\overline{\text{CAS}}$
- Automotive Temperature Range:
  - Option A: 0°C to +70°C
  - Option A1: -40°C to +85°C

### DESCRIPTION

The *ISSI* IS45C16100 and IS45LV16100 are 1,048,576 x 16-bit high-performance CMOS Dynamic Random Access Memories. These devices offer an accelerated cycle access called EDO Page Mode. EDO Page Mode allows 1,024 random accesses within a single row with access cycle time as short as 20 ns per 16-bit word. The Byte Write control, of upper and lower byte, makes the IS45C16100 ideal for use in 16-bit and 32-bit wide data bus systems.

These features make the IS45C16100 and IS45LV16100 ideally suited for high-bandwidth graphics, digital signal processing, high-performance computing systems, and peripheral applications.

The IS45C16100 and IS45LV16100 are packaged in a 42-pin 400-mil SOJ and 400-mil 50- (44-) pin TSOP (Type II).

### PRODUCT SERIES OVERVIEW

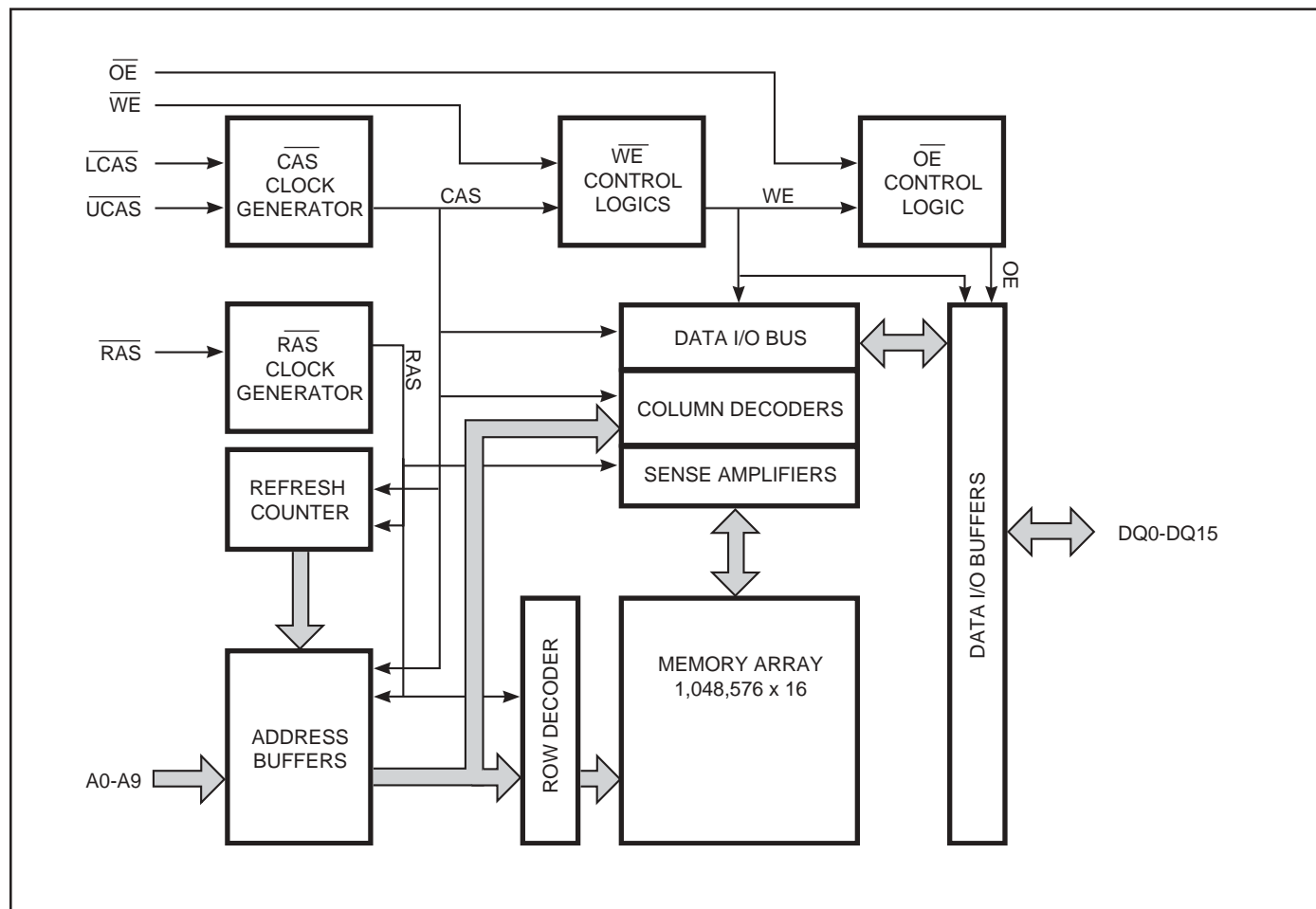
Part No.	Refresh	Voltage
IS45C16100	1K	5V $\pm$ 10%
IS45LV16100	1K	3.3V $\pm$ 10%

### KEY TIMING PARAMETERS

Parameter	-50	-60	Unit
Max. $\overline{\text{RAS}}$ Access Time ( $t_{\text{RAC}}$ )	50	60	ns
Max. $\overline{\text{CAS}}$ Access Time ( $t_{\text{CAC}}$ )	13	15	ns
Max. Column Address Access Time ( $t_{\text{AA}}$ )	25	30	ns
Min. EDO Page Mode Cycle Time ( $t_{\text{PC}}$ )	20	25	ns
Min. Read/Write Cycle Time ( $t_{\text{RC}}$ )	84	104	ns

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## FUNCTIONAL BLOCK DIAGRAM



## TRUTH TABLE

Function		$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Address tr/tc	I/O
Standby		H	H	H	X	X	X	High-Z
Read: Word		L	L	L	H	L	ROW/COL	DOUT
Read: Lower Byte		L	L	H	H	L	ROW/COL	Lower Byte, DOUT Upper Byte, High-Z
Read: Upper Byte		L	H	L	H	L	ROW/COL	Lower Byte, High-Z Upper Byte, DOUT
Write: Word (Early Write)		L	L	L	L	X	ROW/COL	DIN
Write: Lower Byte (Early Write)		L	L	H	L	X	ROW/COL	Lower Byte, DIN Upper Byte, High-Z
Write: Upper Byte (Early Write)		L	H	L	L	X	ROW/COL	Lower Byte, High-Z Upper Byte, DIN
Read-Write <sup>(1,2)</sup>		L	L	L	H→L	L→H	ROW/COL	DOUT, DIN
EDO Page-Mode Read <sup>(2)</sup>	1st Cycle:	L	H→L	H→L	H	L	ROW/COL	DOUT
	2nd Cycle:	L	H→L	H→L	H	L	NA/COL	DOUT
	Any Cycle:	L	L→H	L→H	H	L	NA/NA	DOUT
EDO Page-Mode Write <sup>(1)</sup>	1st Cycle:	L	H→L	H→L	L	X	ROW/COL	DIN
	2nd Cycle:	L	H→L	H→L	L	X	NA/COL	DIN
EDO Page-Mode <sup>(1,2)</sup> Read-Write	1st Cycle:	L	H→L	H→L	H→L	L→H	ROW/COL	DOUT, DIN
	2nd Cycle:	L	H→L	H→L	H→L	L→H	NA/COL	DOUT, DIN
Hidden Refresh	Read <sup>(2)</sup>	L→H→L	L	L	H	L	ROW/COL	DOUT
	Write <sup>(1,3)</sup>	L→H→L	L	L	L	X	ROW/COL	DOUT
RAS-Only Refresh		L	H	H	X	X	ROW/NA	High-Z
CBR Refresh <sup>(4)</sup>		H→L	L	L	X	X	X	High-Z

### Notes:

1. These WRITE cycles may also be BYTE WRITE cycles (either  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  active).
2. These READ cycles may also be BYTE READ cycles (either  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  active).
3. EARLY WRITE only.
4. At least one of the two  $\overline{\text{CAS}}$  signals must be active ( $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$ ).

## Functional Description

The IS45C16100 and IS45LV16100 is a CMOS DRAM optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 16 address bits. These are entered ten bits (A0-A9) at a time. The row address is latched by the Row Address Strobe ( $\overline{\text{RAS}}$ ). The column address is latched by the Column Address Strobe ( $\overline{\text{CAS}}$ ).  $\overline{\text{RAS}}$  is used to latch the first nine bits and  $\overline{\text{CAS}}$  is used to latch the latter nine bits.

The IS45C16100 and IS45LV16100 has two  $\overline{\text{CAS}}$  controls,  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$ . The  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  inputs internally generate a  $\overline{\text{CAS}}$  signal functioning in an identical manner to the single  $\overline{\text{CAS}}$  input on the other 1M x 16 DRAMs. The key difference is that each  $\overline{\text{CAS}}$  controls its corresponding I/O tristate logic (in conjunction with  $\overline{\text{OE}}$  and  $\overline{\text{WE}}$  and  $\overline{\text{RAS}}$ ).  $\overline{\text{LCAS}}$  controls I/O0 through I/O7 and  $\overline{\text{UCAS}}$  controls I/O8 through I/O15.

The IS45C16100 and IS45LV16100  $\overline{\text{CAS}}$  function is determined by the first  $\overline{\text{CAS}}$  ( $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$ ) transitioning LOW and the last transitioning back HIGH. The two  $\overline{\text{CAS}}$  controls give the IS45C16100 and IS45LV16100 both BYTE READ and BYTE WRITE cycle capabilities.

## Memory Cycle

A memory cycle is initiated by bringing  $\overline{\text{RAS}}$  LOW and it is terminated by returning both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  HIGH. To ensure proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum  $t_{\text{RAS}}$  time has expired. A new cycle must not be initiated until the minimum precharge time  $t_{\text{RP}}$ ,  $t_{\text{CP}}$  has elapsed.

## Read Cycle

A read cycle is initiated by the falling edge of  $\overline{\text{CAS}}$  or  $\overline{\text{OE}}$ , whichever occurs last, while holding  $\overline{\text{WE}}$  HIGH. The column address must be held for a minimum time specified by  $t_{\text{AR}}$ . Data Out becomes valid only when  $t_{\text{RAC}}$ ,  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{OEA}}$  are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

## Write Cycle

A write cycle is initiated by the falling edge of  $\overline{\text{CAS}}$  and  $\overline{\text{WE}}$ , whichever occurs last. The input data must be valid at or before the falling edge of  $\overline{\text{CAS}}$  or  $\overline{\text{WE}}$ , whichever occurs first.

## Auto Refresh Cycle

To retain data, 1,024 refresh cycles are required in each 16 ms period. There are two ways to refresh the memory.

1. By clocking each of the 1,024 row addresses (A0 through A9) with  $\overline{\text{RAS}}$  at least once every 128 ms. Any read, write, read-modify-write or  $\overline{\text{RAS}}$ -only cycle refreshes the addressed row.
2. Using a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle.  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is activated by the falling edge of  $\overline{\text{RAS}}$ ,

while holding  $\overline{\text{CAS}}$  LOW. In  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle, an internal 9-bit counter provides the row addresses and the external address inputs are ignored.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

## Self Refresh Cycle

The Self Refresh allows the user a dynamic refresh, data retention mode at the extended refresh period of 128 ms. i.e., 125  $\mu\text{s}$  per row when using distributed CBR refreshes. The feature also allows the user the choice of a fully static, low power data retention mode. The optional Self Refresh feature is initiated by performing a CBR Refresh cycle and holding  $\overline{\text{RAS}}$  LOW for the specified  $t_{\text{RAS}}$ .

The Self Refresh mode is terminated by driving  $\overline{\text{RAS}}$  HIGH for a minimum time of  $t_{\text{RP}}$ . This delay allows for the completion of any internal refresh cycles that may be in process at the time of the  $\overline{\text{RAS}}$  LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting Self Refresh.

However, if the DRAM controller utilizes a  $\overline{\text{RAS}}$ -only or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

## Extended Data Out Page Mode

EDO page mode operation permits all 1,024 columns within a selected row to be randomly accessed at a high data rate.

In EDO page mode read cycle, the data-out is held to the next  $\overline{\text{CAS}}$  cycle's falling edge, instead of the rising edge. For this reason, the valid data output time in EDO page mode is extended compared with the fast page mode. In the fast page mode, the valid data output time becomes shorter as the  $\overline{\text{CAS}}$  cycle time becomes shorter. Therefore, in EDO page mode, the timing margin in read cycle is larger than that of the fast page mode even if the  $\overline{\text{CAS}}$  cycle time becomes shorter.

In EDO page mode, due to the extended data function, the  $\overline{\text{CAS}}$  cycle time can be shorter than in the fast page mode if the timing margin is the same.

The EDO page mode allows both read and write operations during one  $\overline{\text{RAS}}$  cycle, but the performance is equivalent to that of the fast page mode in that case.

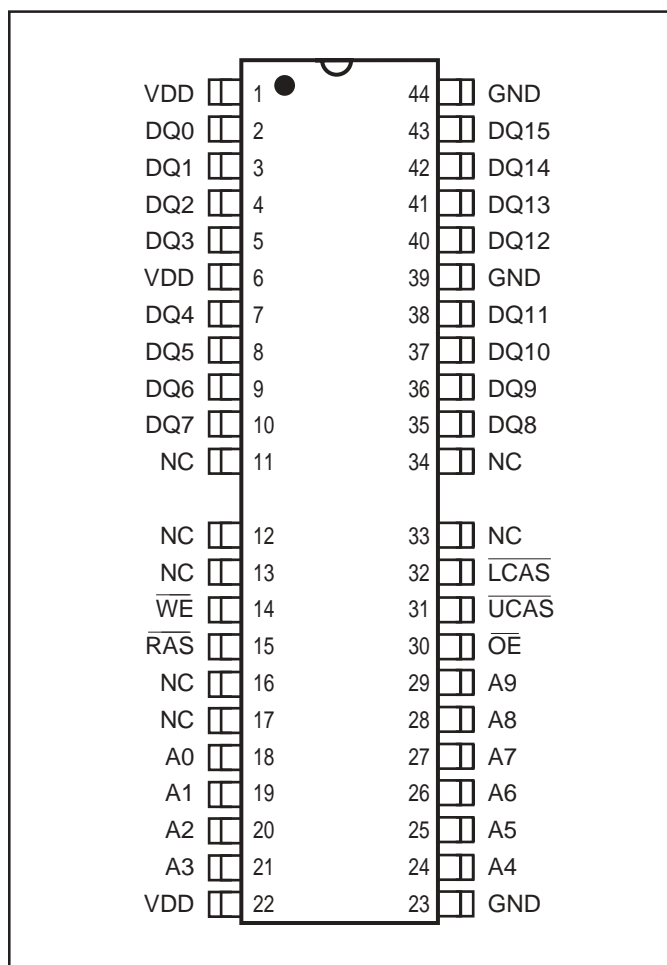
## Power-On

After application of the VDD supply, an initial pause of 200  $\mu\text{s}$  is required followed by a minimum of eight initialization cycles (any combination of cycles containing a  $\overline{\text{RAS}}$  signal).

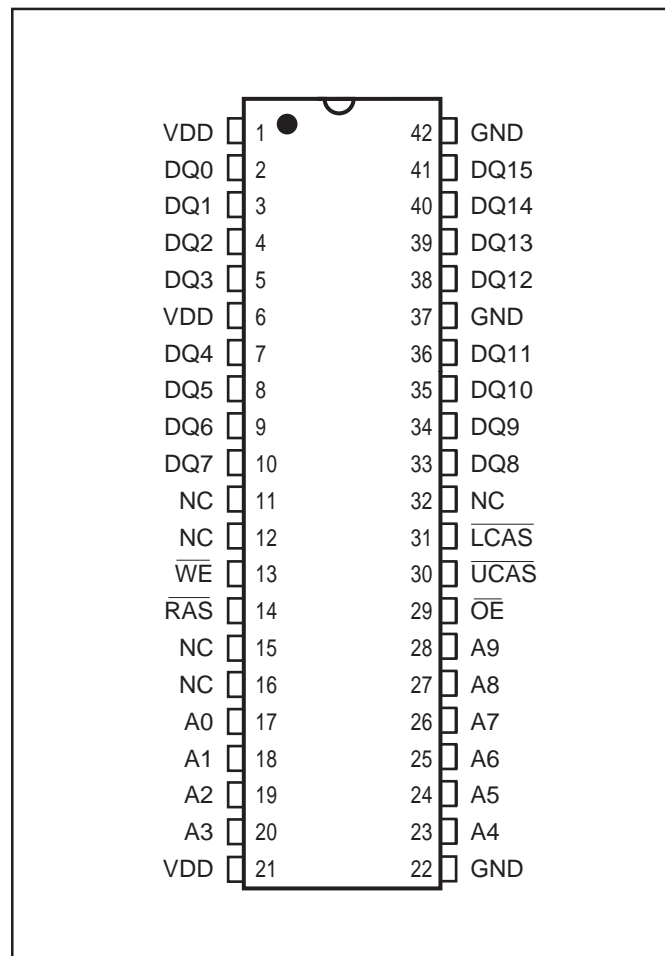
During power-on, it is recommended that  $\overline{\text{RAS}}$  track with VDD or be held at a valid  $V_{\text{IH}}$  to avoid current surges.

## PIN CONFIGURATIONS

### 50(44)-Pin TSOP (Type II)



### 42-Pin SOJ



## PIN DESCRIPTIONS

A0-A9	Address Inputs
DQ0-15	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
VDD	Power
GND	Ground
NC	No Connection

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameters	Rating	Unit
V <sub>T</sub>	Voltage on Any Pin Relative to GND	5V 3.3V	V
V <sub>DD</sub>	Supply Voltage	5V 3.3V	V
I <sub>OUT</sub>	Output Current	50	mA
P <sub>D</sub>	Power Dissipation	1	W
T <sub>STG</sub>	Storage Temperature	–55 to +125	°C

### Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	5V 3.3V	4.5 3.0	5.0 3.3	V
V <sub>IH</sub>	Input High Voltage	5V 3.3V	2.4 2.0	— —	V
V <sub>IL</sub>	Input Low Voltage	5V 3.3V	–1.0 –0.3	— —	V
T <sub>A</sub>	Temperature Range	Option A: Option A1:	0 to +70 –40 to +85		°C

## CAPACITANCE<sup>(1,2)</sup>

Symbol	Parameter	Max.	Unit
C <sub>IN1</sub>	Input Capacitance: A0-A9	5	pF
C <sub>IN2</sub>	Input Capacitance: $\overline{\text{RAS}}$ , $\overline{\text{UCAS}}$ , $\overline{\text{LCAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$	7	pF
C <sub>IO</sub>	Data Input/Output Capacitance: I/O0-I/O15	7	pF

### Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz.

## ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed	Min.	Max.	Unit
I <sub>IL</sub>	Input Leakage Current	Any input $0V \leq V_{IN} \leq V_{DD}$ Other inputs not under test = 0V		-5	5	μA
I <sub>IO</sub>	Output Leakage Current	Output is disabled (Hi-Z) $0V \leq V_{OUT} \leq V_{DD}$		-5	5	μA
V <sub>OH</sub>	Output High Voltage Level	I <sub>OH</sub> = -5.0 mA (5V) I <sub>OH</sub> = -2.0 mA (3.3V)		2.4	—	V
V <sub>OL</sub>	Output Low Voltage Level	I <sub>OL</sub> = 4.2 mA (5V) I <sub>OL</sub> = 2.0 mA (3.3V)		—	0.4	V
I <sub>CC1</sub>	Standby Current: TTL	$\overline{RAS}, \overline{LCAS}, \overline{UCAS} \geq V_{IH}$ Temp Op A: 5V Temp Op A: 3.3V Temp Op A1, : 5V Temp Op A1, : 3.3V		—	3 3 4 4	mA  mA
I <sub>CC2</sub>	Standby Current: CMOS	$\overline{RAS}, \overline{LCAS}, \overline{UCAS} \geq V_{DD} - 0.2V$	5V 3.3V	— —	2 2	mA
I <sub>CC3</sub>	Operating Current: Random Read/Write <sup>(2,3,4)</sup> Average Power Supply Current	$\overline{RAS}, \overline{LCAS}, \overline{UCAS}$ , Address Cycling, t <sub>RC</sub> = t <sub>RC</sub> (min.)	-50 -60	— —	160 145	mA
I <sub>CC4</sub>	Operating Current: EDO Page Mode <sup>(2,3,4)</sup> Average Power Supply Current	$\overline{RAS} = V_{IL}, \overline{LCAS}, \overline{UCAS}$ , Cycling t <sub>PC</sub> = t <sub>PC</sub> (min.)	-50 -60	— —	90 80	mA
I <sub>CC5</sub>	Refresh Current: $\overline{RAS}$ -Only <sup>(2,3)</sup> Average Power Supply Current	$\overline{RAS}$ Cycling, $\overline{LCAS}, \overline{UCAS} \geq V_{IH}$ t <sub>RC</sub> = t <sub>RC</sub> (min.)	-50 -60	— —	160 145	mA
I <sub>CC6</sub>	Refresh Current: CBR <sup>(2,3,5)</sup> Average Power Supply Current	$\overline{RAS}, \overline{LCAS}, \overline{UCAS}$ Cycling t <sub>RC</sub> = t <sub>RC</sub> (min.)	-50 -60	— —	160 145	mA

### Notes:

1. An initial pause of 200 μs is required after power-up followed by eight  $\overline{RAS}$  refresh cycles ( $\overline{RAS}$ -Only or CBR) before proper device operation is assured. The eight  $\overline{RAS}$  cycles wake-up should be repeated any time the t<sub>REF</sub> refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each EDO page cycle.
5. Enables on-chip refresh and address counters.

**AC CHARACTERISTICS** (1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-50		-60		Units
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Random READ or WRITE Cycle Time	84	—	104	—	ns
t <sub>RAC</sub>	Access Time from $\overline{\text{RAS}}$ <sup>(6, 7)</sup>	—	50	—	60	ns
t <sub>CAC</sub>	Access Time from $\overline{\text{CAS}}$ <sup>(6, 8, 15)</sup>	—	13	—	15	ns
t <sub>AA</sub>	Access Time from Column-Address <sup>(6)</sup>	—	25	—	30	ns
t <sub>RAS</sub>	$\overline{\text{RAS}}$ Pulse Width	50	10K	60	10K	ns
t <sub>RP</sub>	$\overline{\text{RAS}}$ Precharge Time	30	—	40	—	ns
t <sub>CAS</sub>	$\overline{\text{CAS}}$ Pulse Width <sup>(26)</sup>	8	10K	10	10K	ns
t <sub>CP</sub>	$\overline{\text{CAS}}$ Precharge Time <sup>(9, 25)</sup>	9	—	9	—	ns
t <sub>CSH</sub>	$\overline{\text{CAS}}$ Hold Time <sup>(21)</sup>	38	—	40	—	ns
t <sub>RCD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time <sup>(10, 20)</sup>	12	37	14	45	ns
t <sub>ASR</sub>	Row-Address Setup Time	0	—	0	—	ns
t <sub>RAH</sub>	Row-Address Hold Time	8	—	10	—	ns
t <sub>ASC</sub>	Column-Address Setup Time <sup>(20)</sup>	0	—	0	—	ns
t <sub>CAH</sub>	Column-Address Hold Time <sup>(20)</sup>	8	—	10	—	ns
t <sub>AR</sub>	Column-Address Hold Time (referenced to $\overline{\text{RAS}}$ )	30	—	40	—	ns
t <sub>RAD</sub>	$\overline{\text{RAS}}$ to Column-Address Delay Time <sup>(11)</sup>	10	25	12	30	ns
t <sub>RAL</sub>	Column-Address to $\overline{\text{RAS}}$ Lead Time	25	—	30	—	ns
t <sub>RPC</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	5	—	5	—	ns
t <sub>RSH</sub>	$\overline{\text{RAS}}$ Hold Time <sup>(27)</sup>	8	—	10	—	ns
t <sub>RHCP</sub>	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	37	—	37	—	ns
t <sub>CLZ</sub>	$\overline{\text{CAS}}$ to Output in Low-Z <sup>(15, 29)</sup>	0	—	0	—	ns
t <sub>CRP</sub>	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time <sup>(21)</sup>	5	—	5	—	ns
t <sub>OD</sub>	Output Disable Time <sup>(19, 28, 29)</sup>	3	15	3	15	ns
t <sub>OE</sub>	Output Enable Time <sup>(15, 16)</sup>	—	13	—	15	ns
t <sub>OED</sub>	Output Enable Data Delay (Write)	20	—	20	—	ns
t <sub>OEHC</sub>	$\overline{\text{OE}}$ HIGH Hold Time from $\overline{\text{CAS}}$ HIGH	5	—	5	—	ns
t <sub>OEP</sub>	$\overline{\text{OE}}$ HIGH Pulse Width	10	—	10	—	ns
t <sub>OES</sub>	$\overline{\text{OE}}$ LOW to $\overline{\text{CAS}}$ HIGH Setup Time	5	—	5	—	ns
t <sub>RCS</sub>	Read Command Setup Time <sup>(17, 20)</sup>	0	—	0	—	ns
t <sub>RRH</sub>	Read Command Hold Time (referenced to $\overline{\text{RAS}}$ ) <sup>(12)</sup>	0	—	0	—	ns
t <sub>RCH</sub>	Read Command Hold Time (referenced to $\overline{\text{CAS}}$ ) <sup>(12, 17, 21)</sup>	0	—	0	—	ns
t <sub>WCH</sub>	Write Command Hold Time <sup>(17, 27)</sup>	8	—	10	—	ns
t <sub>WCR</sub>	Write Command Hold Time (referenced to $\overline{\text{RAS}}$ ) <sup>(17)</sup>	40	—	50	—	ns



**AC CHARACTERISTICS (Continued)**<sup>(1,2,3,4,5,6)</sup>

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-50		-60		Units
		Min.	Max.	Min.	Max.	
tWP	Write Command Pulse Width <sup>(17)</sup>	8	—	10	—	ns
tWPZ	$\overline{WE}$ Pulse Widths to Disable Outputs	10	—	10	—	ns
tRWL	Write Command to $\overline{RAS}$ Lead Time <sup>(17)</sup>	13	—	15	—	ns
tcWL	Write Command to $\overline{CAS}$ Lead Time <sup>(17, 21)</sup>	8	—	10	—	ns
twCS	Write Command Setup Time <sup>(14, 17, 20)</sup>	0	—	0	—	ns
tDHR	Data-in Hold Time (referenced to $\overline{RAS}$ )	39	—	39	—	ns
tACH	Column-Address Setup Time to $\overline{CAS}$ Precharge during WRITE Cycle	15	—	15	—	ns
toEH	$\overline{OE}$ Hold Time from $\overline{WE}$ during READ-MODIFY-WRITE cycle <sup>(18)</sup>	8	—	10	—	ns
tdS	Data-In Setup Time <sup>(15, 22)</sup>	0	—	0	—	ns
tdH	Data-In Hold Time <sup>(15, 22)</sup>	8	—	10	—	ns
trWC	READ-MODIFY-WRITE Cycle Time	108	—	133	—	ns
trWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time during READ-MODIFY-WRITE Cycle <sup>(14)</sup>	64	—	77	—	ns
tcWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time <sup>(14, 20)</sup>	26	—	32	—	ns
tAWD	Column-Address to $\overline{WE}$ Delay Time <sup>(14)</sup>	39	—	47	—	ns
tPC	EDO Page Mode READ or WRITE Cycle Time <sup>(24)</sup>	20	—	25	—	ns
trASP	$\overline{RAS}$ Pulse Width in EDO Page Mode	50	100K	60	100K	ns
tCPA	Access Time from $\overline{CAS}$ Precharge <sup>(15)</sup>	—	30	—	35	ns
tPRWC	EDO Page Mode READ-WRITE Cycle Time <sup>(24)</sup>	56	—	68	—	ns
tCOH	Data Output Hold after $\overline{CAS}$ LOW	5	—	5	—	ns
tOFF	Output Buffer Turn-Off Delay from $\overline{CAS}$ or $\overline{RAS}$ <sup>(13,15,19, 29)</sup>	1.6	12	1.6	15	ns
tWHZ	Output Disable Delay from $\overline{WE}$	3	10	3	10	ns
tCLCH	Last $\overline{CAS}$ going LOW to First $\overline{CAS}$ returning HIGH <sup>(23)</sup>	10	—	10	—	ns
tCSR	$\overline{CAS}$ Setup Time (CBR REFRESH) <sup>(30, 20)</sup>	5	—	5	—	ns
tCHR	$\overline{CAS}$ Hold Time (CBR REFRESH) <sup>(30, 21)</sup>	8	—	10	—	ns
tORD	$\overline{OE}$ Setup Time prior to $\overline{RAS}$ during HIDDEN REFRESH Cycle	0	—	0	—	ns
tREF	Auto Refresh Period (1,024 Cycles)	—	16	—	16	ms
tREF	Self Refresh Period (1,024 Cycles)	—	128	—	128	ms
tr	Transition Time (Rise or Fall) <sup>(2, 3)</sup>	1	50	1	50	ns

## AC TEST CONDITIONS

Output load: Two TTL Loads and 50 pF ( $V_{DD} = 5.0V \pm 10\%$ )

One TTL Load and 50 pF ( $V_{DD} = 3.3V \pm 10\%$ )

Input timing reference levels:  $V_{IH} = 2.4V$ ,  $V_{IL} = 0.8V$  ( $V_{DD} = 5.0V \pm 10\%$ );

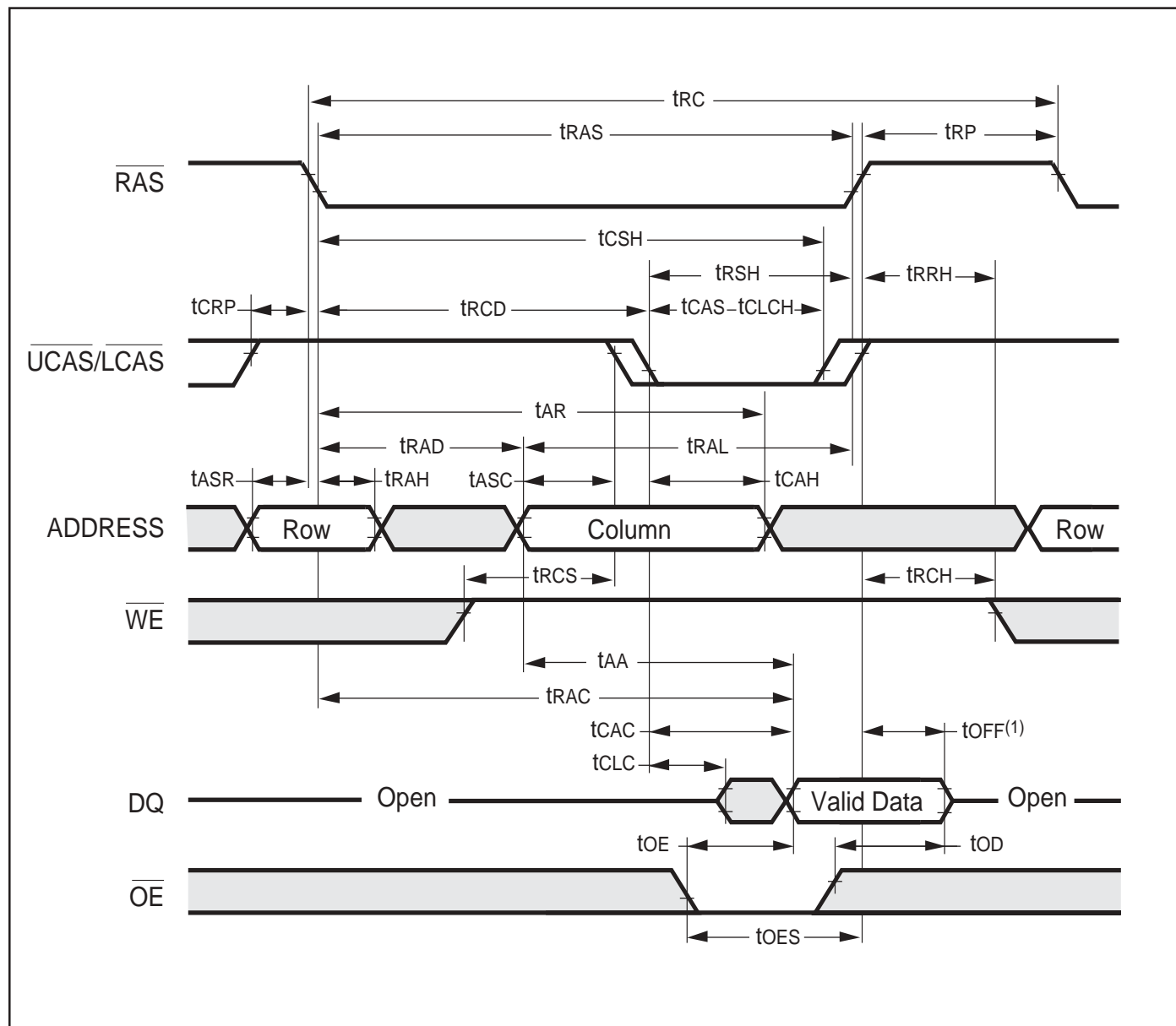
$V_{IH} = 2.0V$ ,  $V_{IL} = 0.8V$  ( $V_{DD} = 3.3V \pm 10\%$ )

Output timing reference levels:  $V_{OH} = 2.0V$ ,  $V_{OL} = 0.8V$  ( $V_{DD} = 5V \pm 10\%$ ,  $3.3V \pm 10\%$ )

### Notes:

1. An initial pause of 200  $\mu s$  is required after power-up followed by eight  $\overline{RAS}$  refresh cycle ( $\overline{RAS}$ -Only or CBR) before proper device operation is assured. The eight  $\overline{RAS}$  cycles wake-up should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
2.  $V_{IH}$  (MIN) and  $V_{IL}$  (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
4. If  $\overline{CAS}$  and  $\overline{RAS} = V_{IH}$ , data output is High-Z.
5. If  $\overline{CAS} = V_{IL}$ , data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that  $t_{RCD} = t_{RCD} (MAX)$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
8. Assumes that  $t_{RCD} \bullet t_{RCD} (MAX)$ .
9. If  $\overline{CAS}$  is LOW at the falling edge of  $\overline{RAS}$ , data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer,  $\overline{CAS}$  and  $\overline{RAS}$  must be pulsed for  $t_{CP}$ .
10. Operation with the  $t_{RCD} (MAX)$  limit ensures that  $t_{RAC} (MAX)$  can be met.  $t_{RCD} (MAX)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD} (MAX)$  limit, access time is controlled exclusively by  $t_{CAC}$ .
11. Operation within the  $t_{RAD} (MAX)$  limit ensures that  $t_{RCD} (MAX)$  can be met.  $t_{RAD} (MAX)$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD} (MAX)$  limit, access time is controlled exclusively by  $t_{AA}$ .
12. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a READ cycle.
13.  $t_{OFF} (MAX)$  defines the time at which the output achieves the open circuit condition; it is not a reference to  $V_{OH}$  or  $V_{OL}$ .
14.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If  $t_{WCS} \bullet t_{WCS} (MIN)$ , the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If  $t_{RWD} \bullet t_{RWD} (MIN)$ ,  $t_{AWD} \bullet t_{AWD} (MIN)$  and  $t_{CWD} \bullet t_{CWD} (MIN)$ , the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until  $\overline{CAS}$  and  $\overline{RAS}$  or  $\overline{OE}$  go back to  $V_{IH}$ ) is indeterminate.  $\overline{OE}$  held HIGH and  $\overline{WE}$  taken LOW after  $\overline{CAS}$  goes LOW result in a LATE WRITE ( $\overline{OE}$ -controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding  $\overline{CAS}$  input, I/O0-I/O7 by  $\overline{LCAS}$  and I/O8-I/O15 by  $\overline{UCAS}$ .
16. During a READ cycle, if  $\overline{OE}$  is LOW then taken HIGH before  $\overline{CAS}$  goes HIGH, I/O goes open. If  $\overline{OE}$  is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as  $\overline{WE}$  going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both  $t_{OD}$  and  $t_{OE}$  met ( $\overline{OE}$  HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if  $\overline{CAS}$  remains LOW and  $\overline{OE}$  is taken back to LOW after  $t_{OE}$  is met.
19. The I/Os are in open during READ cycles once  $t_{OD}$  or  $t_{OFF}$  occur.
20. The first  $\chi\overline{CAS}$  edge to transition LOW.
21. The last  $\chi\overline{CAS}$  edge to transition HIGH.
22. These parameters are referenced to  $\overline{CAS}$  leading edge in EARLY WRITE cycles and  $\overline{WE}$  leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. Last falling  $\chi\overline{CAS}$  edge to first rising  $\chi\overline{CAS}$  edge.
24. Last rising  $\chi\overline{CAS}$  edge to next cycle's last rising  $\chi\overline{CAS}$  edge.
25. Last rising  $\chi\overline{CAS}$  edge to first falling  $\chi\overline{CAS}$  edge.
26. Each  $\chi\overline{CAS}$  must meet minimum pulse width.
27. Last  $\chi\overline{CAS}$  to go LOW.
28. I/Os controlled, regardless  $\overline{UCAS}$  and  $\overline{LCAS}$ .
29. The 3 ns minimum is a parameter guaranteed by design.
30. Enables on-chip refresh and address counters.

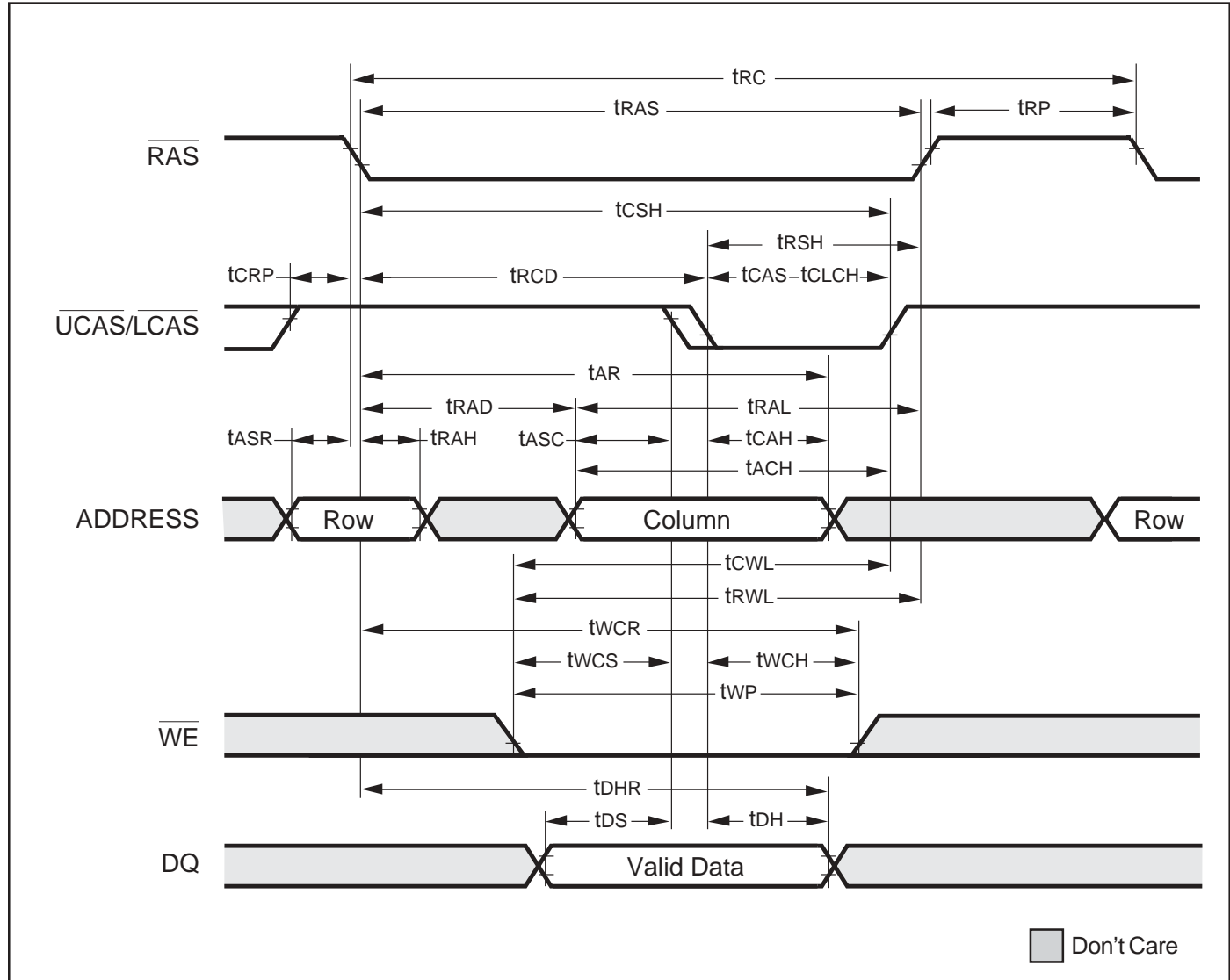
## READ CYCLE



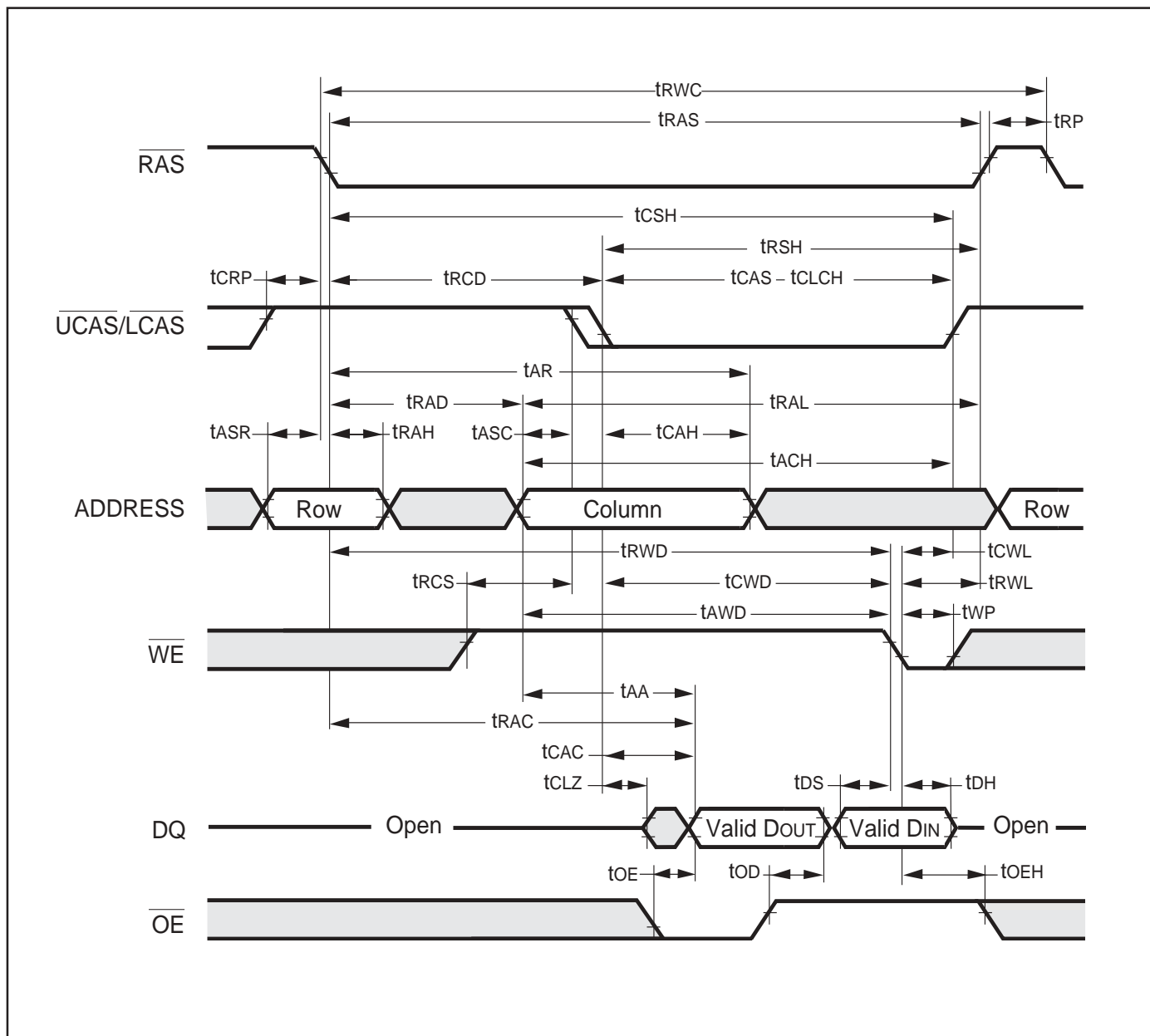
**Note:**

1.  $t_{\text{OFF}}$  is referenced from rising edge of  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$ , whichever occurs last.

EARLY WRITE CYCLE ( $\overline{OE}$  = DON'T CARE)



**READ WRITE CYCLE** (LATE WRITE and READ-MODIFY-WRITE Cycles)



The diagram illustrates the timing relationships for a 2D DRAM array. The signals and their timing parameters are as follows:

- RAS:** RAS enable signal. Timing parameters include  $t_{RASP}$  (RAS pulse width),  $t_{CRP}$  (RAS to UCAS/LCAS setup),  $t_{CSH}$  (RAS to UCAS/LCAS hold),  $t_{PC(1)}$  (RAS to UCAS/LCAS precharge),  $t_{RSH}$  (RAS to UCAS/LCAS setup), and  $t_{RPH}$  (RAS to UCAS/LCAS hold).
- UCAS/LCAS:** UCAS/LCAS enable signal. Timing parameters include  $t_{RCD}$  (RAS to UCAS/LCAS delay),  $t_{CAS, t_{CLCH}}$  (UCAS/LCAS to RAS delay),  $t_{CP}$  (UCAS/LCAS to RAS precharge),  $t_{CAS, t_{CLCH}}$  (UCAS/LCAS to RAS delay), and  $t_{CP}$  (UCAS/LCAS to RAS precharge).
- ADDRESS:** Address signal. Timing parameters include  $t_{ASR}$  (ADDRESS to UCAS/LCAS setup),  $t_{ASR}$  (ADDRESS to UCAS/LCAS setup),  $t_{ASC}$  (ADDRESS to UCAS/LCAS setup),  $t_{CAH}$  (ADDRESS to UCAS/LCAS hold),  $t_{ASC}$  (ADDRESS to UCAS/LCAS setup),  $t_{CAH}$  (ADDRESS to UCAS/LCAS hold),  $t_{ASC}$  (ADDRESS to UCAS/LCAS setup),  $t_{CAH}$  (ADDRESS to UCAS/LCAS hold),  $t_{RAH}$  (ADDRESS to UCAS/LCAS hold),  $t_{RCH}$  (ADDRESS to UCAS/LCAS hold), and  $t_{RRH}$  (ADDRESS to UCAS/LCAS hold).
- WE:** Write Enable signal. Timing parameters include  $t_{RCS}$  (WE to UCAS/LCAS setup),  $t_{RCH}$  (WE to UCAS/LCAS hold),  $t_{TAA}$  (WE to UCAS/LCAS delay),  $t_{CPA}$  (WE to UCAS/LCAS delay),  $t_{CAC}$  (WE to UCAS/LCAS delay),  $t_{CLZ}$  (WE to UCAS/LCAS delay),  $t_{TOFF}$  (WE to UCAS/LCAS delay), and  $t_{TOH}$  (WE to UCAS/LCAS delay).
- DQ:** Data bus signal. Timing parameters include  $t_{OE}$  (OE to DQ delay),  $t_{OES}$  (OE to DQ setup),  $t_{OD}$  (OE to DQ delay),  $t_{OEHC}$  (OE to DQ delay),  $t_{TOE}$  (OE to DQ delay),  $t_{TOES}$  (OE to DQ setup), and  $t_{TOD}$  (OE to DQ delay).
- OE:** Output Enable signal. Timing parameters include  $t_{OE}$  (OE to DQ delay),  $t_{OES}$  (OE to DQ setup),  $t_{OD}$  (OE to DQ delay),  $t_{OEHC}$  (OE to DQ delay),  $t_{TOE}$  (OE to DQ delay),  $t_{TOES}$  (OE to DQ setup), and  $t_{TOD}$  (OE to DQ delay).

Legend:

- Undefined (X symbol)
- Don't Care (Gray box)

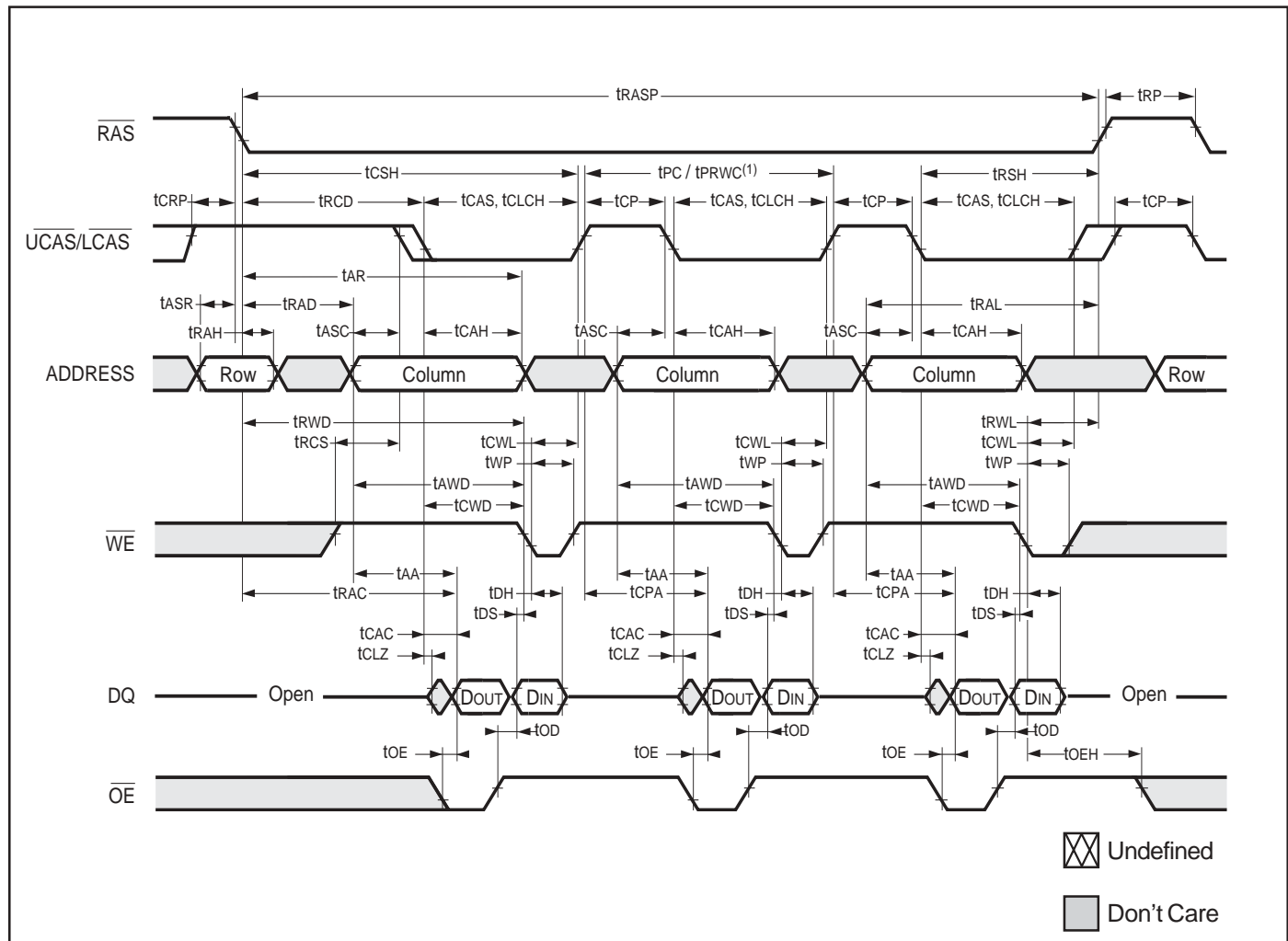
Rev. 00A  
10/21/02

The diagram illustrates the timing relationships for a 2D DRAM array. The signals and their timing parameters are as follows:

- RAS:** RAS Enable signal. Timing parameters include  $t_{RASP}$  (RAS pulse width),  $t_{RHCP}$  (RAS hold time), and  $t_{RP}$  (RAS precharge time).
- UCAS/LCAS:** UCAS/LCAS Enable signal. Timing parameters include  $t_{CRP}$  (UCAS/LCAS precharge time),  $t_{CD}$  (UCAS/LCAS delay),  $t_{CAS}$  (UCAS/LCAS access time),  $t_{CLCH}$  (UCAS/LCAS column hit time),  $t_{CP}$  (UCAS/LCAS precharge time),  $t_{RSH}$  (UCAS/LCAS row hit time), and  $t_{CP}$  (UCAS/LCAS precharge time).
- ADDRESS:** Address signal. Timing parameters include  $t_{AR}$  (ADDRESS delay),  $t_{AD}$  (ADDRESS delay),  $t_{ACH}$  (ADDRESS hit time),  $t_{AL}$  (ADDRESS delay),  $t_{SR}$  (ADDRESS precharge time),  $t_{SC}$  (ADDRESS delay),  $t_{CAH}$  (ADDRESS hit time),  $t_{SC}$  (ADDRESS delay),  $t_{CAH}$  (ADDRESS hit time),  $t_{SC}$  (ADDRESS delay),  $t_{CAH}$  (ADDRESS hit time), and  $t_{RAH}$  (ADDRESS delay).
- WE:** Write Enable signal. Timing parameters include  $t_{WCR}$  (WE delay),  $t_{DHR}$  (WE delay),  $t_{DS}$  (WE delay),  $t_{DH}$  (WE delay),  $t_{WCH}$  (WE hit time),  $t_{WP}$  (WE precharge time), and  $t_{RWL}$  (WE delay).
- DQ:** Data signal. Timing parameters include  $t_{DQ}$  (DQ delay),  $t_{DQ}$  (DQ delay),  $t_{DQ}$  (DQ delay), and  $t_{DQ}$  (DQ delay).
- OE:** Output Enable signal. Timing parameters include  $t_{OE}$  (OE delay).

The diagram shows the sequence of operations: Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE), and Data Output Enable (OE). The data is valid during the RAS and CAS pulses. The timing parameters are defined relative to the signal transitions.

# EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY WRITE Cycles)

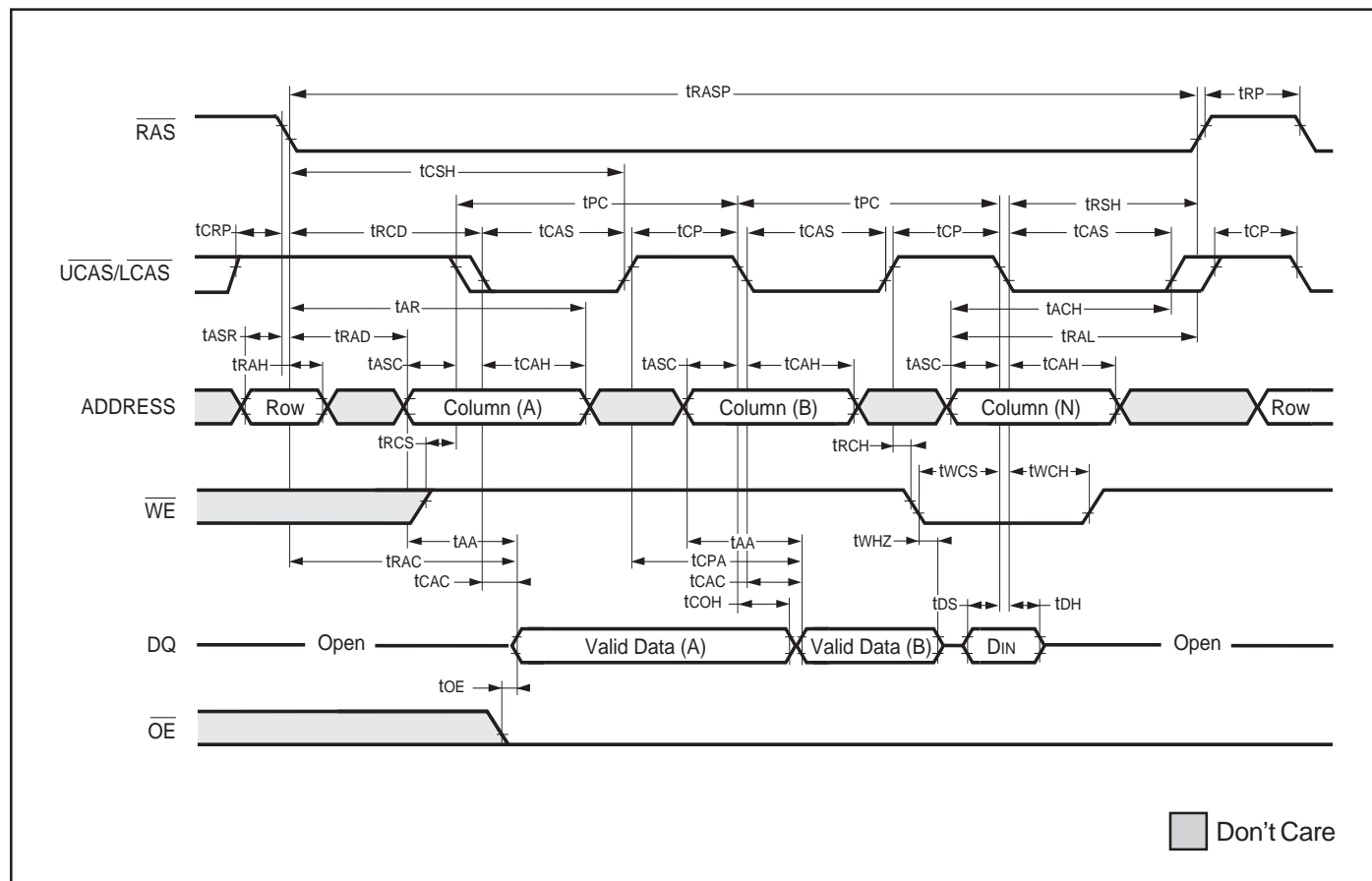


## Note:

1.  $t_{PC}$  can be measured from falling edge of  $\overline{CAS}$  to falling edge of  $\overline{CAS}$ , or from rising edge of  $\overline{CAS}$  to rising edge of  $\overline{CAS}$ . Both measurements must meet the  $t_{PC}$  specifications.

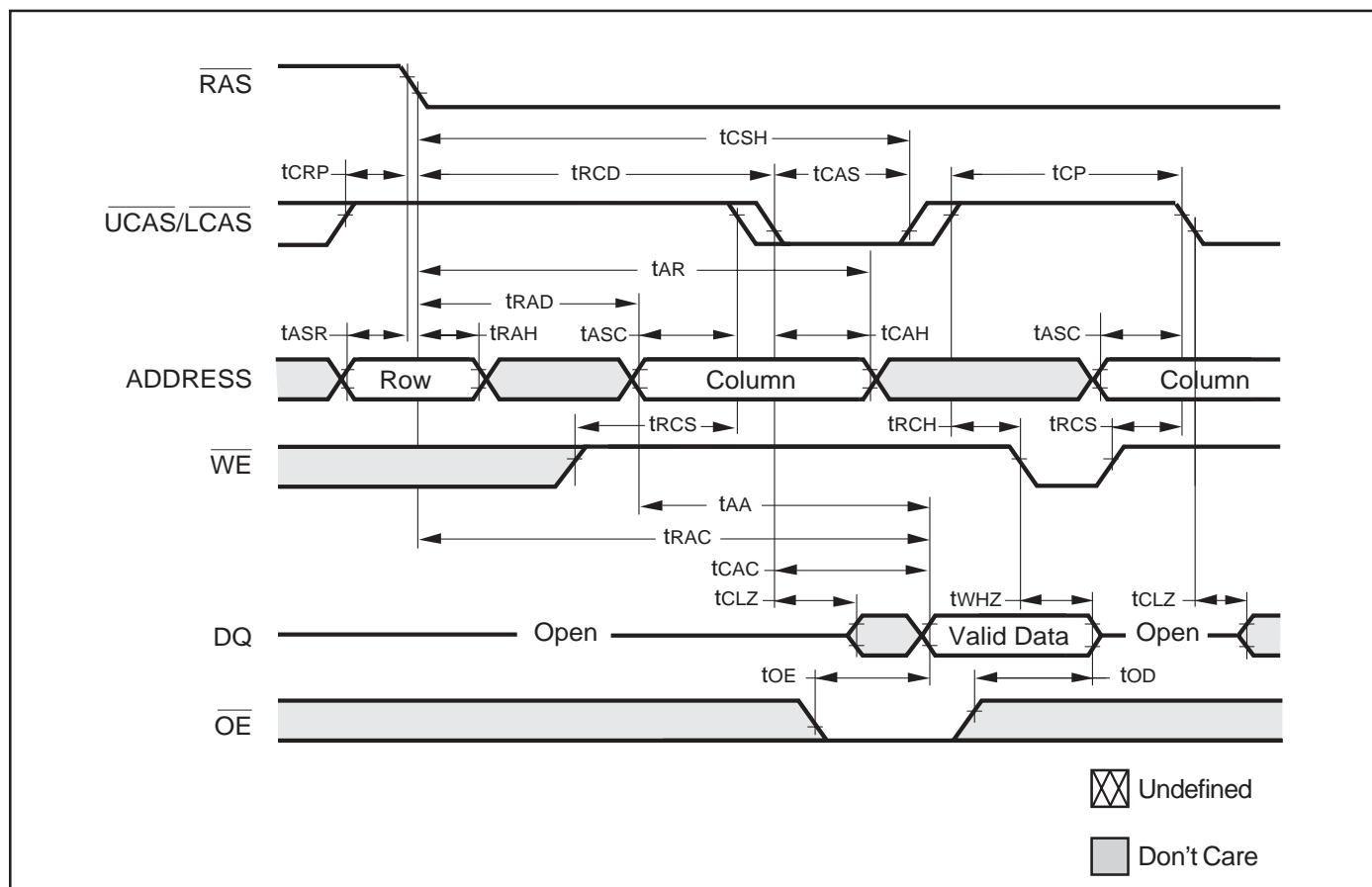


**EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Psuedo READ-MODIFY WRITE)**

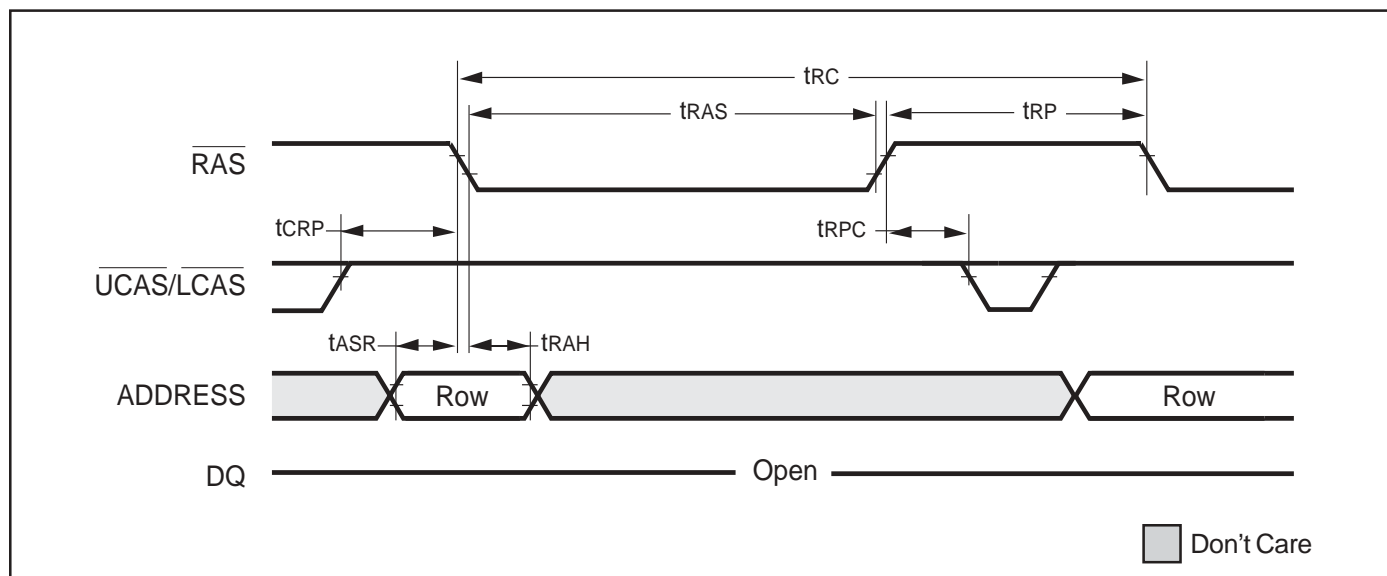


## AC WAVEFORMS

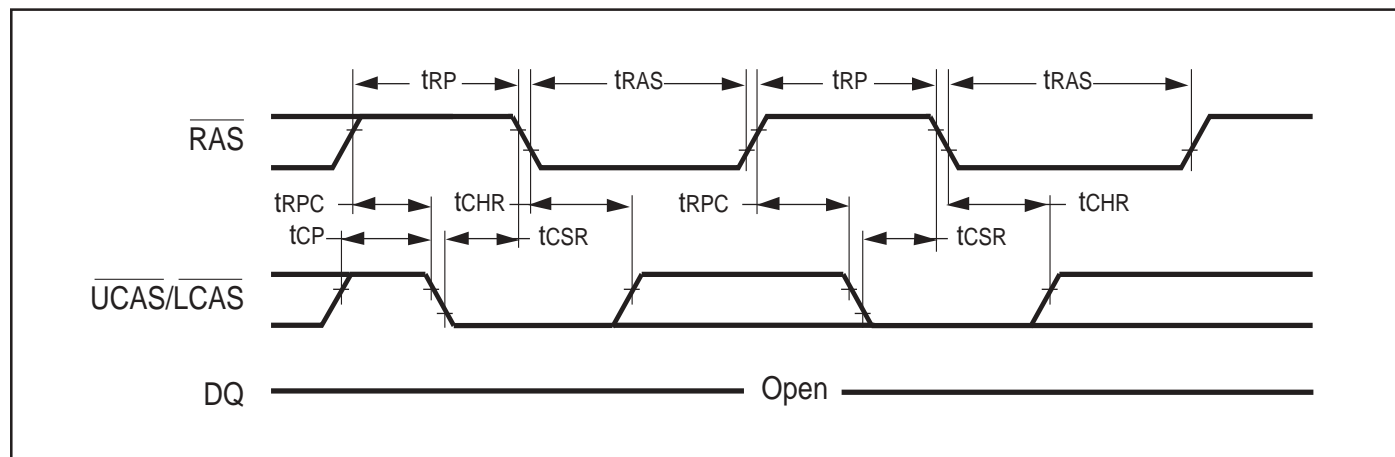
### READ CYCLE (With $\overline{WE}$ -Controlled Disable)



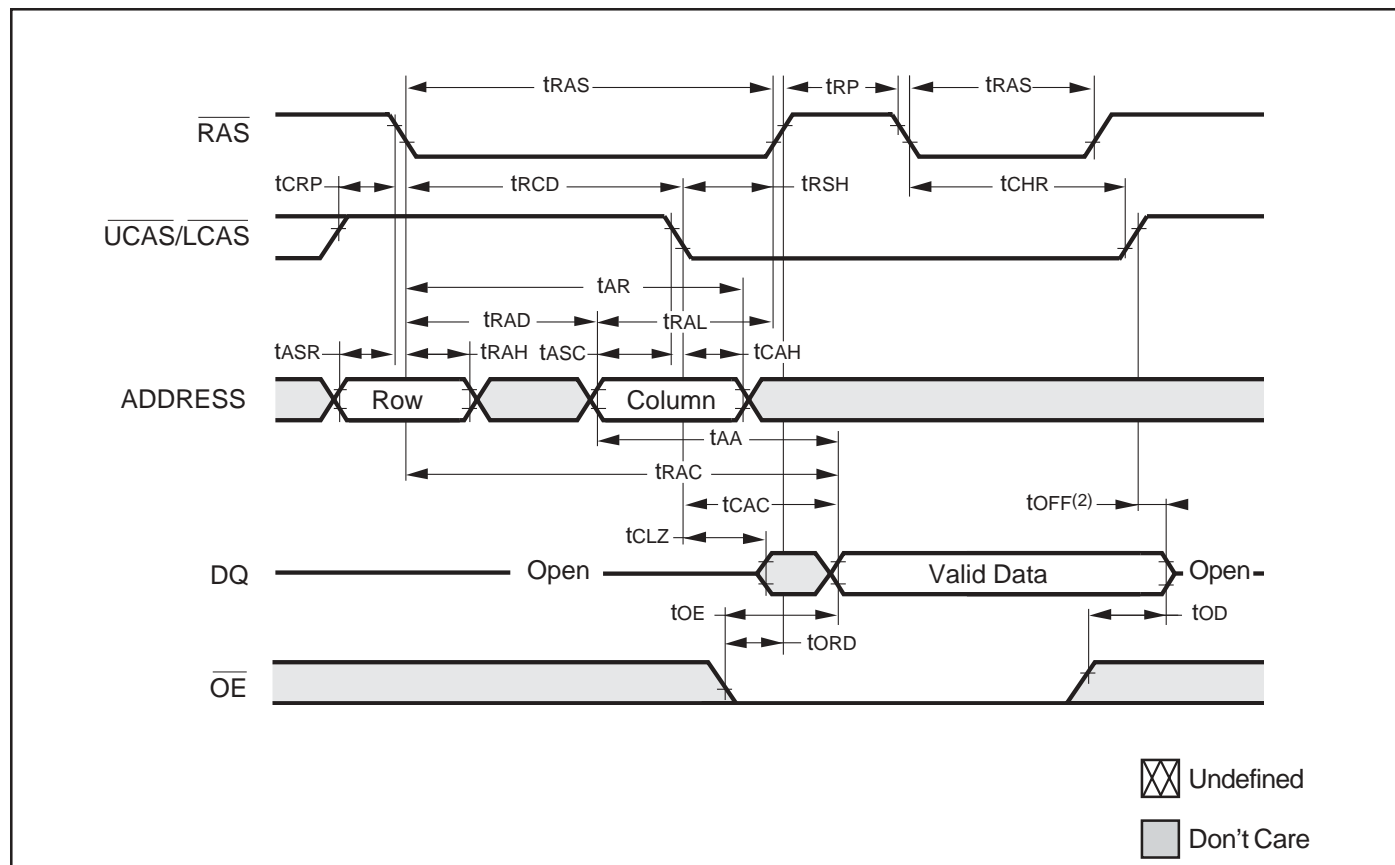
### $\overline{RAS}$ -ONLY REFRESH CYCLE ( $\overline{OE}$ , $\overline{WE}$ = DON'T CARE)



**$\overline{\text{CBR}}$  REFRESH CYCLE** (Addresses;  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$  = DON'T CARE)



**HIDDEN REFRESH CYCLE<sup>(1)</sup>** ( $\overline{\text{WE}}$  = HIGH;  $\overline{\text{OE}}$  = LOW)



**Notes:**

1. A Hidden Refresh may also be performed after a Write Cycle. In this case,  $\overline{\text{WE}}$  = LOW and  $\overline{\text{OE}}$  = HIGH.
2.  $t_{off}$  is referenced from rising edge of RAS or CAS, whichever occurs last.

**ORDERING INFORMATION : 5V**

**Temperature Range Option A: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
50	IS45C16100-50KA	400-mil SOJ
	IS45C16100-50TA	400-mil TSOP (Type II)
60	IS45LV16100-60KA	400-mil SOJ
	IS45LV16100-60TA	400-mil TSOP (Type II)

**Temperature Range Option A1: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
50	IS45C16100-50KA1	400-mil SOJ
	IS45C16100-50TA1	400-mil TSOP (Type II)
60	IS45LV16100-60KA1	400-mil SOJ
	IS45LV16100-60TA1	400-mil TSOP (Type II)

**ORDERING INFORMATION : 3.3V**

**Temperature Range Option A: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
50	IS45C16100-50KA	400-mil SOJ
	IS45C16100-50TA	400-mil TSOP (Type II)
60	IS45LV16100-60KA	400-mil SOJ
	IS45LV16100-60TA	400-mil TSOP (Type II)

**Temperature Range Option A1: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
50	IS45C16100-50KA1	400-mil SOJ
	IS45C16100-50TA1	400-mil TSOP (Type II)
60	IS45LV16100-60KA1	400-mil SOJ
	IS45LV16100-60TA1	400-mil TSOP (Type II)