# 3.3V CMOS 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

## IDT74LVCH16601A

## FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC}$ = 3.3V ±0.3V, Normal Range
- $V_{CC}$ = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

**Drive Features for LVCH16601A:**

- High Output Drivers: ±24mA
- Reduced system switching noise

## APPLICATIONS:

- *5V and 3.3V mixed voltage systems*
- *Data communication and telecommunication systems*

## DESCRIPTION

The LVCH16601A 18-bit universal bus transceiver is built using advanced dual metal CMOS technology. The LVCH16601A combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latched-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs.

For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA and $\overline{CLKENBA}$.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH16601A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16601A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## Functional Block Diagram



TO 17 OTHER CHANNELS
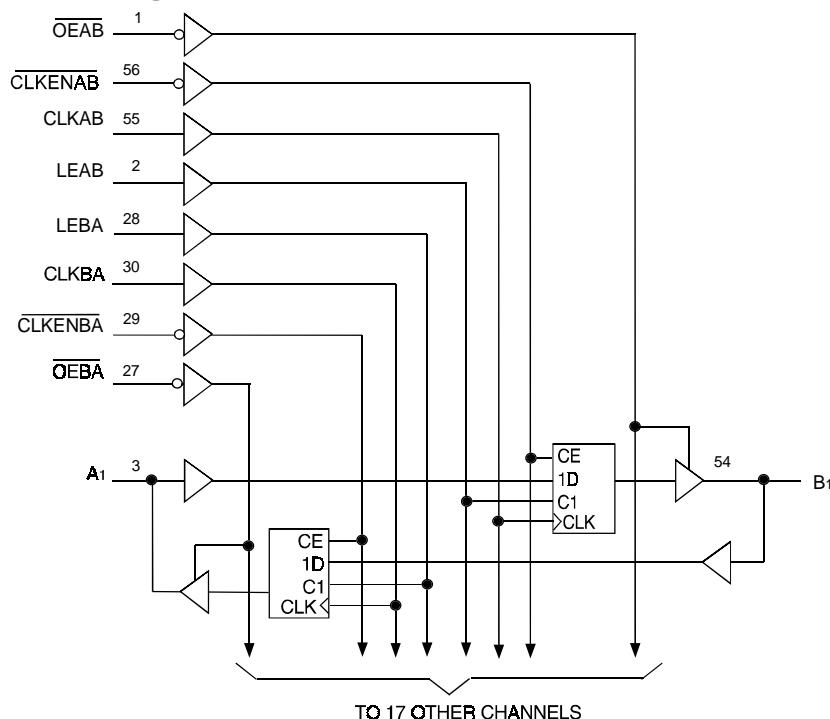
**EXTENDED COMMERCIAL TEMPERATURE RANGE**

**MARCH 1999**

## PIN CONFIGURATION

```
        ___
OEAB  [  1      56  ] CLKENAB
LEAB  [  2      55  ] CLKAB
A1    [  3      54  ] B1
GND   [  4      53  ] GND
A2    [  5      52  ] B2
A3    [  6      51  ] B3
VCC   [  7      50  ] VCC
A4    [  8      49  ] B4
A5    [  9      48  ] B5
A6    [ 10      47  ] B6
GND   [ 11      46  ] GND
A7    [ 12      45  ] B7
A8    [ 13      44  ] B8
A9    [ 14  SO56-1  43  ] B9
A10   [ 15  SO56-2  42  ] B10
A11   [ 16  SO56-3  41  ] B11
A12   [ 17      40  ] B12
GND   [ 18      39  ] GND
A13   [ 19      38  ] B13
A14   [ 20      37  ] B14
A15   [ 21      36  ] B15
VCC   [ 22      35  ] VCC
A16   [ 23      34  ] B16
A17   [ 24      33  ] B17
GND   [ 25      32  ] GND
A18   [ 26      31  ] B18
OEBA  [ 27      30  ] CLKBA
LEBA  [ 28      29  ] CLKENBA
```
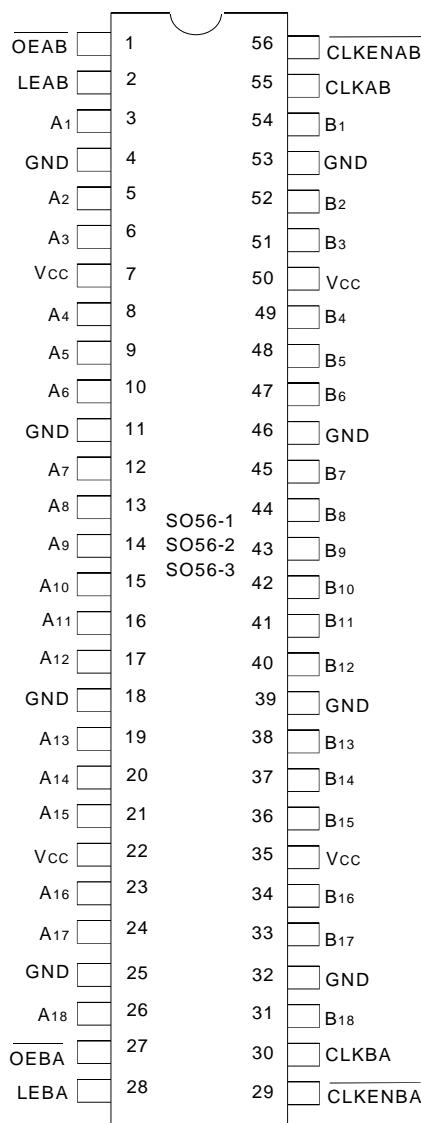
**SSOP/ TSSOP/ TVSOP**
**TOP VIEW**

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| $\overline{\text{OEAB}}$ | A-to-B Output Enable Input (Active LOW) |
| $\overline{\text{OEBA}}$ | B-to-A Output Enable Input (Active LOW) |
| LEAB | A-to-B Latch Enable Input |
| LEBA | B-to-A Latch Enable Input |
| CLKAB | A-to-B Clock Input |
| CLKBA | B-to-A Clock Input |
| Ax | A-to-B Data Inputs or B-to-A 3-State Outputs[1] |
| Bx | B-to-A Data Inputs or A-to-B 3-State Outputs[1] |
| $\overline{\text{CLKENAB}}$ | A-to-B Clock Enable Input (Active LOW) |
| $\overline{\text{CLKENBA}}$ | B-to-A Clock Enable Input (Active LOW) |

**NOTE:**
1.   These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

## ABSOLUTE MAXIMUM RATINGS [1]

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{TERM}$[2] | Terminal Voltage with Respect to GND | – 0.5 to +6.5 | V |
| $V_{TERM}$[3] | Terminal Voltage with Respect to GND | – 0.5 to +6.5 | V |
| $T_{STG}$ | Storage Temperature | – 65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | – 50 to +50 | mA |
| $I_{IK}$ $I_{OK}$ | Continuous Clamp Current, $V_I$ < 0 or $V_O$ < 0 | – 50 | mA |
| $I_{CC}$ $I_{SS}$ | Continuous Current through each $V_{CC}$ or GND | ±100 | mA |

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**NOTES:**
1.   Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2.   $V_{CC}$ terminals.
3.   All terminals except $V_{CC}$.

## CAPACITANCE $(T_A = +25^O C, f = 1.0MHz)$

| Symbol | Parameter[1] | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 4.5 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 6.5 | 8 | pF |
| $C_{I/O}$ | I/O Port Capacitance | $V_{IN}$ = 0V | 6.5 | 8 | pF |

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**NOTE:**
1.   As applicable to the device type.

## FUNCTION TABLE [1, 2]

| Inputs | | | | | Outputs |
|---|---|---|---|---|---|
| $\overline{\text{CLKENAB}}$ | $\overline{\text{OEAB}}$ | LEAB | CLKAB | Ax | Bx |
| X | H | X | X | X | Z |
| X | L | H | X | L | L |
| X | L | H | X | H | H |
| H | L | L | X | X | $B_0$[3] |
| L | L | L | ↑ | L | L |
| L | L | L | ↑ | H | H |
| L | L | L | L | X | $B_0$[3] |
| L | L | L | H | X | $B_0$[4] |

**NOTES:**
1.   H = HIGH Voltage Level
     L = LOW Voltage Level
     X = Don't Care
     Z = High-Impedance
     ↑ = LOW-to-HIGH Transition
2.   A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, CLKBA and $\overline{\text{CLKENBA}}$.
3.   Output level before the indicated steady-state input conditions were established.
4.   Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

**Following Conditions Apply Unless Otherwise Specified:**
**Operating Condition: TA = –40°C to +85°C**

| Symbol | Parameter | Test Conditions | | Min. | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 2 | — | — | |
| $V_{IL}$ | Input LOW Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | — | — | 0.8 | |
| $I_{IH}$ $I_{IL}$ | Input Leakage Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 5.5V | — | — | ±5 | µA |
| $I_{OZH}$ $I_{OZL}$ | High Impedance Output Current (3-State Output pins) | $V_{CC}$ = 3.6V | $V_O$ = 0 to 5.5V | — | — | ±10 | µA |
| $I_{OFF}$ | Input/Output Power Off Leakage | $V_{CC}$ = 0V, $V_{IN}$ or $V_O$ ≤ 5.5V | | — | — | ±50 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = 2.3V, $I_{IN}$ = – 18mA | | — | – 0.7 | – 1.2 | V |
| $V_H$ | Input Hysteresis | $V_{CC}$ = 3.3V | | — | 100 | — | mV |
| $I_{CCL}$ $I_{CCH}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V | $V_{IN}$ = GND or $V_{CC}$ | — | — | 10 | µA |
| $I_{CCZ}$ | | | 3.6 ≤ $V_{IN}$ ≤ 5.5V[2] | — | — | 10 | |
| $\Delta I_{CC}$ | Quiescent Power Supply Current Variation | One input at $V_{CC}$ - 0.6V other inputs at $V_{CC}$ or GND | | — | — | 500 | µA |

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**NOTES:**
1. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

## BUS-HOLD CHARACTERISTICS

| Symbol | Parameter[1] | Test Conditions | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 3.0V | $V_I$ = 2.0V | – 75 | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.8V | 75 | — | — | |
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 2.3V | $V_I$ = 1.7V | — | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.7V | — | — | — | |
| $I_{BHHO}$ $I_{BHLO}$ | Bus-Hold Input Overdrive Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 3.6V | — | — | ± 500 | µA |

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**NOTES:**
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OH}$ = − 0.1mA | $V_{CC}$ – 0.2 | — | V |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = − 6mA | 2 | — | |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = − 12mA | 1.7 | — | |
| | | $V_{CC}$ = 2.7V | | 2.2 | — | |
| | | $V_{CC}$ = 3.0V | | 2.4 | — | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = − 24mA | 2.2 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OL}$ = 0.1mA | — | 0.2 | V |
| | | $V_{CC}$ = 2.3V | $I_{OL}$ = 6mA | — | 0.4 | |
| | | | $I_{OL}$ = 12mA | — | 0.7 | |
| | | $V_{CC}$ = 2.7V | $I_{OL}$ = 12mA | — | 0.4 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 24mA | — | 0.55 | |

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**NOTE:**

1. $V_{IH}$ and $V_{IL}$ must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate $V_{CC}$ range. $T_A$ = − 40°C to +85°C.

## OPERATING CHARACTERISTICS, $V_{CC}$ = 3.3V ± 0.3V, $T_A$ = 25°C

| Symbol | Parameter | Test Conditions | Typical | Unit |
|---|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance per transceiver Outputs enabled | $C_L$ = 0pF, f = 10Mhz | | pF |
| $C_{PD}$ | Power Dissipation Capacitance per transceiver Outputs disabled | | | pF |

## SWITCHING CHARACTERISTICS (1)

| Symbol | Parameter | | Vcc = 2.7V | | Vcc = 3.3V±0.3V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| tPLH tPHL | Propagation Delay Ax to Bx or Bx to Ax | | — | 5.4 | — | 4.6 | ns |
| tPLH tPHL | Propagation Delay LEBA to Ax, LEAB to Bx | | — | 6.2 | — | 5.2 | ns |
| tPLH tPHL | Propagation Delay CLKBA to Ax, CLKAB to Bx | | — | 6.3 | — | 5.3 | ns |
| tPZH tPZL | Output Enable Time $\overline{OEBA}$ to Ax, $\overline{OEAB}$ to Bx | | — | 6.8 | — | 5.6 | ns |
| tPHZ tPLZ | Output Disable Time $\overline{OEBA}$ to Ax, $\overline{OEAB}$ to Bx | | — | 6 | — | 5.2 | ns |
| tSU | Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA | | 1.5 | — | 1.5 | — | ns |
| tH | Hold Time HIGH or LOW Ax after CLKAB, Bx after CLKBA | | 0.8 | — | 0.8 | — | ns |
| tSU | Set-up Time HIGH or LOW Ax to LEAB, Bx to LEBA | Clock LOW | 1 | — | 1 | — | ns |
| | | Clock HIGH | 1 | — | 1 | — | ns |
| tSU | Set-up Time, $\overline{CLKENAB}$ to CLKAB | | 2.1 | — | 2.1 | — | ns |
| tSU | Set-up Time, $\overline{CLKENBA}$ to CLKBA | | 2.1 | — | 2.1 | — | ns |
| tH | Hold Time, HIGH or LOW Ax after LEAB, Bx after LEBA | | 1.8 | — | 1.8 | — | ns |
| tH | Hold Time, $\overline{CLKENAB}$ after CLKAB | | 0.5 | — | 0.5 | — | ns |
| tH | Hold Time, $\overline{CLKENBA}$ after CLKBA | | 0.5 | — | 0.5 | — | ns |
| tw | LEAB or LEBA Pulse Width HIGH | | 3 | — | 3 | — | ns |
| tw | CLKAB or CLKBA Pulse Width HIGH or LOW | | 3 | — | 3 | — | ns |
| tSK(o) | Output Skew[2] | | — | — | — | 500 | ps |

**NOTES:**
1. See test circuits and waveforms. TA = − 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

# TEST CIRCUITS AND WAVEFORMS

## TEST CONDITIONS

| Symbol | $V_{CC}$[(1)] = 3.3V ±0.3V | $V_{CC}$[(1)] = 2.7V | $V_{CC}$[(2)] = 2.5V ±0.2V | Unit |
|--------|------|------|------|------|
| $V_{LOAD}$ | 6 | 6 | 2 x $V_{CC}$ | V |
| $V_{IH}$ | 2.7 | 2.7 | $V_{CC}$ | V |
| $V_T$ | 1.5 | 1.5 | $V_{CC}$ / 2 | V |
| $V_{LZ}$ | 300 | 300 | 150 | mV |
| $V_{HZ}$ | 300 | 300 | 150 | mV |
| $C_L$ | 50 | 50 | 30 | pF |

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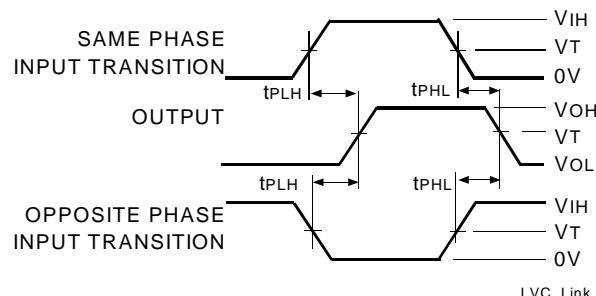
## TEST CIRCUITS FOR ALL OUTPUTS



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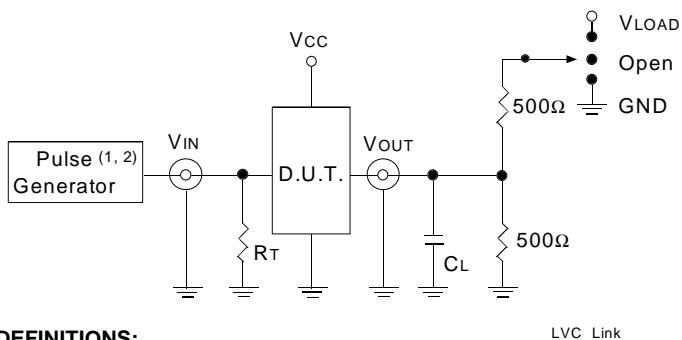
**DEFINITIONS:**
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse
Generator.

**NOTE:**
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2ns; $t_R$ ≤ 2ns.

## SWITCH POSITION

| Test | Switch |
|------|--------|
| Open Drain<br>Disable Low<br>Enable Low | $V_{LOAD}$ |
| Disable High<br>Enable High | GND |
| All Other tests | Open |

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## OUTPUT SKEW - tsk (x)



$$t_{SK(x)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$
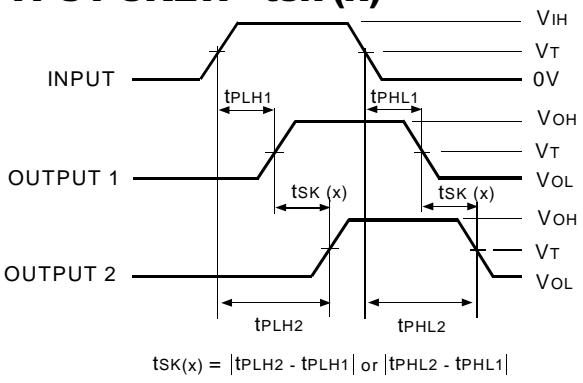
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**NOTES:**
1. For $t_{SK(o)}$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK(b)}$ OUTPUT1 and OUTPUT2 are in the same bank.

## PROPAGATION DELAY



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## ENABLE AND DISABLE TIMES



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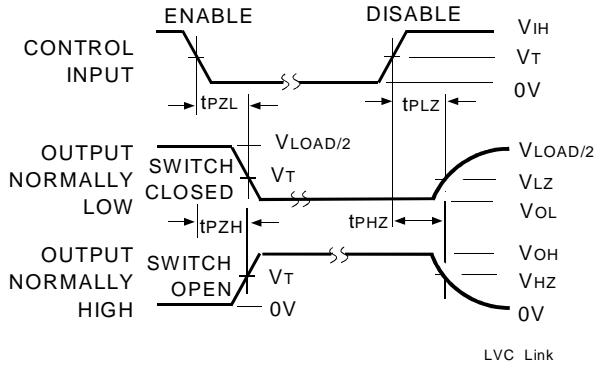
**NOTE:**
1. Diagram shown for input Control Enable-LOW and input Control
Disable-HIGH.

## SET-UP, HOLD, AND RELEASE TIMES
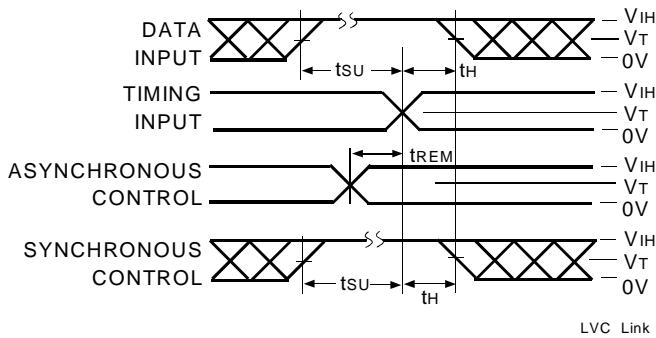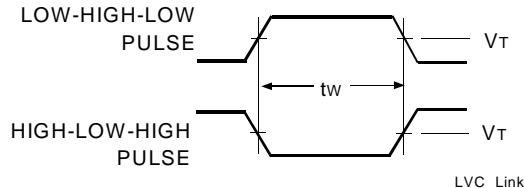


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## PULSE WIDTH



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## ORDERING INFORMATION
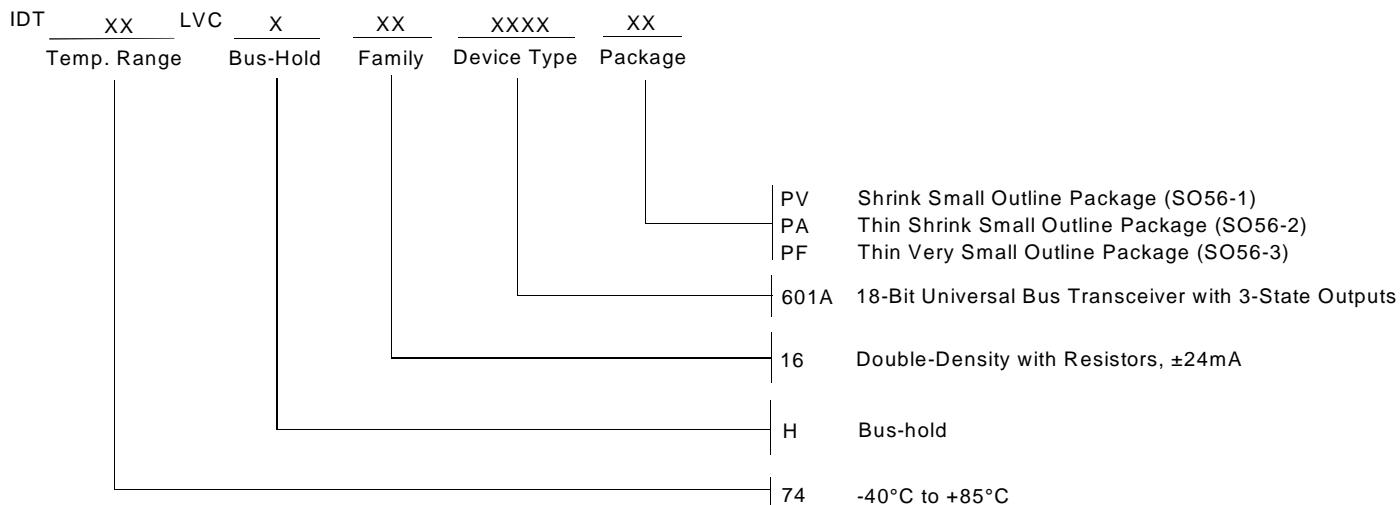
IDT <u>  XX  </u> LVC <u> X </u> <u> XX </u> <u> XXXX </u> <u> XX </u>
    Temp. Range   Bus-Hold  Family  Device Type  Package

| | |
|---|---|
| PV | Shrink Small Outline Package (SO56-1) |
| PA | Thin Shrink Small Outline Package (SO56-2) |
| PF | Thin Very Small Outline Package (SO56-3) |
| 601A | 18-Bit Universal Bus Transceiver with 3-State Outputs |
| 16 | Double-Density with Resistors, ±24mA |
| H | Bus-hold |
| 74 | -40°C to +85°C |

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