LTC1875

15µA Quiescent Current 1.5A Monolithic Synchronous Step-Down Regulator

October 2001

FEATURES

- **High Efficiency: Up to 95%**
- **Low Quiescent Current: Only 15µA with No Load**
- **550kHz Constant Frequency Operation**
- **2.65V to 6V Input Voltage Range**
- **V_{OUT} from 0.8V to V_{IN}, I_{OUT} to 1.5A**
- **True PLL Frequency Locking from 350kHz to 750kHz**
- **Power Good Output Voltage Monitor**
- **Low Dropout Operation: 100% Duty Cycle**
- Burst Mode® or Pulse Skipping Operation
- Current Mode Operation for Excellent Line and Load Transient Response
- Shutdown Mode Draws <1µA Supply Current
- ±2% Output Voltage Accuracy
- Overcurrent and Overtemperature Protected
- Available in 16-Lead SSOP Package

APPLICATIONS

- Cellular Telephones
- Portable Instruments
- Wireless Modems

DESCRIPTION

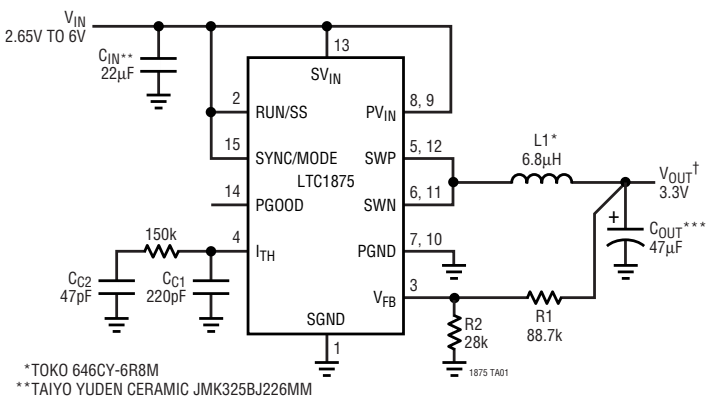
The LTC®1875 is a high efficiency monolithic synchronous buck regulator using a constant frequency, current mode architecture. Operating supply current is only 15µA with no load and drops to <1µA in shutdown. The input supply voltage range of 2.65V to 6V makes the LTC1875 ideally suited for single Li-Ion battery-powered applications. 100% duty cycle provides low dropout operation, extending battery life in portable systems.

Switching frequency is internally set to 550kHz, allowing the use of small surface mount inductors and capacitors. For noise sensitive applications, the LTC1875 can be externally synchronized from 350kHz to 750kHz. Burst Mode operation is inhibited during synchronization or when the SYNC/MODE pin is pulled low.

The internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. Low output voltages are easily supported with a 0.8V feedback reference voltage. The LTC1875 comes in a 16-lead SSOP package.

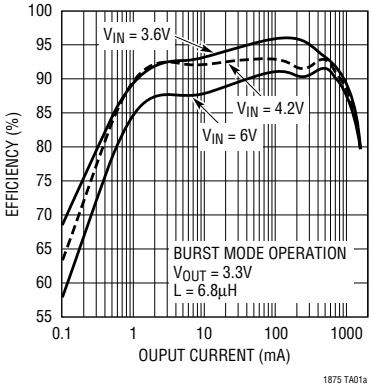
TYPICAL APPLICATION

High Efficiency Step-Down Converter



*TOKO 646CY-6R8M
**TAIYO YUDEN CERAMIC JMK325BJ226MM
***SANYO POSCAP 6TPA47M
†V_{OUT} CONNECTED TO V_{IN} FOR 2.65V < V_{IN} < 3.3V

Efficiency vs Output Load Current

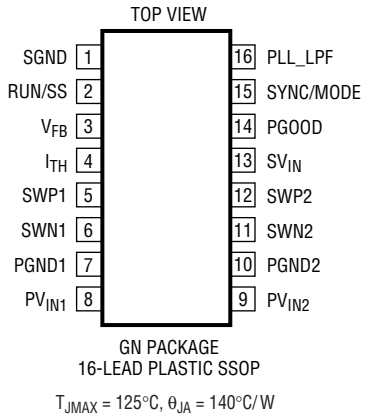


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage ..... –0.3V to 7V
I_{TH}, PLL_LPF Voltages ..... –0.3V to 2.7V
RUN/SS, V_{FB} Voltages ..... –0.3V to V_{IN}
SYNC/MODE Voltage ..... –0.3V to V_{IN}
(V_{PVIN} – V_{SWP}) Voltage ..... –0.3V to 7V
V_{SWN} Voltage ..... –0.3V to 7V
P-Channel Switch Source Current (DC) 2A
N-Channel Switch Sink Current (DC) 2A
Peak Switching Sink and Source Current 3A
Operating Ambient Temperature Range
(Note 2) ..... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 140°C/W

ORDER PART NUMBER
LTC1875EGN
GN PART MARKING
1875

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{VFB}	Feedback Current	(Note 4)	●		8	60	nA
V_{FB}	Regulated Output Voltage	(Note 4) 0°C ≤ T_A ≤ 85°C (Note 4) –40°C ≤ T_A ≤ 85°C	 ●	0.784 0.740	0.80 0.80	0.816 0.840	V V
ΔV_{OVL}	Output Overvoltage Lockout	$\Delta V_{OVL} = V_{OVL} - V_{FB}$	●	20	60	110	mV
ΔV_{UVL}	Output Undervoltage	$\Delta V_{UVL} = V_{FB} - V_{UVL}$	●	20	60	110	mV
$\Delta V_{FB}/V_{FB}$	Reference Voltage Line Regulation	V_{IN} = 2.65V to 6V (Note 4)			0.05	0.25	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	Measured in Servo Loop, V_{ITH} = 0.9V to 1.2V Measured in Servo Loop, V_{ITH} = 1.6V to 1.2V	● ●		0.1 –0.1	0.6 –0.6	% %
V_{IN}	Input Voltage Range		●	2.65		6	V
I_Q	Input DC Bias Current Pulse Skipping Mode Burst Mode Operation Shutdown	(Note 5) 2.65V < V_{IN} < 6V, $V_{SYNC/MODE}$ = 0V, I_{OUT} = 0A $V_{SYNC/MODE}$ = V_{IN}, I_{OUT} = 0A V_{RUN} = 0V, V_{IN} = 6V			 270 15 0	 365 22 1	 µA µA µA
f_{SYNC}	SYNC Capture Range			350		750	kHz
f_{OSC}	Oscillator Frequency	V_{FB} = 0.8V V_{FB} = 0V		495	550 80	605	kHz kHz
I_{PLLLPF}	Phase Detector Output Current Sinking Capability Sourcing Capability	 $f_{PLLIN} < f_{OSC}$ $f_{PPLIN} > f_{SOC}$	 ● ●	 3 –3	 10 –10	 20 –20	 µA µA
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW} = 100mA, V_{IN} = 5V			0.28	0.35	Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW} = –100mA, V_{IN} = 5V			0.35	0.4	Ω
I_{PK}	Peak Inductor Current	V_{FB} = 0.7V, Duty Cycle < 35%, V_{IN} = 3V		1.6	2.0	2.5	A
I_{LSW}	SW Leakage	V_{RUN} = 0V, V_{SW} = 0V or 6V, V_{IN} = 6V			±0.01	±2.5	µA
$V_{SYNC/MODE}$	SYNC/MODE Threshold		●	0.2	1.0	1.5	V
$I_{SYNC/MODE}$	SYNC/MODE Leakage Current				±0.01	±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RUN}	RUN Threshold	V_{RUN} Ramping Up	●	0.2	0.7	1.5	V
I_{RUN}	RUN Input Current	V_{RUN} = 0V			±0.01	±1	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1875E is guaranteed to meet specified performance from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

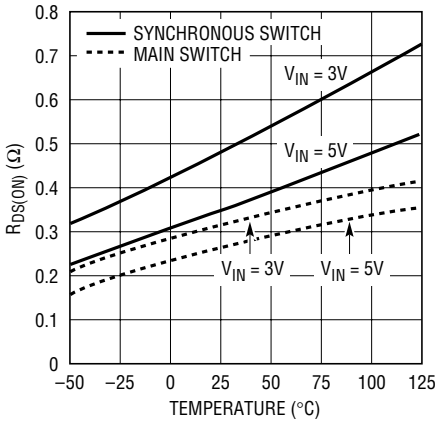
LTC1875: $T_J = T_A + (P_D \times 140°C/W)$

Note 4: The LTC1875 is tested in a feedback loop which servos V_{FB} to the balance point for the error amplifier (V_{ITH} = 1.2V)

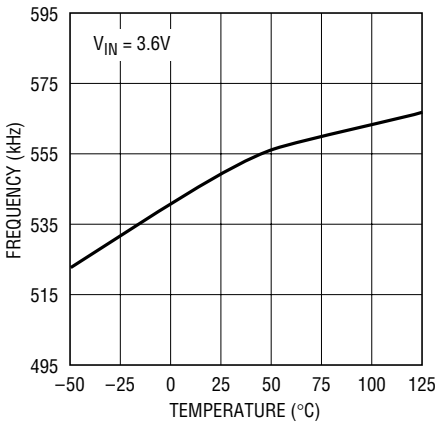
Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

TYPICAL PERFORMANCE CHARACTERISTICS

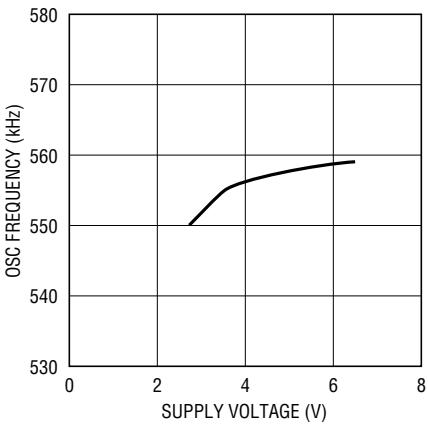
$R_{DS(ON)}$ vs Temperature



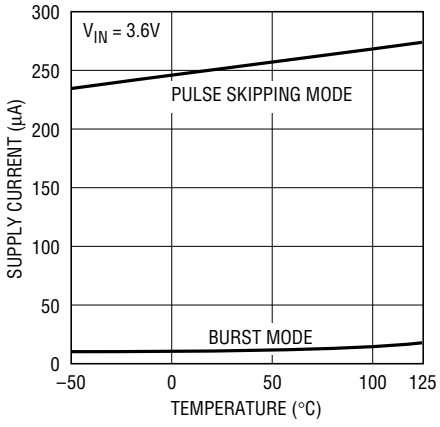
Oscillator Frequency vs Temperature



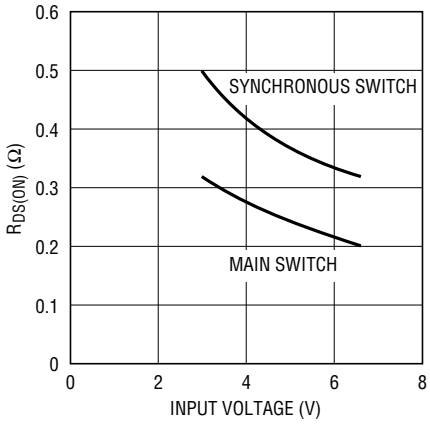
Oscillator Frequency vs Supply Voltage



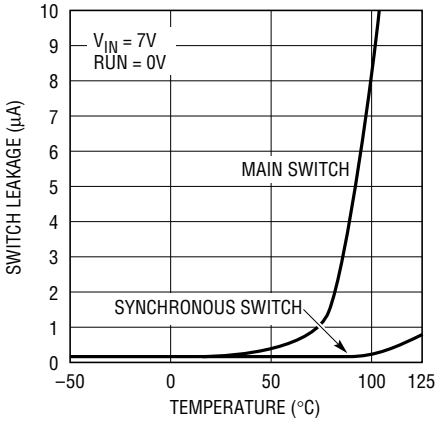
DC Supply Current vs Temperature



$R_{DS(ON)}$ vs Input Voltage

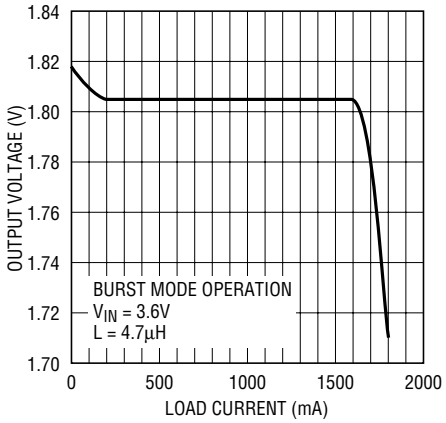


Switch Leakage Current vs Temperature

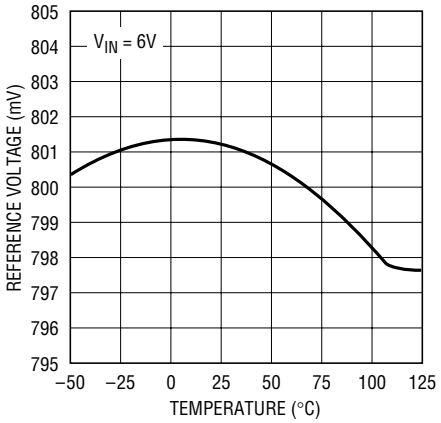


TYPICAL PERFORMANCE CHARACTERISTICS

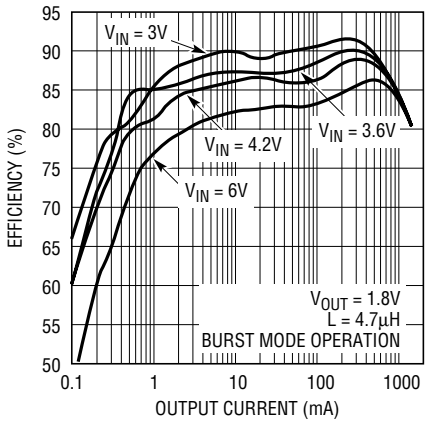
Output Voltage vs Load Current



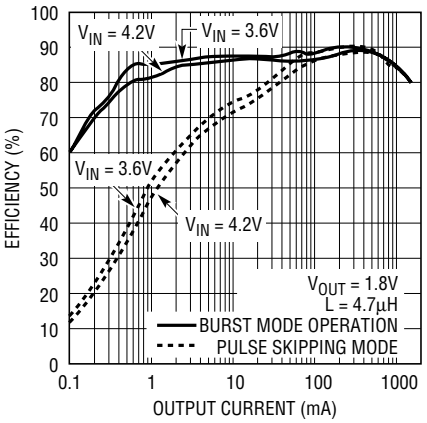
Reference Voltage vs Temperature



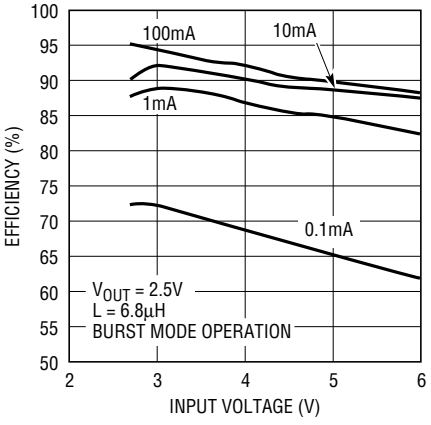
Efficiency vs Output Current



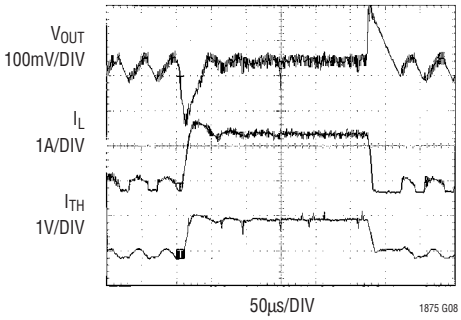
Efficiency vs Output Current



Efficiency vs Input Voltage



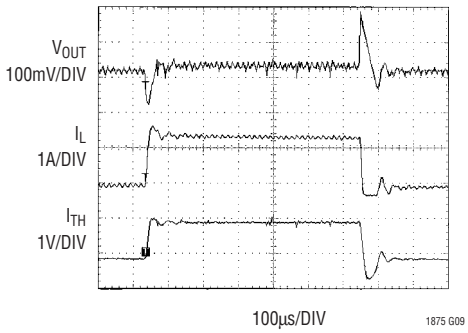
Load Step (Burst Mode Operation)



VIN = 3.6V CIN = 22µF
VOUT = 1.5V COUT = 47µF
L = 6.8µH ILOAD = 200mA to 1700mA

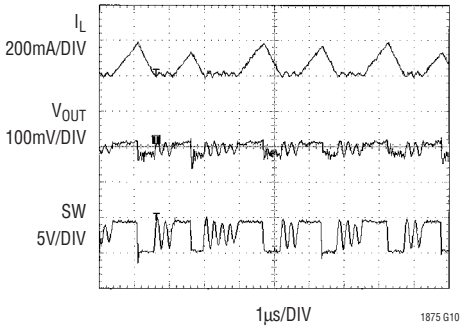
TYPICAL PERFORMANCE CHARACTERISTICS

Load Step Response (Pulse Skipping Mode)



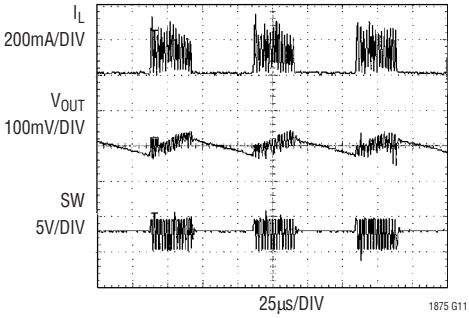
V_{IN} = 3.6V C_{IN} = 22µF
V_{OUT} = 1.5V C_{OUT} = 47µF
L = 6.8µH I_{LOAD} = 200mA to 1700mA

Pulse Skipping Mode Operation



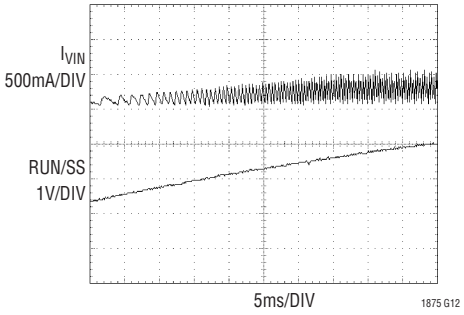
V_{IN} = 4.2V C_{IN} = 22µF
V_{OUT} = 2.5V C_{OUT} = 47µF
L = 6.8µH I_{LOAD} = 50mA

Burst Mode Operation



V_{IN} = 4.2V C_{IN} = 22µF
V_{OUT} = 2.5V C_{OUT} = 47µF
L = 6.8µH I_{LOAD} = 50mA

Soft-Start with Shorted Output



V_{IN} = 3.6V C_{IN} = 22µF
V_{OUT} = 0V C_{OUT} = 47µF
L = 6.8µH I_{LOAD} = 0A

PIN FUNCTIONS

SGND (Pin 1): Signal Ground Pin.

RUN/SS (Pin 2): Combination of Soft-Start and Run Control Inputs. Forcing this pin below 0.4V shuts down the device. In shutdown all functions are disabled and device draws zero supply current. For the proper operation of the part, force this pin above 2.5V. Do not leave this pin floating. Soft-start can be accomplished by raising the voltage on this pin gradually with an RC circuit.

V_{FB} (Pin 3): Feedback Pin. Receives the feedback voltage from an external resistor divider across the output.

I_{TH} (Pin 4): Error Amplifier Compensation Point. The current output increases with this control voltage. Nominal voltage range for this pin is 0.5V to 1.8V.

SWP1, SWP2 (Pins 5, 12): Upper Switch Nodes. These pins connect to the drains of the internal main PMOS switches and should always be connected together externally.

SWN1, SWN2 (Pins 6, 11): Lower Switch Nodes. These pins connect to the drains of the internal synchronous NMOS switches and should always be connected together externally.

PGND1, PGND2 (Pins 7, 10): Power Ground Pins. Ground pins for the internal drivers and switches. These pins should always be tied together.

PV_{IN1}, PV_{IN2} (Pins 8, 9): Power Supply Pins for the Internal Drivers and Switches. These pins should always be tied together.

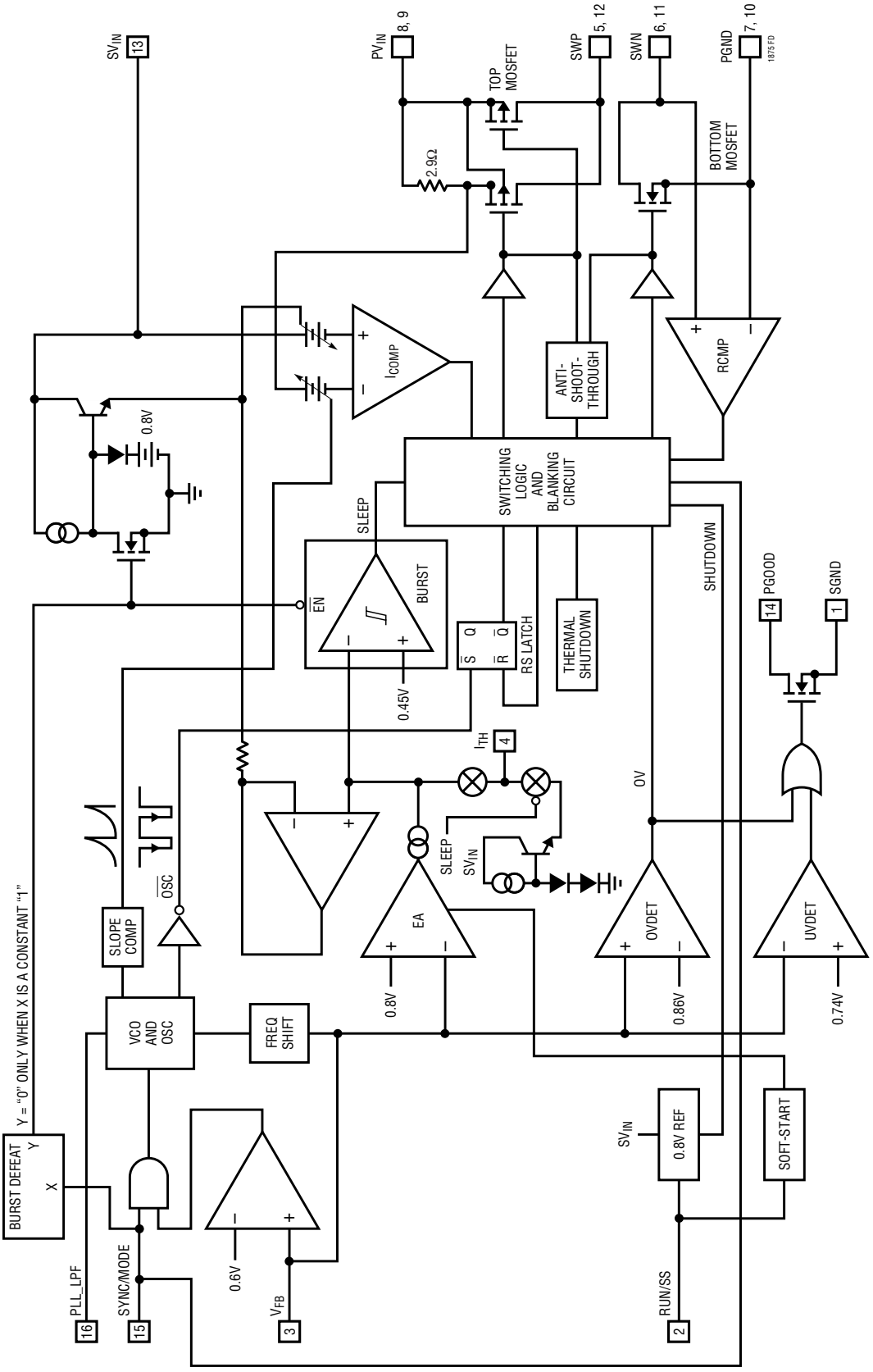
SV_{IN} (Pin 13): Signal Power Supply Pin.

PGOOD (Pin 14): Power Good Indicator Pin. Power good is an open-drain logic output. The PGOOD pin is pulled to ground when the voltage on the V_{FB} pin is not within ±7.5% of its nominally regulated potential. This pin requires a pull-up resistor for power good indication. Power good indication works in all modes of operation.

SYNC/MODE (Pin 15): External Clock Synchronization and Mode Select Input. To synchronize, apply an external clock with a frequency between 350kHz and 750kHz. To select Burst Mode operation, tie pin to SV_{IN}. Grounding this pin selects pulse skipping mode. Do not leave this pin floating.

PLL_LPF (Pin 16): Output of the Phase Detector and Control Input of Oscillator. Connect a series RC lowpass network from this pin to ground if externally synchronized. If unused, this pin may be left open.

BLOCK DIAGRAM



OPERATION (Refer to Block Diagram)

Main Control Loop

The LTC1875 uses a constant frequency, current mode step-down architecture. Both the top MOSFET and synchronous bottom MOSFET switches are internal. During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, I_{COMP}, resets the RS latch. The peak inductor current at which I_{COMP} turns the top MOSFET off is controlled by the voltage on the I_{TH} pin, which is the output of error amplifier EA. When the load current increases, it causes a slight decrease in the feedback voltage, V_{FB}, relative to the 0.8V internal reference, which, in turn, causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse direction or the next clock cycle begins.

Comparator OVDET guards against transient overshoots >7.5% by turning the main switch off and keeping it off until the fault is removed.

Burst Mode Operation

The LTC1875 is capable of Burst Mode operation in which the internal power MOSFETs operate intermittently based on load demand. To enable Burst Mode operation, simply tie the SYNC/MODE pin to SV_{IN} or connect it to a logic high ($V_{SYNC/MODE}$ > 1.5V). To disable Burst Mode operation and enable PWM pulse skipping mode, connect the SYNC/MODE pin to SGND. In this mode, the efficiency is lower at light loads but becomes comparable to Burst Mode operation when the output load exceeds 100mA. The advantage of pulse skipping mode is lower output ripple.

When the converter is in Burst Mode operation, the peak current of the inductor is set to approximately 400mA, even though the voltage at the I_{TH} pin indicates a lower value. The voltage at the I_{TH} pin drops when the inductor's average current is greater than the load requirement. As the I_{TH} voltage drops below approximately 0.45V, the BURST comparator trips, turning off both power MOSFETs. The I_{TH} pin is then disconnected from the output of the EA amplifier and held 0.65V above ground.

In sleep mode, both power MOSFETs are held off and the internal circuitry is partially turned off, reducing the quiescent current to 15μA. The load current is now being supplied from the output capacitor. When the output voltage drops, the I_{TH} pin reconnects to the output of the EA amplifier and the top MOSFET is again turned on and this process repeats.

Soft-Start/Run Function

The RUN/SS pin provides a soft-start function and a means to shut down the LTC1875. Soft-start reduces the input current surge by gradually increasing the regulator's maximum output current. This pin can also be used for power supply sequencing.

Pulling the RUN/SS pin below 0.4V shuts down the LTC1875, which then draws <1μA current from the supply. This pin can be driven directly from logic circuits as shown in Figure 1. It is recommended that this pin is driven to V_{IN} during normal operation. Note that there is no current flowing out of this pin. Soft-start action is accomplished by connecting an external RC network to the RUN/SS pin as shown in Figure 1. The LTC1875 actively pulls the RUN/SS pin to ground under low input supply voltage conditions.

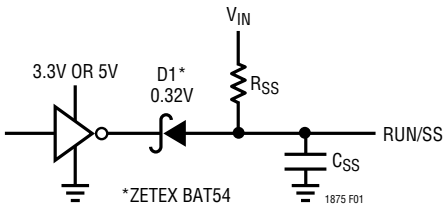


Figure 1. RUN/SS Pin Interfacing

OPERATION (Refer to Block Diagram)

Power Good Indicator

The power good function monitors the output voltage in all modes of operation. Its open-drain output is pulled low when the output voltage is not within ±7.5% of its nominally regulated voltage. The feedback voltage is filtered before it is fed to a power good window comparator in order to prevent false tripping of the power good signal during fast transients. The window comparator monitors the output voltage even in Burst Mode operation. In shutdown mode, open drain is actively pulled low to indicate that the output voltage is invalid.

Short-Circuit Protection

When the output is shorted to ground, the frequency of the oscillator is reduced to about 80kHz, 1/7 the nominal frequency. This frequency foldback ensures that the inductor current has more time to decay, thereby preventing runaway. The oscillator's frequency will progressively increase to 550kHz (or to the synchronized frequency) when V_{FB} rises above 0.3V.

Frequency Synchronization

The LTC1875 can be synchronized to an external clock source connected to the SYNC/MODE pin. The turn-on of the top MOSFET is synchronized to the rising edge of the external clock.

When the LTC1875 is clocked by an external source, Burst Mode operation is disabled. In this synchronized mode, when the output load current is very low, current comparator, I_{COMP}, may remain tripped for several cycles and force the main switch to stay off for the same number of cycles. Increasing the output load slightly allows constant frequency PWM operation to resume.

Frequency synchronization is inhibited when the feedback voltage V_{FB} is below 0.6V. This prevents the external clock from interfering with the frequency foldback for short-circuit protection.

Low Dropout Operation

When the input supply voltage decreases toward the output voltage in a buck regulator, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the top MOSFET and the inductor.

Low Supply Operation

The LTC1875 is designed to operate down to an input supply voltage of 2.65V although the maximum allowable output current is reduced at this low voltage. Figure 2 shows the reduction in the maximum output current as a function of input voltage.

Another important detail to remember is that at low input supply voltages, the $R_{DS(ON)}$ of the P-channel switch increases. Therefore, the user should calculate the power dissipation when the LTC1875 is used at 100% duty cycle with low supply voltage (see Thermal Considerations in the Applications Information section).

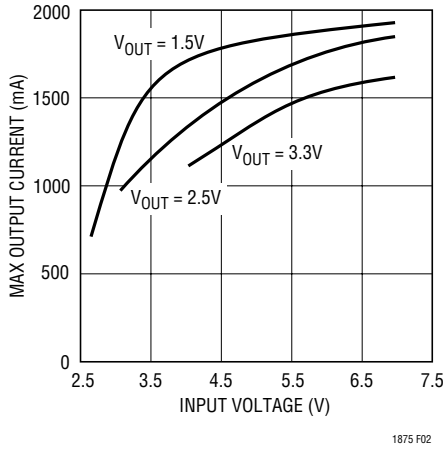


Figure 2. Maximum Output Current vs Input Voltage

OPERATION

Slope Compensation and Inductor Peak Current

Slope compensation is required in order to prevent subharmonic oscillation at high duty cycles. It is accomplished by internally adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. As a result, the maximum inductor peak current is reduced for duty cycles >40%. This is shown in the decrease of the inductor peak current as a function of duty cycle graph in Figure 3.

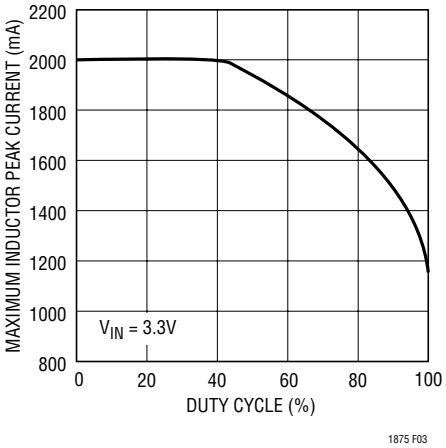


Figure 3. Maximum Inductor Peak Current vs Duty Cycle

APPLICATIONS INFORMATION

The basic LTC1875 application circuit is shown on the first page of this data sheet. External component selection is driven by the load requirement and begins with the selection of L followed by C_{IN} and C_{OUT}.

Inductor Value Calculation

The inductor selection will depend on the operating frequency of the LTC1875. The internal nominal frequency is 550kHz, but can be externally synchronized from 350kHz to 750kHz.

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. However, operating at a higher frequency results in lower efficiency because of increased switching losses.

The inductor value has a direct effect on ripple current. The ripple current ΔI_L decreases with higher inductance or frequency and increases with higher input voltages.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

Accepting larger values of ΔI_L allows the use of smaller inductors, but results in higher output voltage ripple. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$.

The inductor value also has an effect on Burst Mode operation. The transition to low current operation begins when the inductor current peaks fall to approximately 500mA. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Selection

The inductor should have a saturation current rating greater than the peak inductor current set by the current comparator of LTC1875. Also, consideration should be given to the resistance of the inductor. Inductor conduction losses are directly proportional to the DC resistance of the inductor. Manufacturers sometimes provide maximum current ratings based on the allowable losses in the inductor.

Suitable inductors are available from Coilcraft, Coiltronics, Dale, Sumida, Toko, Murata, Panasonic and other manufacturers.

APPLICATIONS INFORMATION

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a trapezoidal waveform of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS input capacitor current is given by:

$$I_{RMS(CIN)} \cong I_{OMAX} \frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there are any questions.

Depending on how the LTC1875 circuit is powered up, you may need to check for input voltage transients. Input voltage transients may be caused by input voltage steps or by connecting the circuit to an already powered up source such as a wall adapter. The sudden application of input voltage will cause a large surge of current in the input leads that will store energy in the parasitic inductance of the leads. This energy will cause the input voltage to swing above the DC level of the input power source and it may exceed the maximum voltage rating of the input capacitor and LTC1875.

The easiest way to suppress input voltage transients is to add a small aluminum electrolytic capacitor in parallel with the low ESR input capacitor. The selected capacitor needs to have the right amount of ESR in order to critically dampen the resonant circuit formed by the input lead inductance and the input capacitor. The typical values of ESR will fall in the range of 0.5Ω to 2Ω and capacitance will fall in the range of 5μF to 50μF.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. For the LTC1875, the general rule for proper operation is:

$ESR_{COUT} < 0.125\Omega$

The choice of using a smaller output capacitance increases the output ripple voltage due to the frequency dependent term but can be compensated for by using capacitor(s) of very low ESR to maintain low ripple voltage. The I_{TH} pin compensation components can be optimized to provide stable high performance transient response regardless of the output capacitor selected.

Manufacturers such as Taiyo Yuden, AVX, Kemet and Sanyo should be considered for low ESR, high performance capacitors. The POSCAP solid electrolytic chip capacitor available from Sanyo is an excellent choice for output bulk capacitors due to its low ESR/size ratio. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

Output Voltage Programming

The output voltage is set by a resistor divider according to the following formula:

$$V_{OUT} = 0.8V\left(1 + \frac{R1}{R2}\right) \quad (2)$$

The external resistor divider is connected to the output, allowing remote voltage sensing as shown in Figure 4.

APPLICATIONS INFORMATION

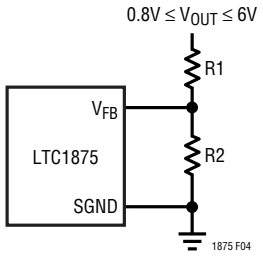


Figure 4. Setting the LTC1875 Output Voltage

Phase-Locked Loop and Frequency Synchronization

The LTC1875 has an internal voltage-controlled oscillator and phase detector comprising a phase-locked loop. This allows the MOSFET turn-on to be locked to the rising edge of an external frequency source. The frequency range of the voltage-controlled oscillator is 350kHz to 750kHz. The phase detector used is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock up on input frequencies close to the harmonics of the VCO center frequency. The PLL hold-in range Δf_H is equal to the capture range, $\Delta f_H = \Delta f_C = \pm 200kHz$.

The output of the phase detector is a pair of complementary current sources charging or discharging the external filter network on the PLL_LPF pin. The relationship between the voltage on the PLL_LPF pin and operating frequency is shown in Figure 5. A simplified block diagram is shown in Figure 6.

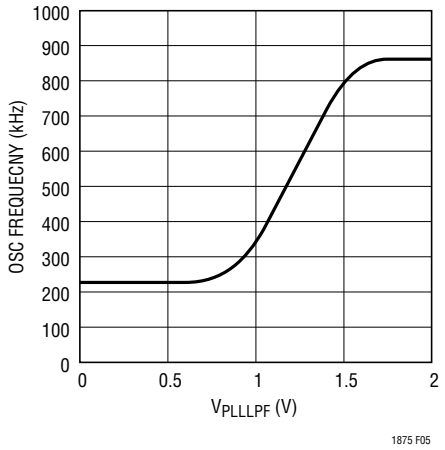


Figure 5. Relationship Between Oscillator Frequency and Voltage at PLL_LPF Pin

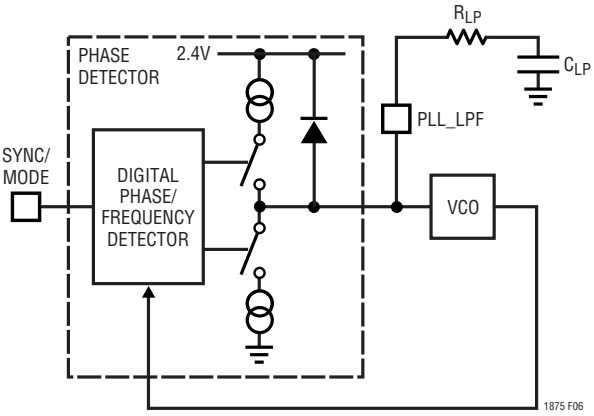


Figure 6. Phase-Locked Loop Block Diagram

If the external frequency ($V_{SYNC/MODE}$) is greater than 550kHz, the center frequency, current is sourced continuously, pulling up the PLL_LPF pin. When the external frequency is less than 550kHz, current is sunk continuously, pulling down the PLL_LPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLL_LPF pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor C_{LP} holds the voltage.

The loop filter components C_{LP} and R_{LP} smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is 2200pF to 0.01µF. When not synchronized to an external clock, the internal connection to the VCO is disconnected. This disallows setting the internal oscillation frequency by a DC voltage on the V_{PLLLPF} pin.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

APPLICATIONS INFORMATION

Where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in LTC1875 circuits: supply quiescent currents and I^2R losses. The supply quiescent current loss dominates the efficiency loss at very low load current whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence as illustrated in Figure 7.

1. The supply quiescent current is due to two components: the DC bias current as given in the Electrical Characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge dQ moves from PV_{IN} to ground. The resulting dQ/dt is the current out of PV_{IN} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to supply voltage and thus their effects will be more pronounced at higher supply voltages.

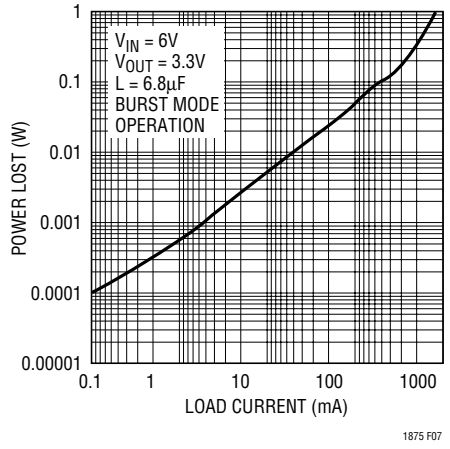


Figure 7. Power Lost vs Load Current

2. I^2R losses are calculated from the resistances of the internal switches R_{SW} and external inductor R_L. In continuous mode the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into SW pins is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(DC) + R_{DS(ON)BOT})(1 - DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

In most applications, the LTC1875 does not dissipate much heat due to its high efficiency. But, in applications where the LTC1875 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW nodes will become high impedance.

To avoid the LTC1875 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. Normally, some iterative calculation is required to determine a reasonably accurate value. The temperature rise is given by:

$$T_R = P \bullet \theta_{JA}$$

where P is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature is given by:

$$T_J = T_A + T_R$$

APPLICATIONS INFORMATION

where T_A is the ambient temperature. Because the power transistor $R_{DS(ON)}$ is a function of temperature, it is usually necessary to iterate 2 to 3 times through the equations to achieve a reasonably accurate value for the junction temperature.

As an example, consider the LTC1875 in dropout at an input voltage of 3V, a load current of 0.8A and an ambient temperature of 70°C. From the typical performance graph of switch resistance, the $R_{DS(ON)}$ of the P-channel switch at 70°C is 0.35Ω. Therefore, power dissipated by the IC is:

$$P = I^2 \bullet R_{DS(ON)} = 0.224W$$

For the SSOP package, the θ_{JA} is 140°C/W. Thus the junction temperature of the regulator is:

$$T_J = 70°C + (0.224)(140) = 101°C$$

However, at this temperature, the $R_{DS(ON)}$ is actually 0.4Ω. Therefore:

$$T_J = 70°C + (0.256)(140) = 106°C$$

which is below the maximum junction temperature of 125°C.

Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$).

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to (ΔI_{LOAD} • ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating a feedback error signal. The regulator loop then acts to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The I_{TH} pin can be used for external compensation as shown in Figure 9. (The capacitor, C_{C2}, is typically needed for noise decoupling.)

A second, more severe transient is caused by switching in loads with large (>1μF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25 • C_{LOAD}). Thus, a 10μF capacitor charging to 3.3V would require a 250μs rise time, limiting the charging current to about 130mA.

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PC Board Layout Checklist

As with all high frequency switchers, when considering layout, care must be taken in order to achieve optimal electrical, thermal and noise performance. Figure 8 is a sample of PC board layout for the design example shown in Figure 9. A 4-layer PC board is used in this design. Several guidelines are followed in this layout:

1. In order to minimize switching noise and improve output load regulation, the PGND pins of the LTC1875 should be connected directly to 1) the negative terminal of the output decoupling capacitors, 2) the negative terminal of the input capacitor and 3) vias to the ground plane immediately adjacent to Pins 1, 7 and 10. The ground trace on the top layer of the PC board should be as wide and short as possible to minimize series resistance and inductance.
2. Beware of ground loops in multiple layer PC boards. Try to maintain one central ground node on the board and use the input capacitor to avoid excess input ripple for high output current power supplies. If the ground is to be used for high DC currents, choose a path away from the small-signal components.
3. The high di/dt loop from the top terminal of the input capacitor, through the power MOSFETs and back to the input capacitor should be kept as tight as possible to reduce inductive ringing. Excess inductance can cause increased stress on the power MOSFET and increase noise on the input. If low ESR ceramic capacitors are used to reduce input noise, place these capacitors close to the DUT in order to keep the series inductance to a minimum.
4. Place the small-signal components away from high frequency switching nodes. In the layout shown in Figure 8, all of the small-signal components have been placed on one side of the IC and all of the power components have been placed on the other.
5. For optimum load regulation and true sensing, the top of the output resistor divider should connect independently to the top of the output capacitor (Kelvin connection), staying away from any high dV/dt traces. Place the divider resistors near the LTC1875 in order to keep the high impedance FB node short.

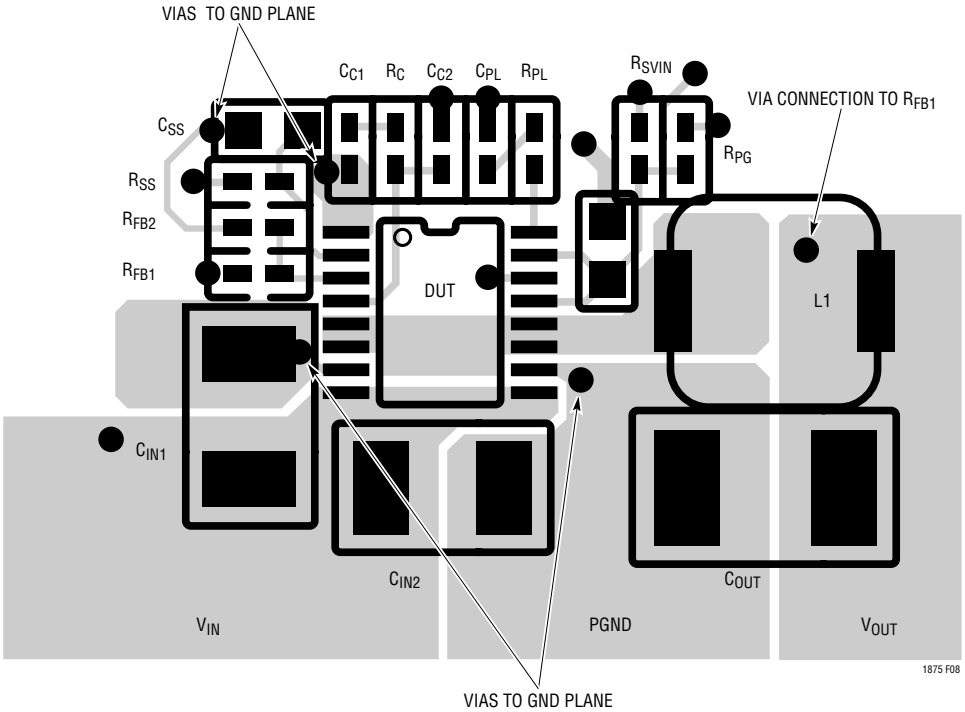


Figure 8. Typical Application and Suggested Layout (Topside Only)

APPLICATIONS INFORMATION

Design Example

As a design example, assume the LTC1875 is used in a single lithium-ion battery-powered cellular phone application. The V_{IN} will be operating from a maximum of 4.2V down to about 2.65V. The load current requirement is a maximum of 1.5A but most of the time it will be on standby mode, requiring only 2mA. Efficiency at both low and high load currents is important. Output voltage is 2.5V. With this information we can calculate L using equation (1),

$$L = \frac{1}{(f)(\Delta I_L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Substituting V_{OUT} = 2.5V, V_{IN} = 4.2V, ΔI_L = 450mA and f = 550kHz in equation (3) gives:

$$L = \frac{2.5V}{550kHz \bullet 450mA}\left(1 - \frac{2.5V}{4.2V}\right) = 4.09\mu H$$

A 4.7µH inductor works well for this application. For good efficiency choose a 2A inductor with less than 0.125Ω series resistance.

C_{IN} will require an RMS current rating of at least 0.75A at temperature and C_{OUT} will require an ESR of less than 0.125Ω. In most applications, the requirements for these capacitors are fairly similar.

For the feedback resistors, choose R2 = 412k. R1 can then be calculated from equation (2) to be:

$$R1 = \left(\frac{V_{OUT}}{0.8} - 1\right) \bullet R2 = 875.5k, \text{ use } 887k$$

Figure 9 shows the complete circuit along with its efficiency curve.

APPLICATIONS INFORMATION

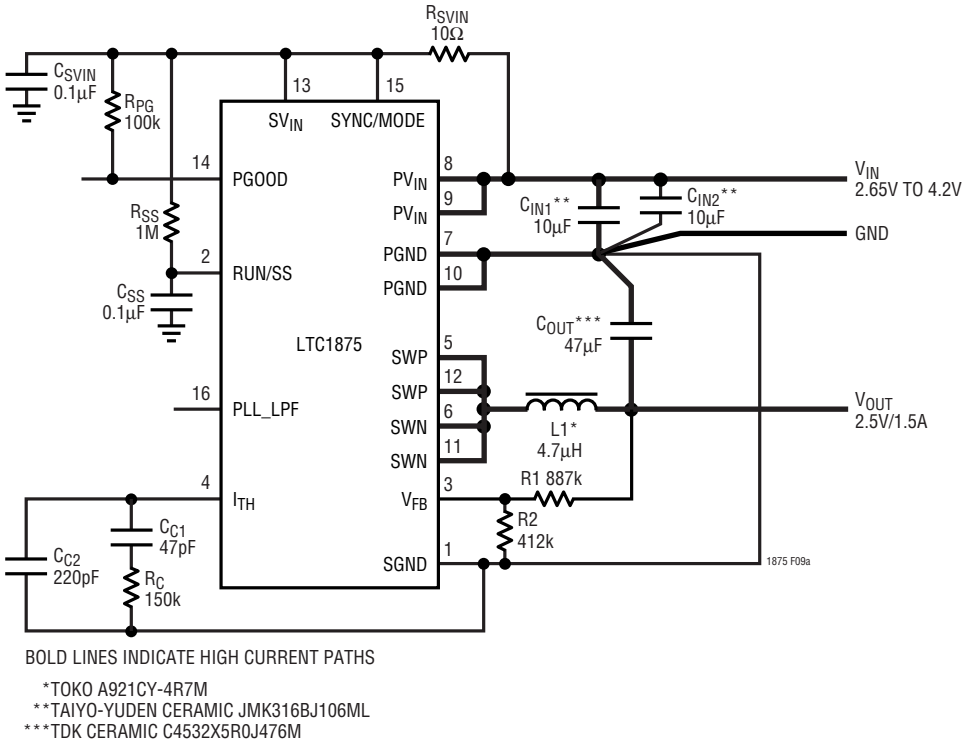


Figure 9a. Single Lithium-Ion to 2.5V/1.5A Regulator from Design Example

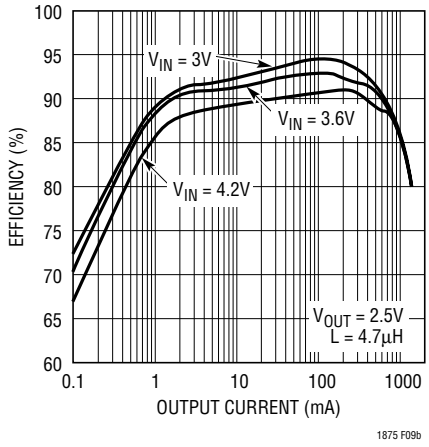
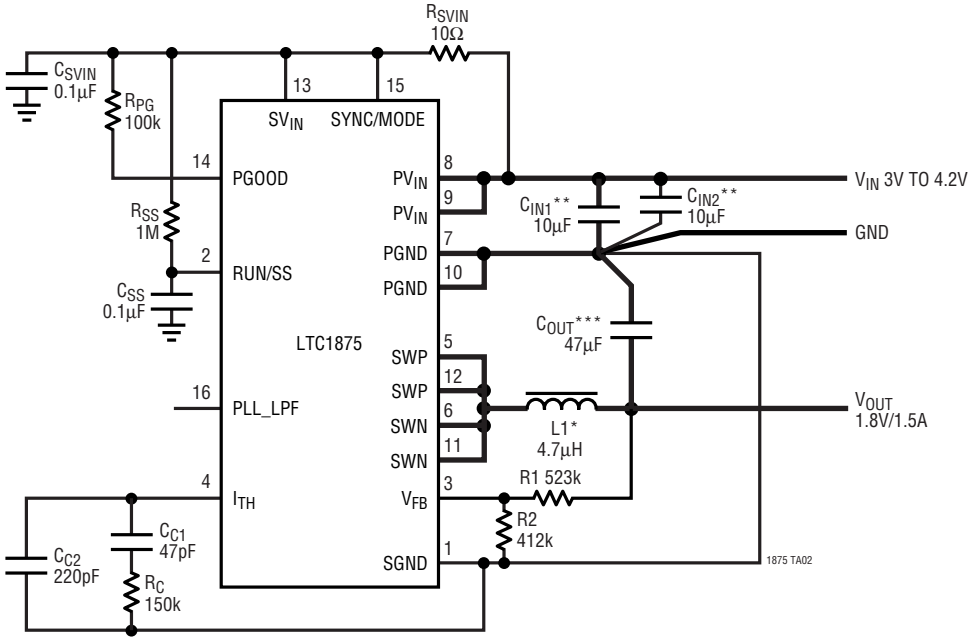


Figure 9b. Efficiency vs Output Current for Design Example

TYPICAL APPLICATION

Single Li-Ion to 1.8V/1.5A Regulator Using All Ceramic Capacitors

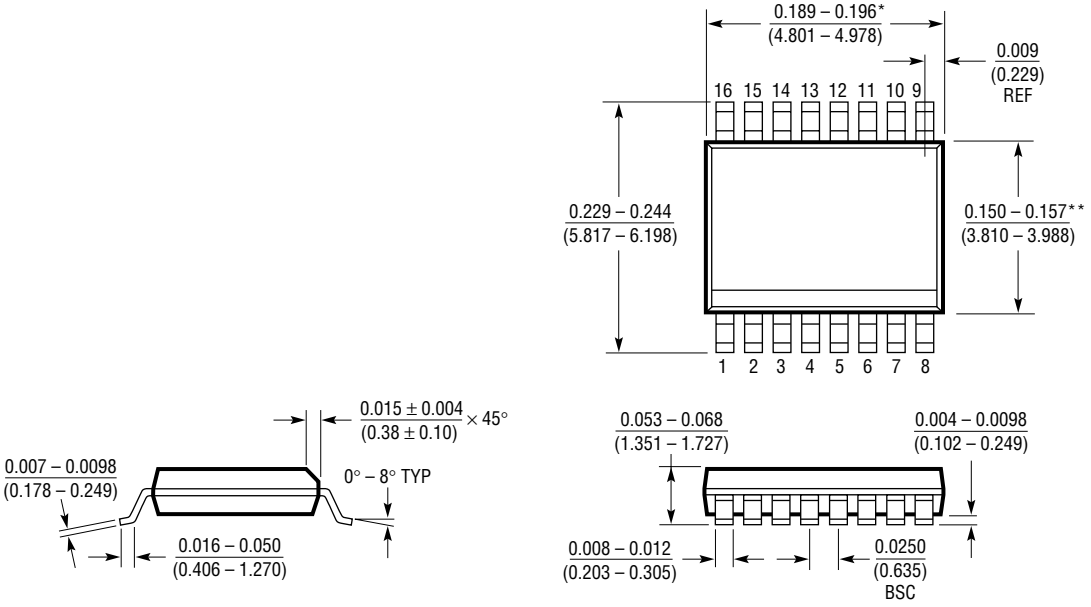


BOLD LINES INDICATE HIGH CURRENT PATHS

*TOKO A921CY-4R7M
**TAIYO YUDEN CERAMIC JMK316BJ106ML
***TDK CERAMIC C4532X5R0J476M

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



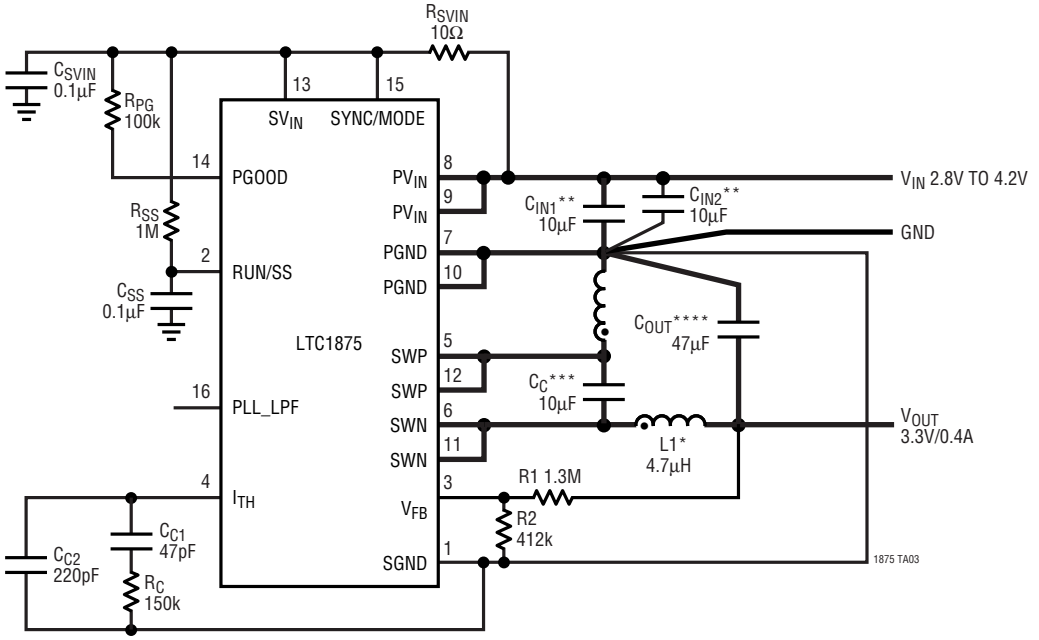
* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1098

TYPICAL APPLICATION

Single Li-Ion to 3.3V/0.4A (ZETA) Regulator Using All Ceramic Capacitors



BOLD LINES INDICATE HIGH CURRENT PATHS

*COILTRONICS CTX5-4
**TAIYO YUDEN CERAMIC JMK316BJ106ML
***TAIYO YUDEN CERAMIC LMK325BJ106MN
****TDK CERAMIC C4532X5R0J476M

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1265	1.2A, High Efficiency Step-Down DC/DC Converter	Constant Off-Time, Monolithic, Burst Mode Operation
LTC1474/LTC1475	Low Quiescent Current Step-Down DC/DC Converters	Monolithic, I_{OUT} to 250mA, I_Q = 10µA, 8-Pin MSOP
LTC1504A	Monolithic Synchronous Step-Down Switching Regulator	Low Cost, Voltage Mode I_{OUT} to 500mA, V_{IN} from 4V to 10V
LTC1622	Low Input Voltage Current Mode Step-Down DC/DC Controller	High Frequency, High Efficiency, 8-Pin MSOP
LTC1626	Low Voltage, High Efficiency Step-Down DC/DC Converter	Monolithic, Constant Off-Time, I_{OUT} to 600mA, Low Supply Voltage Range: 2.5V to 6V
LTC1627	Monolithic Synchronous Step-Down Switching Regulator	Constant Frequency, I_{OUT} to 500mA, Secondary Winding Regulation, V_{IN} from 2.65V to 8.5V
LTC1701	Monolithic Current Mode Step-Down Switching Regulator	Constant Off-Time, I_{OUT} to 500mA, 1MHz Operation, V_{IN} from 2.5V to 5.5V
LTC1707	Monolithic Synchronous Step-Down Switching Regulator	1.19V V_{REF} Pin, Constant Frequency, I_{OUT} to 600mA, V_{IN} from 2.65V to 8.5V
LT1767	1.5A, 1.25MHz, Step-Down DC/DC Converter	V_{IN} from 3V to 25V, 8-Lead MSOP Package
LTC1772	Low Input Voltage Current Mode Step-Down DC/DC Controller	550kHz, 6-Pin ThinSOT, I_{OUT} Up to 5A, V_{IN} from 2.2V to 10V
LTC1877	High Efficiency Monolithic Step-Down Regulator	550kHz, MS8, V_{IN} Up to 10V, I_Q = 10µA, I_{OUT} to 600mA at V_{IN} = 5V
LTC1878	High Efficiency Monolithic Step-Down Regulator	550kHz, MS8, V_{IN} Up to 6V, I_Q = 10µA, I_{OUT} to 600mA at V_{IN} = 3.3V
LTC3404	1.4MHz High Efficiency Monolithic Synchronous Step-Down Regulator	0.8V_{REF} Pin, I_{OUT} to 600mA at V_{IN} = 3.3V, I_Q = 10µA
LTC3405	1.5MHz, 300mA Synchronous Step-Down Regulator	V_{IN} to 6V, IQ = 20µA, ThinSOT™

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