SINGLE CHIP 10/100 FAST ETHERNET CONTROLLER WITH uP INTERFACE

1.0 Features

- Direct interface to 80188/186 up to 40Mhz.
- Integrated 10/100 TP tranceiver on chip to reduce overall cost
- Optional MII interface for external tranceiver.
- Fully comply to IEEE 802.3u spec.
- Best fit in network printer and hub/switch management application
- A local DMA channel between on-chip FIFOs and packet memory
- Shared memory architecture allow host and MX98726EC to use only one single SRAM
- Host DMA can share packet memory with local DMA with simple hand shake protocol for x188/186 type of processor
- Supports proprietary local DMA channel to share packet memory
- Support bus size configuration:
  - CPU : 8 bits, SRAM: 8 bits
  - CPU : 16 bits, SRAM: 8/16 bits
- Flexible packet buffer partition and addressing space for 32k, 64k up to 512K bytes
- NWAY autonegotiation function to automatically set up network speed and protocol
- 3 loop back modes for system level diagnostics
- Rich on-chip register set to support a wide variety of network management functions
- Support 64 bits hash table for multicast addressing
- Support software EEPROM interface for easy upgrade of EEPROM content
- Support 1K bits and 4K bits EEPROM interface
- 5V CMOS in 128 PQFP package for minimum board size application

1.1 Introduction

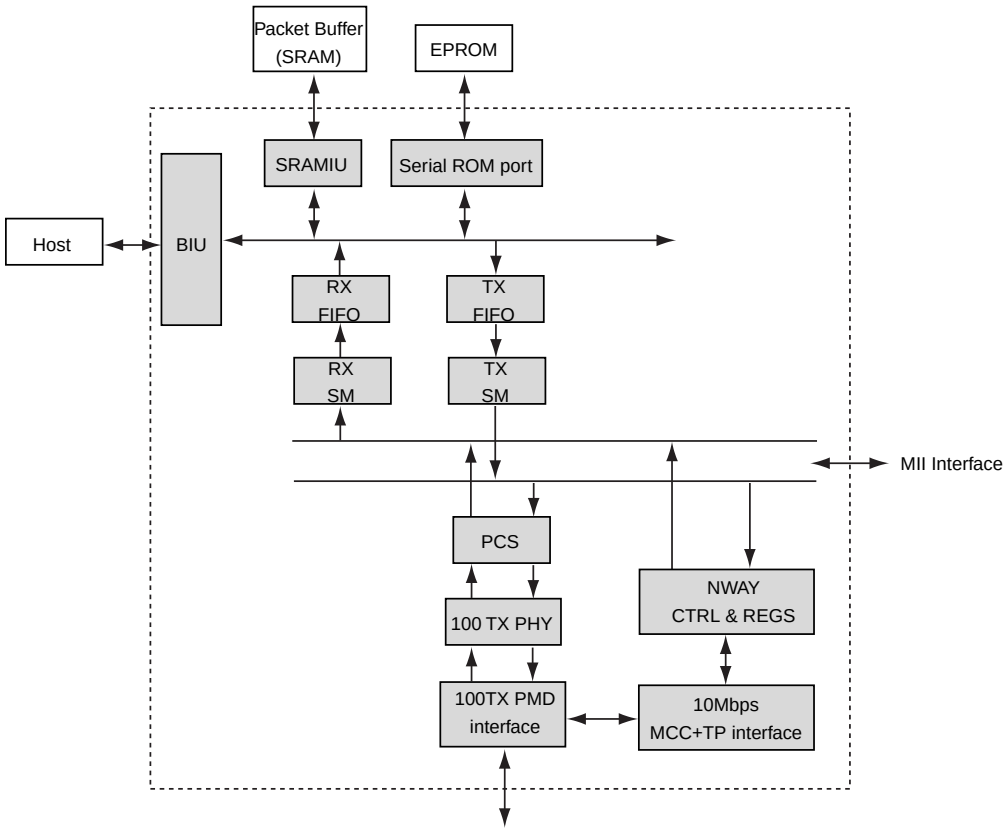
MX98726EC (Generic MAC , or GMAC) is a cost effective solution as a generic single chip 10/100 Fast Ethernet controller. It is designed to directly interface 80188, 80186 (host) without glue logic. Two types of memory sharing schemes are supported, i.e. interleaved and shared mode to support a variety of applications. Single chip solution will help reduce system cost not only on the components but also the board size. Full NWAY function with 10/100 tranceiver will ease the field installation, simply plug the chip in and it will connect itself with the best protocol available.

The interleaved mode allow uP to access SRAM (packet/host buffer) through MX98726EC's local DMA channel. This way, no extra SRAM interface logic is needed on the host side. If high performance is desired, then shared memory mode is another alternative which allow host to access SRAM on its own by denying SRAM bus grant to MX98726EC using simple hand shake protocol. Without SRAM bus grant, MX98726EC will float its interface connected to the SRAM, therefore host can utilize its own memory subsystem to conduct its own SRAM access.

A intelligent built-in SRAM bus arbitor will manage all the SRAM access requests from host, on-chip transmit channel and on-chip receive channel. The throughput of these network channels and MX98726EC's DMA burst length can be easily adjusted by option bits on the chip. These options can help system developers to "fine tune" a best cost/performance ratio.

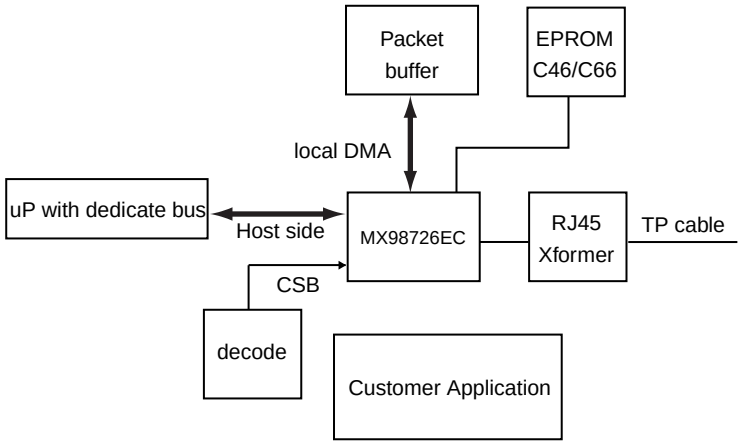
MX98726EC is also equipped with fast back-to-back transmit capability which allow software to "fire" as many transmit packets as needed in a single command. Receive FIFO also allow back-to-back reception. Optional EEPROM can be used to stored network network address and other information. In case cost is really a concern, most configuration options including network address can be programmed through uP.

1.2 Internal Block Diagram

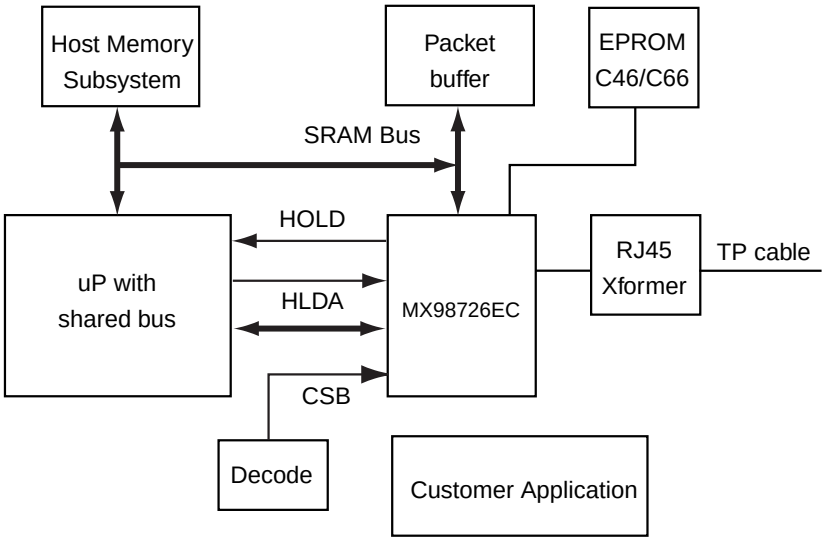


Architecture and Interface overview

1.3 Typical Applications

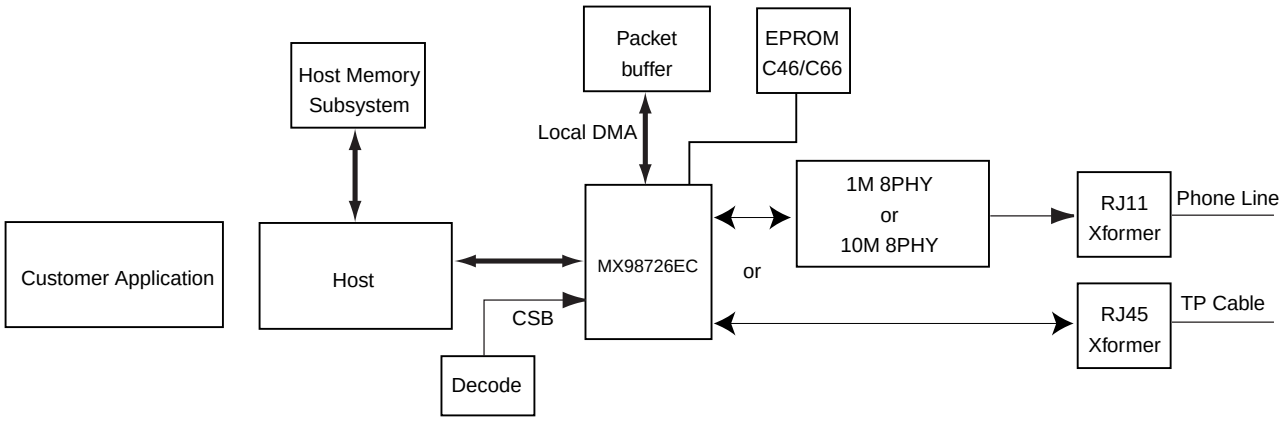


Interleaved memory Architecture



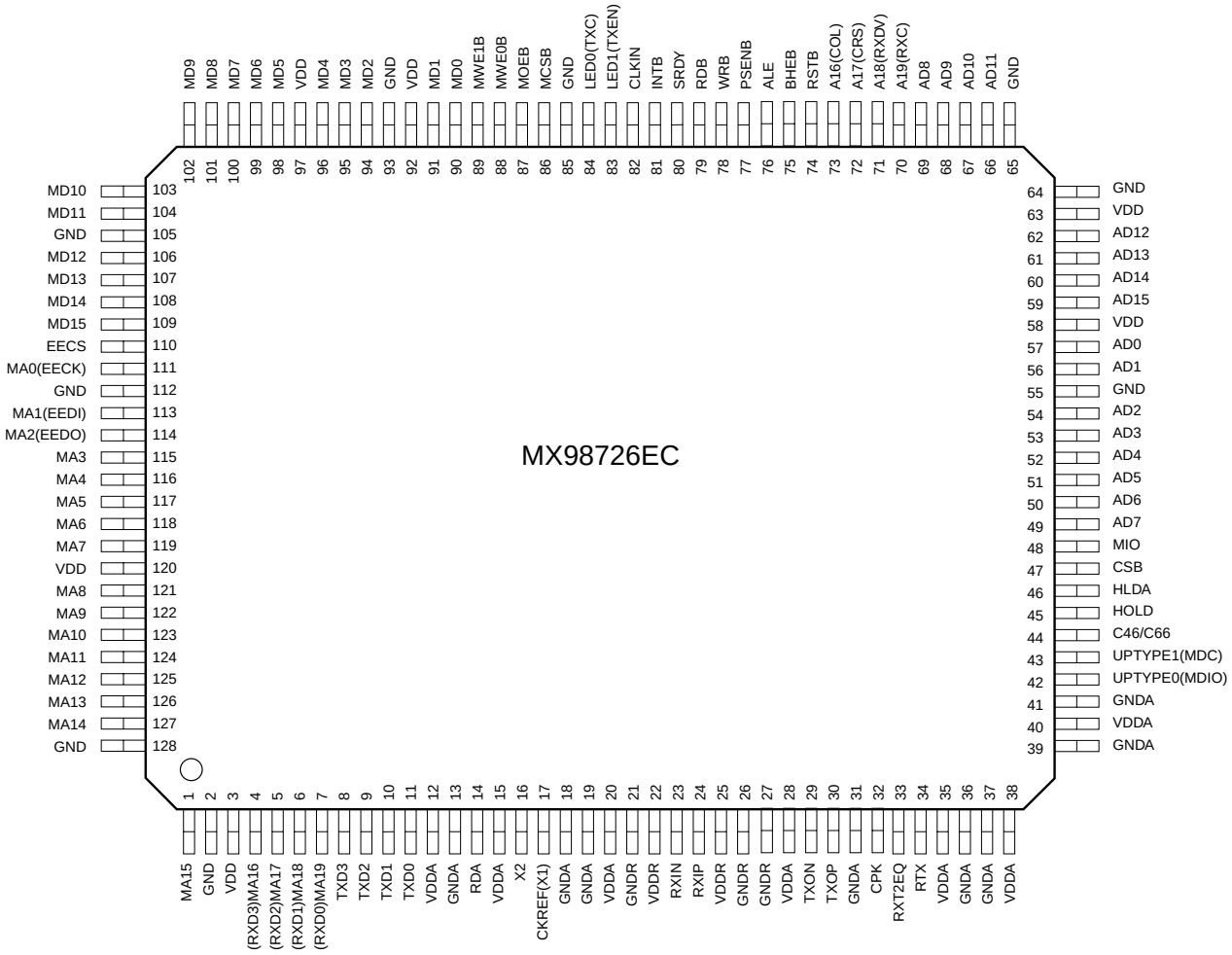
Shared memory Architecture

1.4 Combo Application



COMBO APPLICATION

2.0 Pin Configuration and Description



2.1 Pin Description :

PIN#	Pin Name	Type	Description
82	CLKIN	I, TTL	Host Clock Input : 8M to 40 Mhz.
49-54, 56,57	AD[7:0]	I/O, 4ma	Multiplexed Address/Data Bit [7:0] : Internal pull-down
59-62, 66-69	AD[15:8]	I/O, 4ma	Multiplexed Address/Data Bit [15:8] : Internal pull-down
76	ALE	I,TTL	Address Latch Enable : Active high
70	A19(RXC)	I, TTL	Host Bus Address Bit19, when on-chip tranceiver is used,it is used in A[19:16], when in MII mode, it is defined as receive clock RXC (25MHz or 2.5MHz) When this pin is used as address bit, it is internally grounded until Reg50.6 (A19A16EN bit) is set to enable decoding of this pin as address bit. Internal pull-up
71	A18(RXDV)	I,TTL	Host Bus Address Bit18, when on-chip tranceiver is used,it is used in A[19:16], when in MII mode, it is defined as receive data valid RXDV signal. When this pin is used as address bit, it is internally grounded until Reg50.6 (A19A16EN bit) is set to enable decoding of this pin as address bit. Internal pull-up.
72	A17(CRS)	I,TTL	Host Bus Address Bit17, when on-chip tranceiver is used, it is used in A[19:16], when in MII mode, it is defined as carrier same CRS signal. When this pin is used as address bit, it is internally grounded until Reg50.6 (A19A16EN bit) is set to enable decoding of this pin as address bit. Internal pull-up.
73	A16(COL)	I,TTL	Host Bus Address Bit16, when on-chip tranceiver is used, it is used in A[19:16], when in MII mode, it is defined as collision COL signal. When this pin is used as address bit, it is internally grounded until Reg50.6 (A19A16EN bit) is set to enable decoding of this pin as address bit. Internal pull-up.
79	RDB	I, TTL	Host Read Strobe: Active low. Internal pull-up
78	WRB	I, TTL	Host Write Strobe : Active low. Internal pull-up
81	INTB	O/D, 4ma	Host Interrupt Output : Polarity can be programmed, default is active low. For active Low interrupt application, external pull-up is reguired. For active high interrupt application, external pull-down is required.
75	BHEB	I,TTL	Host Byte High Enable : Internal pull-up. BHEB A0 Function 0 0 Word Transfer 0 1 Upper Byte Transfer 1 0 Lower Byte Transfer 1 1 Lower Byte Transfer
80	SRDY	O, 4ma	Synchronous Host Ready Output : Active high synchronized to CLKIN to indicate data is ready to be transferred. Initially low at the beginning of a host cycle.
47	CSB	I, TTL	Chip Select : Active low, used to enable GMAC to decode host address. When high, no host cycle is recognized by MAC.
48	MIO	I, TTL	Host Memory/IO cycle indicator : Set for memory access and reset for IO access. Internal pull-up. Decode of MIO can be disable by DISMIO register bit. Default is enabled.

45	HOLD	O, 4ma	Packet Memory Bus Hold Request : Active high to request Host to "float" its interface of the packet memory. Host grants the packet buffer bus to MX98726EC by asserting HLDA = 1.
46	HLDA	I, TTL	Packet Memory Bus Hold Acknowledge: Packet buffer bus is granted to MX98726EC. If HLDA=0 then MX98726EC will float its interface on the packet buffer. Internal pull-up.
77	PSENB	I, TTL	Host Program Strobe Enable : Active low to indicate current cycle is a ROM access and MX98726EC will not decode this ROM cycle. PSENB must high for packet memory access. Internal pull-up.
74	RSTB	I,TTL	Host Reset Input : Active low, Internal pull-up.

Packet Buffer Interface :

PIN#	Pin Name	Type	Description
1, 115-119	MA[19:3]	O,4ma	Memory Address Bit 19-0: If HLDA = 0 then all these address lines are tri-stated.
7	MA19(RXD0)	I/O, 4ma	Memory Address Bit19, when on-chip tranceiver is used, it is defined as MA19, while in MII mode, it is used as receive data bit RXD0 pin.
6	MA18(RXD1)	I/O, 4ma	Memory Address Bit18, when on-chip tranceiver is used, it is defined as MA18, while in MII mode, it is used as receive data bit RXD1 pin.
5	MA17(RXD2)	I/O, 4ma	Memory Address Bit17, when on-chip tranceiver is used, it is defined as MA17, while in MII mode, it is used as receive data bit RXD2 pin.
4	MA16(RXD3)	I/O, 4ma	Memory Address Bit16, when on-chip tranceiver is used, it is defined as MA16, while in MII mode, it is used as receive data bit RXD3 pin.
90-96, 98-104, 106-109	MD[15:0]	I/O,4ma	Memory Data Bit 15-0 : Internal pull-down.
114	MA2(EEDO)	1/O,4ma	Memory Address Bit 2 or EEPROM Data Out bit: Right after host reset, GMAC automatically load configuration information from external EEPROM. During this period, MA2 pin acts as a EEDO pin that read in output data stream from EEPROM. After EEPROM auto load sequence is done, this pin becomes MA2 together with MA[19:3] forms packet buffer address line 19 - 0. Internally pull-down.
113	MA1(EEDI)	1/O,4ma	Memory Address Bit 1 or EEPROM Data In bit: During EEPROM auto load sequence, MA1 pin acts as EEDI pin that write data stream into EEPROM. After EEPROM auto load sequence is done, this pin becomes MA1, together with MA[19:2] forms packet buffer address lines.
111	MA0(EECK)	1/O,4ma	Memory Address Bit 0 or EEPROM Clock Input : During EEPROM auto load sequence, MA0 pin acts as EECK pin that provides clock to EEPROM. After EEPROM auto load sequence is done, this pin becomes MA0, together with MA[19:1] forms packet buffer address lines.
87	MOEB	O,4ma	Memory Output Enable: Active low during packet buffer read access.
86	MCSB	O,4ma	Memory Chip Select: Active low during packet buffer accesses.
88, 89	MWEB[1:0]	O,4ma	Byte Write Enable: Active low during packet buffer write cycle. MWEB1 for high byte and MWEB0 for low byte.

10/100 Tranceiver interface :

PIN#	Pin Name	Type	Description
14	RDA	O	RDA external resistor to ground: 10K ohm, 5%
17	CKREF(X1)	I, TTL	25Mhz , 30 PPM external osc./crystal input :
16	X2	O	25Mhz , 30 PPM external crystal output :
23	RXIN	I	Twisted pair receive differential input: support both 10/100 Mbps speed
24	RXIP	I	Twisted pair receive differential input: support both 10/100 Mbps speed
29	TXON	O	Twisted pair transmit differential output: support both 10/100 Mbps speed, meet 802.3/802.3u spec.
30	TXOP	O	Twisted pair transmit differential output: support both 10/100 Mbps speed, meet 802.3/802.3u spec.
32	CPK	O	NC pin : used in test mode only
33	RTX2EQ	O	RTX2EQ external resistor to ground: 1.4K ohm, 5%
34	RTX	O	RTX external resistor to ground: 560 ohm, 5%

Miscellaneous :

PIN#	Pin Name	Type	Description
110	EECS	O,2ma	EEPROM Chip Select Signal : Active high
44	C46/C66	I,TTL	EEPROM Size Select : Set for C46, reset for C66. Internal pull-up.
84	LED0(TXC)	I/O,16ma	LED0 (TXC in MII mode) : When on-chip tranceiver is used, it is defined as SPEED LED. When the light is on, it indicates the 100 Mbps speed. When off, it indicates the 10 Mbps speed. When both LED0 and LED1 are flashing identically, it means the bus integrity error. (Internal pull-up). When in MII mode, this pin is defined as transmit clock TXC (25 MHz or 2.5 MHz) input.
83	LED1(TXEN)	O,16ma	LED1 (TXEN in MII mode) :When on-chip tranceiver is used, it is defined as Link/Activity LED. When the light is stable and on, it indicates a good link. When flashing, it indicates TX and RX activities. When off, it means a bad link. (Internal pull-up). When in MII mode, this pin is defined as transmit enable TXEN pin.
42,43	UPTYPE0,	I,TTL	uP type select control bit 1-0: UPTYPE1 and UPTYPE0 must be externally pull-up or down through ≤ 4.7K ohm resistors to configure the bus interface for different uP. UPTYPE1 UPTYPE0 uP selected 0 0 reserved 0 0 1 80x1 1 0 80188 1 1 80186
42	UPTYPE0(MDIO)	I/O,TTL	uP type select control bit 0 (MDIO in MII mode): UPTYPE0 is internally pull-down and used as uP type selection during host reset (RSTB=0). After host reset sequence is completed, this pin become MDIO pin if MII mode is selected.
43	UPTYPE1(MDC)	I/O, TTL	uP type select control bit 1 (MDC in MII mode) : UPTYPE1 is internally pull-down, after host reset sequence is completed , this pin become MDC clock output pin if MII mode is selected.

Vdd/Gnd Pins :

PIN#	Pin Name	Description
12,15,20,28,35,38,40	VDDA	Analog Vdd Pins : Must be carefully isolated in a separted vdd plane.
13,18,19,31,36,37,39,41	GNDA	Analog Ground Pins : Must be carefully isolated in a separted ground plane.
22,25	VDDR	RX Vdd Pins : Must be carefully isolated in a separted Vdd plane.
21,26,27	GNDR	RX Ground Pins : Must be carefully isolated in a separted ground plane.
3,58,63,92,97,120	VDD	Digital Vdd Pins : Must be carefully isolated in a separted Vdd plane.
2,55,64,65,85,93,105,112,128	GND	Digital Ground Pins : Must be carefully isolated in a separted ground plane.

3.0 Register (Default value is defined after hardware/power-up reset)

Reset logic : All register bits are cleared by hardware reset, while register bit with an "*" in its symbol name is also cleared by software reset.

Network Control Register A : NCRA (Reg00h),R/W, default=00h

Bit	Symbol	Description
0.0	RESET	Software reset.
0.1 0.2	ST0* ST1*	Start Transmit Command/Status : Write to issue commands. When done, both bits are cleared automatically. Transmit command : ST1 ST0 IDLE state 0 0 Read to indicate TX DMA idle state, write has no effect. TX DMA Poll 0 1 Start TX DMA, send packets stored in packet memory. TX FIFO Send 1 0 Immediately send the packet stored in the TX FIFO. TX DMA Poll 1 1 Start TX DMA, send packets stored in packet memory. All transmit commands are cleared to 00 when the operation is done to indicate idle state. When the TX DMA poll and the TX FIFO Send can not be used at the same time. New packet can be written to the FIFO directly only when ST1, ST0=IDLE and TXDMA[3:0]=1h. The TX DMA poll and the TX FIFO Send commands can be issued only when ST1, ST0=IDLE and TXDMA[3:0]=1h, regardless of any error status in previous transmission.
0.3	SR*	Start Receive: Enable the MAC receive packets. Default is disabled.
0.4, 0.5	LB0*,LB1*	Loopback Mode: LB1 LB0 Mode0 0 0 Normal mode Mode1 0 1 Internal FIFO Loopback Mode2 1 0 Internal NWAY Loopback Mode3 1 1 Internal PMD Loopback Mode 2 and 3 are reserved for IC test purpose. Only mode 1 can be used on bench. External loopback for bench can be done by full duplex normal mode with real cable hooked up from TX port to RX port.
0.6	INTMODE	Interrupt Mode: Set for active high interrupt, reset for active low interrupt case.
0.7	CLKSEL	Clock Select : Set to use internal 40MHz clock for all internal DMA, default is reset to use internal 50MHz clock for all internal DMA.

Network Control Register : NCRB (Reg01h),R/W, default=01h

Bit	Symbol	Description
1.0	PR*	Promiscuous mode: Set to receive any incoming valid frames received, regardless of its destination address. Default is set.
1.1	CA*	Capture Effect Mode: Set to enable an enhanced backoff algorithm to avoid network capture effect.
1.2	PM*	Pass Multicast: Set to accept all multicast packets including broadcast address (1st bit in destination address is 1), default is reset
1.3	PB*	Pass Bad Frame: Enable GMAC to accept Runt frame. Default is reset.
1.4	AB*	Accept Broadcast: Default is reset. Set to accept all broadcast packets.
1.5	HBD*	Reserved for test purpose. Default is 0.
Reserved		Must be 00.

GMAC Test Register A : TRA (Reg02h),R/W, default=00h

Bit	Symbol	Description
2.0	TEST	Test mode enable: Set to enable test modes defined by TMODE[2:0], default is reset for normal operation.
2.1-2.3	TMODE[2:0]	Test Mode Select bits[2:0]: Reserved for GMAC's internal tests, only meaningful when the TEST bit is set, except when TMODE [2:0] = "110" which is also used as normal mode with EEPROM interface disabled. When TMODE [2:0] = "110" & Test =0, then MA19~MA16 are still SRAM address bit19~16, while Test = 1, MA19~MA16 are defined as test pins reserved for debug purpose.
2.4	RWR	Receive Watchdog Release : When set, the receive watchdog is released 40 to 48 bit times from the last carrier deassertion. When reset, the receive watchdog is released 16 to 24 bits times from the last carrier deassertion.
2.5	RWD	Receive Watchdog Disable : When set, the receive watchdog is disabled. When reset, receive carriers longer than 2560 bytes are guaranteed to cause the watchdog timeout. Packets shorted than 2048 bytes are guaranteed to pass.
2.6	FC	Forced Collision : Set to force collision at every transmit packet, this bit works only in internal FIFO loopback mode, i.e. LB0=1, LB1=0, to test excessive collision. Default is reset.
2.7	SB	Start/Stop Backoff counter: When set, indicates internal backoff counter stops counting when any carrier is detected. Counter resumed when carrier drops. When reset, the internal backoff counter is not affected by carrier activity. Default is reset.

GMAC Test Register : TRB (Reg03h),R/W, default=00h

Bit	Symbol	Description
3.0	FKD*	Flaky Oscillator Disable: When set, indicates that the internal flaky oscillator is disabled. Pseudo random numbers are chosen instead of fully random numbers, used for the internal diagnostic purpose. Set to disable the normal clocking scheme in the timer's test. Reset to enable the timer test. Default is reset.
3.1	RDNCNTCB*	Reserved for test
3.2	RDNCNTSB*	Reserved for test
3.3	COLCNTCB*	Reserved for test
3.4	BFS0*(MDC)	Normally used as BFS0 pin for test purpose, while in MII mode, it is defined as MII management clock signal (MDC) to be used as a timing reference of MDIO pin.
3.5	BKCNTLB*(MDIOEN)	Normally used as BKCNTLB pin for test purpose, while in MII mode, it is used to control the direction of MDIO pin. Set MDIOEN = 1 will make MDIO pin as input pin, the value can be read from MDI bit. Set MDIOEN = 0 will make MDIO pin as output pin, the value of MDO bit is driven out to MDIO pin.
3.6	BFS1*(MDO)	Normally used as BFS1 pin for test purpose, while in MII mode, it is used as MII management write data (MDO) for MDIO pin's output data.
3.7	BFSTATUS*(MDI)	Normally used as BFSTATUS pin for test purpose, while in MII mode, it is used as MII management read data (MDI) for MDIO pin's input data.

Last Transmitted Packet Status: LTPS (Reg04h), RO, default=00h

Bit	Symbol	Description
4.0	CC0*	Collision Count Bit 0 :
4.1	CC1*	Collision Count Bit 1 :
4.2	CC2*	Collision Count Bit 2 :
4.3	CC3*	Collision Count Bit 3 : when CC[3:0] = 1111 and a new collision is detected, then it is called excessive collision error which will abort the current packet, TEI interrupt bit will be set.
4.4	CRSLOST*	Carrier Sense Lost : Set to indicate CRS was lost during the transmission, default is reset for normal packet transmission.
4.5	UF*	TX FIFO underflow : Set to indicate a underflow problem in TX FIFO an FIFOEI interrupt is generated for driver to resolve this problem.
4.6	OWC*	Out of Window Collision : Set to indicate an collision occured after 64 bytes of data has been transmitted, no retransmission will be issued
4.7	TERR*	Transmit Error: Set to indicate packet transmitted with error, reset for normal packet transmission.

Last Received Packet Status: LRPS (Reg05h), RO, default=00h

Bit	Symbol	Description
5.0	BF*	RX Packet Buffer Full Error : 1 indicates RX packet buffer is full.
5.1	CRC*	CRC error : Calculation is based on integer multiple of bytes, set to indicate CRC error for received packet.
5.2	FAE*	Frame Alignment Error : Set to indicate extra nibble is received which is not at octet boundary. This error is independent of CRC detection.
5.3	FO*	FIFO overrun : When set, an interrupt is generated, driver must resolve this error.
5.4	RW*	Receive Watchdog : Set to indicate the frame length exceeds 2048 bytes. An interrupt will be generated to driver.
5.5	MF*	Multicast address : Set to indicate current frame has multicast address.
5.6	RF*	Runt Frame : Set to indicate a frame length less than 64 bytes, only meaningful when Reg01h.3 PB bit =1 is set.
5.7	RERR*	Receive Error : Set to indicate a packet received with errors including CRC, FAE, FO, RW, (RF and PB=1).

Notes : This LRPS register contains the same status byte as in the description field of the last received packet in the packet memory.

Missed Packet Counter: MPC (Reg07/06h), R/W, default=0000h

Bit	Symbol	Description
6.7-0	MISSCNT[7:0]*	Miss Packet Counter Bit [7:0]: Lower byte of Miss packet counter
7.7-0	MISSCNT[15:8]*	Miss Packet Counter Bit [15:8]: Upper byte of Miss packet counter

Interrupt Mask Register: IMR (Reg08h), R/W, default=00h

Bit	Symbol	Description
8.0	CNTOFIM	Miss Counter Over Flow Interrupt Mask : Set to enable Miss counter overflow interrupt, default is reset. When Overflow condition of the miss packet counter occures, counter is halt and driver need to resolve this condition in order to reset the counter if counter is ever used.
8.1	RIM	Received Interrupt Mask: Set to enable Packet Received Interrupt, default is reset which disable RI interrupt.
8.2	TIM	Transmit Interrupt Mask: Set to enable Packet transmit OK interrupt, default is reset which disable TI interrupt.
8.3	RXEIM	Receive Error Mask: Set to enable Receive Error interrupt, default is reset which disable RXEI interrupt.
8.4	TXEIM	Transmit Error Mask: Set to enable transmit error interrupt, default is reset which disable TXEI interrupt.
8.5	FIFOEIM	FIFO Error Interrupt Mask: Set to enable FIFO Error interrupt, default is reset which disable FIFOEI interrupt.
8.6	BUSEIM	Bus Error Interrupt Mask: Set to enable Bus Error interrupt, default is reset which disable BUSEI interrupt.
8.7	RBFIM	RX Buffer Full Interrupt Mask: Set to enable RX Buffer full interrupt, default is reset which disable BFI interrupt.

Interrupt Register: IR (Reg09h), R/W, default=00h

Bit	Symbol	Description
9.0	CNTOFI*	Miss Counter Over Flow Interrupt : Set to assert interrupt when Miss packet counter is overflow, write 1 to this bit will clear the bit and interrupt, write 0 has no effect.
9.1	RI*	Receive OK interrupt : Set to assert interrupt, write 1 to this bit will clear the bit and interrupt, write 0 has no effect
9.2	TI*	Transmit OK interrupt: Set to assert interrupt, write 1 to this bit will clear the bit and interrupt, write 0 has no effect
9.3	REI*	Receive Error Interrupt: Set to assert interrupt when packet is received with error , write 1 to this bit will clear the bit and interrupt, write 0 has no effect
9.4	TEI*	Transmit Error Interrupt : Set to assert interrupt when packet is transmitted with error, write 1 to this bit will clear the bit and interrupt, write 0 has no effect
9.5	FIFOEI*	FIFO Error Interrupt: Set to assert interrupt when either TX FIFO is overrun or RX FIFO is overrun, write 1 to this bit will clear the bit and interrupt, write 0 has no effect
9.6	BUSEI*	Bus Error Interrupt: Set to assert interrupt when Bus integrity check is enabled and failed. Write 1 to this bit will clear the bit and interrupt, write 0 has no effect
9.7	RBFI*	RX Buffer Full Interrupt: Set to assert interrupt when RX buffer area is being overwritten by new received packets, write 1 to this bit will clear the bit and interrupt, write 0 has no effect

Note : All page pointer bit [11:0] are mapped to MA[19:8] in the same bit ordering.

Boundary Page Pointer Register: BP (Reg0Bh/0Ah), R/W, default=x000h

Bit	Symbol	Description
0A.7-0, 0B.3-0	BP[11:0]	Boundary Page Pointer between tx/rx buffer: page TLBP[11:0] to page BP[11:0] is tx buffer. page BP[11:0] to RHBP[11:0] is rx buffer. BP[11:0] is mapped to MA[19:8]. MSB bit is Reg0BH.3 bit. LSB is Reg0AH.0 bit.

TX Low Boundary Page Pointer Register: TLBP (Reg0Dh/0Ch), R/W, default=x000h

Bit	Symbol	Description
0C.7-0, 0D.3-0	TLBP[11:0]	TX Low Boundary Page Pointer : Points to the first page of transmit buffer ring. It's a static pointer that is used by GmAC to link to the last page pointed by boundary pointer. TLBP[11:0] MSB bit is Reg0Fh.3 bit. LSB is Reg0Ch.0 bit.

Transmit Buffer Write Page Pointer : TWP (Reg.0Fh/0Eh), R/W, default=x000h

Bit	Symbol	Description
0E.7-0, 0F.3-0	TWP[11:0]	Transmit Buffer Write Page Pointer: TWP[11:0] are mapped to MA[19:8] with the same bit ordering. The MSB is the Reg0Fh.3 bit. The LSB is the Reg0Eh.0 bit. TWP is normally controlled by the device driver. An internal Byte Counter (TWPBC) is associated with this page register.

IO Base Page Register: IOB (Reg11h/10h), R/W, default=x000h

Bit	Symbol	Description
10.7-0, 11.3-0	IOB[11:0]	IO Base Address Register: On-chip register IO base address register. This page address register defines the base page address of all on-chip registers in a IO address space.(00h-FFh). MIO=0 and CSB=0 will force GMAC to decode IO address for on chip register access. if MIO=1 and CSB=0, then all on chip registers are localed in memory page 0. IOB register is mapped to physical address [19:8] during decoding. IOB is 0000h after Reset, software can assign new base address by writing new page number to this register.

Transmit Buffer Read Page Pointer Register: TRP (Reg13h/12h), R/W, default=x000h

Bit	Symbol	Description
12.7-0, 13.0-3	TRP[11:0]	The Page Index of transmit buffer read pointer: Current transmit read page pointer. MSB bit is Reg13h.3 bit. LSB is Reg12h.0 bit. TRP is controlled by GMAC only. An internal Byte Counter (TRPBC) is associated with this page register.

Receive Interrupt Timer: RXINTT (Reg15h/14h), R/W

Bit	Symbol	Description
14.7-0, 15.7-0,	RXINTT[7:0], RXINTT[15:8]	Receive Interrupt Timer: Default is 0000h "not used".

Receive Buffer Write Page Pointer Register: RWP (Reg17h/16h), R/W, default=x000h

Bit	Symbol	Description
16.7-0, 17.0-3	RWP[11:0]	Receive Buffer Write Page Pointer: Current receive write page pointer. MSB bit is Reg17h.3 bit. LSB is Reg16h.0 bit. This register is controlled by GMAC only. An internal Byte Counter (RWPBC) is associated with this page register.

Receive Buffer Read Page Pointer Register: RRP (Reg19h/18h), R/W, default=000h

Bit	Symbol	Description
18.7-0, 19.0-3	RRP[11:0]	Receive Buffer Read Page Pointer: MAC current receive read page pointer. RRP[11:0] is mapped to MA[19:8]. MSB bit is Reg19h.3 bit. LSB is Reg18h.0 bit. This register is normally controlled by device driver. An internal byte Counter (RRPBC) is associated with this page register.

64K Memory Bank Address : Reg19h (R/W), default=0h

Bit	Symbol	Description
19.7-4	BANK[3:0]	Reserved : Default is 0000

RX High Boundary Page Pointer Register: RHBP (Reg1Bh/1Ah), R/W, default=x000h

Bit	Symbol	Description
1A.7-0. 1B.0-3	RHBP[11:0]	Receive High Boundary Page Pointer : RX packet buffer is defined as between RHBP [11:0] and BP[11:0]. MSB bit is Reg1Bh.3 bit. LSB is Reg1Ah.0 bit.

EEPROM Interface Register: Reg1Ch, R/W, default=00h

Bit	Symbol	Description
1C.0	EECS*	Chip select output to external EEPROM clock device
1C.1	EECK*	Serial clock output to external EEPROM clock device, <1MHz
1C.2	EEDI*	Serial data input to external EEPROM clock device
1C.3	EEDO*	Serial data output from external EEPROM clock device
1C.4	EESEL*	Set to enable external EEPROM write operation, default 0 is read.
1C.5	EELD*	Set to enable reloading the entire content of EEPROM just like power-on reset or hardware reset. When loading is done, this bit will be set by GMAC automatically.
1C.6	HOLDREQ	Reserved, default = 0, set to hold host access to SRAM in order to access EEPROM by software.
1C.7	HLDAACK	Reserved, Read only, set to indicate that request to hold host is granted, GMAC can access EEPROM through Reg. IC by software.

Reserved (Reg 1Dh), default=00h

Bit	Symbol	Description
Reserved		Must be 00h

Reserved (Reg1Fh/1Eh), R/W, default=0000h

Bit	Symbol	Description
1E.7-0, 1F.7-0	reserved	

Network Address Registers : Reg20h~25h (R/W), 26h~2Dh (R/W), default=00h

Bit	Symbol	Description
20.[7:0]	PAR0	Physical Address Byte 0: PAR[7:0]
21.[7:0]	PAR1	Physical Address Byte 1: PAR[15:8]
22.[7:0]	PAR2	Physical Address Byte 2 : PAR[23:16]
23.[7:0]	PAR3	Physical Address Byte 3 : PAR[31:24]
24.[7:0]	PAR4	Physical Address Byte 4 : PAR[39:32]
25.[7:0]	PAR5	Physical Address Byte 5 : PAR[47:40]
26.[7:0]	MAR0	Hash Table Register Byte 0 : MAR[7:0]
27.[7:0]	MAR1	Hash Table Register Byte 1 : MAR[15:8]
28.[7:0]	MAR2	Hash Table Register Byte 2 : MAR[23:16]
29.[7:0]	MAR3	Hash Table Register Byte 3 : MAR[31:24]
2A.[7:0]	MAR4	Hash Table Register Byte 4 : MAR[39:32]
2B.[7:0]	MAR5	Hash Table Register Byte 5 : MAR[47:40]
2C.[7:0]	MAR6	Hash Table Register Byte 6 : MAR[56:48]
2D.[7:0]	MAR7	Hash Table Register Byte 7 : MAR[63:57]

Transceiver Control Register : ANALOG (Reg 2Eh), R/W, default=07h

Bit	Symbol	Description
2E.0	DS120	Must be 1 for NORMAL mode with auto-compensation.
2E.1	DS130	Must be 1 for NORMAL mode with auto-compensation
2E.2	PWD10B	Set for NORMAL mode, write 0 followed by write 1 will power down 10 Base-T analog circuit.
2E.3	PWD100	Reset for NORMAL mode, write 1 followed by write 0 will power down 100 Base-T analog circuit.
2E.4	RSQ	Reduced SQuelch Enable : Set to enable the reduced squelch circuit in the 10 Base-T mode for the receive channel. This can help the reception in a long cable application. Default is reset, meaning the normal CAT-5 cable is used.
2E.5	RST100	Reset for NORMAL mode, write 1 followed by write 0 will reset 100 Bare-T analog circuit.
2E.6-7	Reserved	must be zero.

Reserved, default=00h

Bit	Symbol	Description
2F.7-0	Reserved	

NWAY Configuration Register : NWAYC (Reg 30h), R/W, default=84h

Bit	Symbol	Description
30.0	FD	Full Duplex Mode: Set 1 to force the full duplex mode. The default is 0, meaning the half duplex mode. This bit is meaningful only if ANE = 0
30.1	PS100/10	Port Select 100/10 bit : Default is 0, meaning the 10 Base-T mode.
30.2	ANE	Autonegotiation Enable: Set to enable the NWAY function. Default is set. ANS[2:0] should be written 001 to restart the autonegotiation sequence after ANE is set.
30.[5:3]	ANS[2:0]	Autonegotiation status bits: Read only for the NWAY status, except when write 001 will restart the autonegotiation sequence. The MSB is the Reg30h.5 bit when Nway settles down in one network mode, one bit of Reg31.4~Reg 31.7 will be set to indicate the chosen network mode. Autonegotiation Arbitration State, arbitration states are defined 000 = Autonegotiation disable 001 = Transmit disable 010 = ability detect 011 = Acknowledge detect 100 = Complete acknowledge detect 101 = FLP link good; autonegotiation complete 110 = Link check
30.6	NTTEST	Reserved
30.7	LTE	Link Test Enable : Default is high, meaning the link check is always enabled. Reset forces a good link in the 10 Base-T mode for the testing purpose.

NWAY Status Register : NWAYS (Reg 31h), RO, default=00h

Bit	Symbol	Description
31.0	LS10	Physical Link Status of 10 Mbps TP : Set for good link in 10 Base-T.
31.1	LS100	Physical Link Status of 100 Mbps TP : Set for good link in 100 Base-TX.
31.2	LPNWAY	Link Partner Status : 1 to indicate link partner is capable of NWAY support, reset for non-NWAY link partner.
31.3	ANCLPT	Autonegotiation Completion : Set to indicate that a normal NWAY state machine completion. Reset for incomplete.
31.4	100TXF	NWAY 100 TX Full_duplex Mode : Set to indicate NWAY is settle down in 100 TX full duplex mode.
31.5	100TXH	NWAY 100 TX Half_dulpex Mode : Set to indicate NWAY is settle down in 100 Base-T half duplex mode.
31.6	10TXF	NWAY 10 TX Full_duplex Mode : Set to indicate NWAY is settle down in 10 Base-T full duplex mode.
31.7	10TXH	NWAY 10 TX Half_duplex Mode : Set to indicate NWAY is settle down in 10 Base-T half duplex mode.

GMAC Configuration A Register: GCA (Reg32h), R/W, default=00h

Bit	Symbol	Description
32.0	BPSCRM	Bypass 100TX Scrambler: Default is 0, meaning enable scrambler during 100TX mode, set to disable scrambler.
32.1	PBW	Packet Buffer Data Width : Default is 0. Meaning packet buffer data width is byte wide. Set for word (16 bit) wide packet buffer. For 8 bit system bus, the packet buffer bus width must be byte wide.
32.2	SLOWSRAM	Slow SRAM select bit: Default is 0 meaning fast SRAM must be used (Taa <= 20ns), if set , then Taa<= 70ns can be used. Slow SRAM will reduce packet through put, therefore, if high speed host is intended, then SRAM should be fast otherwise, FIFO underrun or overrun can happen.
32.3	ARXERRB	Accept RX packet with error : Default is reset to receive packets with error, set to reject packets with error, packet memory will not contain packet with RW, FO, CRC errors.
32.4	MIISEL	Default = 0 after reset, on-chip tranceiver is used. Set by software to enable MII interface.
32.5	AUTOPUB	Auto Page Update option : Set to disable the automatic host page update during the host DMAs. Reset to enable the host page update for the RRP, TWP registers. Default is reset.
32.6	TXFIFOCNTEN	Default=0, after rest which means Reg 3E & 3F (TXFIFOCNT) are not used. This option is only good for a byte-base host transfer. For host which do word/double word transfer, this bit must be set to 1 to force TXFIFO use actual packet length for transmission.
32.7	reserved	

GMAC Configuration B Register: GCB (Reg33h), R/W

Bit	Symbol	Description			
33.1-0	TTHD[1:0]	Transmit FIFO Threshold : Default is 00			
		TTHD1	TTHD0	FIFO depth	aggressiveness
		0	0	1/2	medium
		0	1	1/4	least
		1	0	3/4	most
		1	1	reserved	reserved
33.3-2	RTHD[1:0]	Receive FIFO Threshold : Default is 00			
		RTHD1	RTHD0	FIFO depth	aggressiveness
		0	0	1/2	medium
		0	1	1/4	most
		1	0	3/4	least
		1	1	reserved	reserved
33.4	SRAMELEN	SRAM Early Latch Enable : Default = 0. Set to enable.			
33.5	X4ELEN	X4 FIFO Early Latch Enable : Defautl = 0. Set to enable.			
33.6	DREQB2EN	DREQB NEW Timing Enable : Default = 0. Set to enable.			
33.7	reserved				

Reserved (Reg34h/35h/36h/37h), R/W

Bit	Symbol	Description
34.7-0	Reserved	
35,7-0		
36.7-0		
38.8-0		
34.7-0	Reserved	
35,7-0		
36.7-0		
37.7-0		

Reserved (Reg39h/38h), R/W, default=0000h

Bit	Symbol	Description
38.7-0	Reserved	
39.7-0	Reserved	

Reserved (Reg3Ah), default=00h

Bit	Symbol	Description
3A.7-0	Reserved	

Link Partner Link Code Register : LPC, Reg3Bh, RO

Bit	Symbol	Description
3B.0	LPC[0]	Link Partner Link Code A0 : 10 Base-T half duplex ability
3B.1	LPC[1]	Link Partner Link Code A1 : 10 Base-T full duplex ability
3B.2	LPC[2]	Link Partner Link Code A2 : 100 Base-TX half duplex ability
3B.3	LPC[3]	Link Partner Link Code A3 : 100 Base-TX full duplex ability
3B.4	LPC[4]	Link Partner Link Code A4 : 100 Base-T4 ability
3B.5	LPC[5]	Link Partner Link Code RF bit : Remote Fault bit
3B.6	LPC[6]	Link Partner Link Code Ack bit : Acknowledge bit
3B.7	LPC[7]	Link Partner Link Code NP bit : Next Page bit

TX/RX DMA Status Register: Reg3Ch, R/W, default=00h

Bit	Symbol	Description
3C.7-4	TXDMA[3:0]*	TX DMA State Indicators : For internal diagnostic purpose indicating TX DMA's current status. TXDMA3 is TX status error bit, set to indicate error during transmission. TXDMA2 is TX FIFO underflow error.
3C.3-0	RXDMA[3:0]*	RX DMA State Indicators : For internal diagnostic purpose indicating RX DMA's current status. RXDMA3 is RX status error bit, set to indicate error during receive. RXDMA2 is RX FIFO overflow error.

TXDMA[1:0]	State Description
00	Idle
01	Read TX Description
10	Transmit Current Packet
11	Write TX Description

RXDMA[1:0]	State Description
00	Idle
01	Receive Current Packet
10	Write TX Description
11	Run Frame/Reset RX FIFO

MISC Control Register : MISC1, Reg3Dh, R/W, default=3Ch

Bit	Symbol	Description
3D.0	BURSTDMA	reserved for internal DMA burst control, default = 0 after reset.
3D.1	DISLDMA*	Disable Local DMA arbitration : Default is 0 after reset, meaning local DMAs are enabled in the SRAM bus arbitration. Set to disable the local DMA arbitration only when the Reg02h.0 TEST bit is also set. It is used to force the overrun or the underrun error for the test purpose.
3D.2	TPF	10 Base-T Port Full Duplex capability bit in the linkcode word : Default is set to enable advertising the 10 Base-T Full duplex capability. Reset to disable advertising this capability in the outgoing NWAY's linkcode word.
3D.3	TPH	10 Base-T Port Half Duplex capability bit in the linkcode word : Default is set to enable advertising the 10 Base-T Half duplex capability. Reset to disable advertising this capability in the outgoing NWAY's linkcode word.
3D.4	TXF	100 Base-TX Full Duplex capability bit in the linkcode word : Default is set to enable advertising the 100 Base-TX Full duplex capability. Reset to disable advertising this capability in the outgoing NWAY's linkcode word.
3D.5	TXH	100 Base-TX Half Duplex capability bit in the linkcode word ; Default is set to enable advertising the 100 Base-TX Half duplex capability. Reset to disable advertising this capability in the outgoing NWAY's linkcode word.
3D.6	TXFIFORST	TX FIFO Reset control : Writing a 1 to this bit will clear the TX FIFO, reset all the current TX FIFO's internal pointers and related byte counters and bring the TX DMA back to the idle state. After reset this bit to 0, GMAC starts normal operation. If current transmission takes too long due to collisions, the software can use this bit to abort "current transmission" and bring GMAC's TX DMA back to idle state for a fresh new transmission.
3D.7	RXFIFORST	RX FIFO Reset control : Writing a 1 to this bit will clear the RX FIFO, reset all the current RX FIFO's internal pointers and related byte counters and bring the RX DMA back to the idle state. After reset this bit to 0, GMAC starts normal operation.

TX FIFO Byte Counter (Direct FIFO Mode) : TXFIFOCNT, Reg3F/3Eh, R/W

Bit	Symbol	Description
3E.7-0	TXFIFOCNT[7:0]	TX FIFO Send Byte Count bit [7:0]: Together with TXFIFOCNT[11:8] forms a 12 bits TX FIFO byte count for direct FIFO mode.
3F.3-0	TXFIFOCNT[11:8]	TX FIFO Send Byte Count bit [11:8]: Together with TXFIFOCNT[7:0] forms a 12 bits TX FIFO byte count for direct FIFO mode.

Reser ved (Reg 40h-43h), RO

Bit	Symbol	Description
Reserved		Register 40h[7:0] to register43h[7:0] are all reserved.

ID1 (Reg45h/44h), RO, default="MX"

Bit	Symbol	Description
44.7-0, 45.7-0	ID1[15:0]	ID1 16 bit code : Reg45h is MSB byte is set to "M", Reg44h is LSB byte is set to "X".

ID2 (Reg46h/47h), RO, default="0001"

Bit	Symbol	Description
46.7-0, 47.7-0	ID2[15:0]	ID2 16 bit code : Reg47h is MSB byte is set to 00h, Reg46h is LSB byte is set to 01h.

Write TX FIFO Data Port: WRTXFIFOD (Reg48h), WO

Bit	Symbol	Description
48.7-0,	WRTXFIFOD[7:0]	Write TX FIFO Data Port: Data written to this port is directly forward to TX FIFO, GMAC will keep track of total bytes written to FIFO. ST1,ST0 should be in IDLE state when a packet is started to be written through this port. Don't mix the write to this port with TX DMA start command, this may inter-mix data coming from this port and TX local DMA from packet memory.
49.7-0,	Reserved	
4A.7-0	Reserved	
4B.7-0	Reserved	

IO Read Data Port: Register : Reserved, RO

Bit	Symbol
4C.7-0,	Reserved
4D.7-0	Reserved
4E.7-0	Reserved
4F.7-0	Reserved

MISC Control Register 2 : MISC2, Reg50h, R/W, default=00h.

Bit	Symbol	Description
50.0	Reserved	
50.1	Reserved	
50.2	RUNTSIZE	Runt Frame Size Select bit : Default is 0, meaning the runt frame is defined as less than 64 bytes. Set to define the runt frame as less than 60 bytes.
50.3	Reserved	
50.4	Reserved	
50.5	ITPSEL	reserved for internal test probing select.
50.6	A19A16EN	Default=0, A19 to A16 are internally grounded. Set this bit to enable A19 to A16 decoding. This bit is ignored if MIISEL = 1 in MII mode.
50.7	AUTORCVR	Auto RX Full Recovery: Default is reset meaning when RX buffer full and RX FIFO overflow happen at the same time, GMAC will stop receiving until host clear up RX FIFO and RX full condition. Set to enable GMAC to recover from such error automatically , the last packet with such error will be discarded in the packet memory and RX FIFO will be cleared at the end of current receiving, and then receiving is resumed for next packet.

Host Receive Packet Counter : Reserved, RO

Bit	Symbol
52.7-0	Reserved
53.7-0	Reserved

Host DMA Fragment Counter : Reserved, RW

Bit	Symbol
54.7-0	Reserved
55.7-0	Reserved
56.7-0	Reserved

4.0 Host Communication

GMAC and the device driver communicate through three data structures :

* On chip registers described in Chapter 3.
* Descriptor and data buffer resides in packet memory.
* Direct IO port to on chip TX FIFO for direct packet transmission.

ON CHIP REGISTERS ADDRESSING SCHEME

MIO=1 and CSB=0, memory space page0 (from 00000h00 to 000ffh) is used for GMAC's on chip register. Therefore, page0 of memory mapped scheme is always recerved for GMAC's on chip registers and can not be used as part of packet buffer. So that usable free packet buffer of a 64K SRAM is actually 64K bytes - 256 bytes if GMAC's on chip registers occupied memory page0.

if MIO=0 and CSB=0, then I/O space is used to decode GMAC's on chip register access. IOB page register is initially 0 force GMAC to use page 0 of I/O space as GMAC's on chip register's page.
After changing IOB to a desirable page address, GMAC's on chip registers address can be relocated to other page for system integration. Such IO addressing scheme for GMAC on chip register can avoid the waste of SRAM's page 0 issue described above.

TX RING BUFFER AND RX RING BUFFER

GMAC moves received data frames to the receive buffer in the local packet memory and transmits data from the transmit buffers in the local packet memory. All the page pointers in the registers together with the descriptors acts as pointers to these buffers in the packet memory. Figure 4.0 depict the general data structure of packet memory and page pointers.

There are two data buffers inside the packet memory, i.e. transmit buffer and receive buffer. Packet memory is partitioned into pages, each page contains exactly 256 bytes. A page pointer defined by registers acts as the base address of the corresponding page. By programming these page pointers, size and area of transmit buffer and receive buffer can be individually set to desirable size and area.

The transmit and receive buffers must be contiguous and separated by the BP (Boundary Page pointer) defined in registers 0Ah and 0Bh. TLBP (Transmit Low Boundary Pointer) defines the start page of the transmit buffer. BP- 1 defines the end page of the transmit buffer. If the current transmit process exceeds the end of BP- 1 page then it will be set to the start page pointed by TLBP, thus forms a "ring buffer" that logically links the end page back to the start page of transmit buffer.

Receive buffer has a similar structure as transmit buffer. The start page of receive buffer is pointed to by BP while the end page is pointed to by RHBP (Receive High Boundary Page Pointer). If current receive process exceeds the end of the end page pointed by RHBP, then it will be set to the start page pointed by BP, thus forms a "ring buffer" that logically links the end page and the start page of receive buffer.

MORE RECEIVE BANDWIDTH WITHOUT USING TX RING BUFFER

A 1.6K bytes TX FIFO can also be used to send out a packet directly from FIFO. Register port 48h can be used by host to write packet data directly into TX FIFO. After moving the last byte into the TX FIFO of a packet, host can issue a command (called TX FIFO send command) to send out the packet stored in the TX FIFO. This function can be used alternately with the other transmission that uses TX buffer ring.

All incoming and outgoing packets are stored in these buffers. Long packet may occupy multiple pages that are logically contiguous. The descriptor is located at the beginning of the first page of this multiple-page packet. Normally there might be some free space left in the last page of this multiple-page packet which is called fragment. These fragment will not affect network packet's data integrity.

Descriptor structure

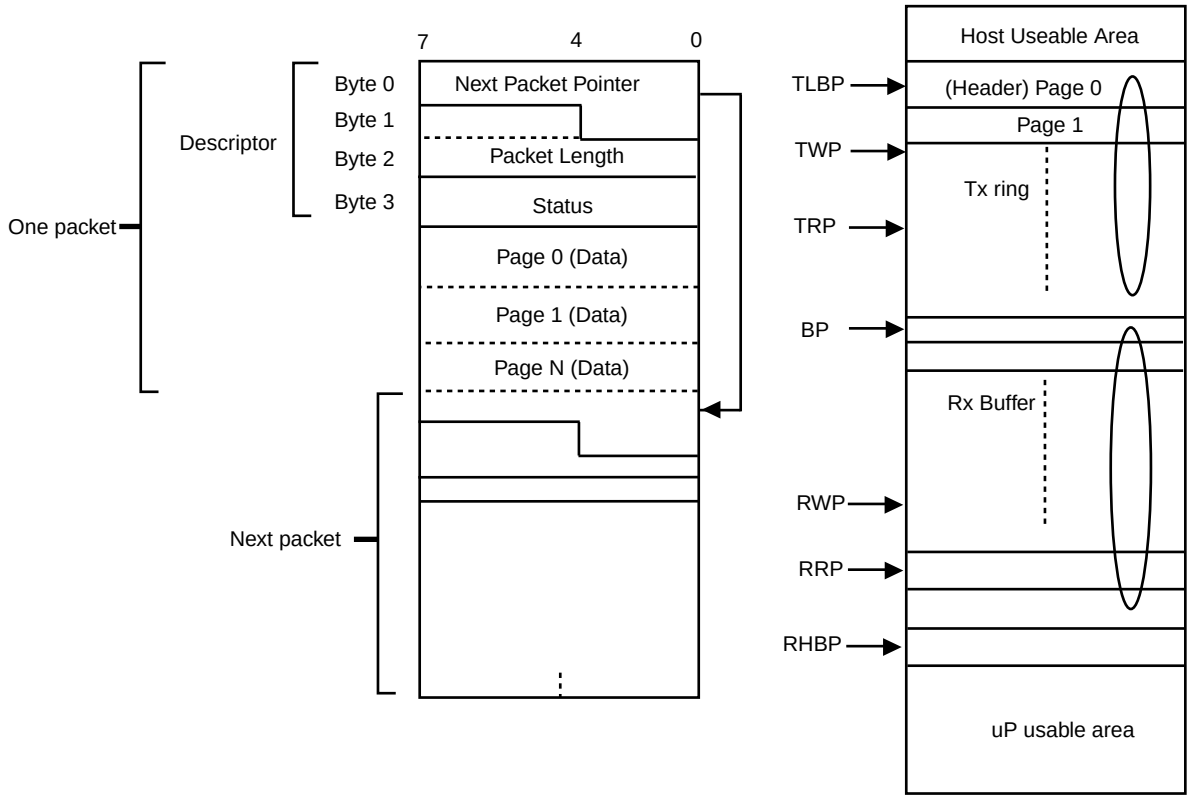


Figure 4.0 Packet Buffer Data Structures

4.1 Packet Transmission

GMAC supports two ways to prepare packet(s) for transmission, one way is the host can write a packet directly into TX FIFO through an IO port and send the packet directly from FIFO, this way is called direct FIFO mode. The other way is to write packet(s) into TX buffer ring in the packet memory and activate TX local DMA to send out packet(s). Using direct FIFO mode can eliminate TX local DMA completely which will leave packet memory's total bandwidth to RX local DMA and host. Therefore, receiving at the full line speed is more achievable in this way. The disadvantage is that only one packet is prepared and sent out at a time, next packet must wait until current packet is sent out and FIFO is empty before it can be moved into TX FIFO. In another word, you can not issue multiple packet transmission with a single command. But you still can prepare new packet(s) in TX buffer ring while a packet in direct FIFO mode is still active, so once the packet in direct FIFO mode is finished, you can active TX DMA right away.

The TX local DMA mode is used between GMAC and packet memory during transmission of packet. TRP (Transmit Read Page pointer) is used by local DMA to fetch the first page of the desired packet in the packet memory. When GMAC receive a TX DMA send command (register 00h.ST1=0, ST0=1), data in the packet memory will be moved into GMAC's transmit FIFO. GMAC will append preamble, sync and CRC field during the actual tranmission. The advantage of this mode is multiple packets can be processed with a single comannd, also new packet(s) can be prepared while TX local DMA is active. Therefore, potential higher through-put of TX channel can be achieved. The disadvantage is packet memory bandwidth is now shared by host, TX channel and RX channel. This means bandwidth might not be enough for all three to run at their full speed which may result in TX FIFO underrun, or RX FIFO overrun and slow host accesses, especially in a system where you only have a 8 bit packet memory.

It may be desireable to mix both direct FIFO mode anf TX local DMA mode so that bandwidth of packet memory and convenience of concurrent processing of mutiple packets can be compromised for the best interest of the system's performance. Some cautions should be taken when you using mixed mode. Do not write to FIFO while TX local DMA is active, because such write will corrupt whatever packet being transmitted in the FIFO. Do not activate TX local DMA while direct FIFO send has not been finished for current packet's transmission. Register 00h.ST1 and ST0 bits are both command and status, before host issues any packet send command. Always read these two bits and make sure they are both 0 which indicate a transmit cnahhel IDLE (FIFO is also empty). The rule of the mixed modes is always activate one mode at a time, ST1 and ST0 must be both 0 before the other mode is used.

Prior to transmission in direct FIFO mode

When ST1 and ST0 bits are both 0, host can write a packet no longer than 1518 bytes through IO port register 48h. GMAC will record the byte count. Since register 48h is write only port, it can not be read. Before the entire packet is completely inside FIFO, host can do other operations except activating TX local DMA. Issuing TX local DMA before current direct FIFO write operations or TX FIFO send completion will "corrupt" current packet inside TX FIFO. When the entire packet is in the FIFO, host can issue ST1=1 and ST0=0 (TX FIFO send command). When this packet is sent out completely, transmit status will be recorded in register 04h and both ST1 and ST0 are cleared to 0 to indicate IDLE state.

Prior to transmission in TX local DMA mode

The transmit descriptor located at the beginning of the first page of the desired packet in the packet memory must be properly set by device driver prior to a transmit command. By using TWP (Transmit Write Page Pointer), device driver can fill up packet(s) in the transmit buffer ring. For single packet transmission, the Next Packet Page Pointer field should be equal to TRP page pointer which links to the current packet itself. If multiple packets are to be transmitted, then Next Packet Page Pointer field of transmit descriptor should be set to the start page of next packet. Current Packet Length (in byte) is set to indicate the size of current packet. Transmit Status bit 7 (OWN bit) of the descriptor needed to be set to 1 to indicate that device driver has finished preparing the current packet. Then the packet can be transferred to GMAC for transmission. At this point, transmit command can be issued by setting Reg00h.ST1=0, ST0=1 (TX DMA poll command) to activate transmit operation. ST1 and ST0 bits will be cleared to 0 when transmission is done.

During the process of filling up packet(s) in the transmit buffer ring, current write address to TX buffer ring is mapped directly from uP's address lines during uP write to packet buffer. TWP is updated by driver only and TWP is used to be checked against TRP,BP,TLBP by both GMAC and driver to maintain TX buffer ring's integrity.

Packets between TRP and TWP will be transmitted by GMAC if TX DMA poll command is issued. TWP serves as the start page of non-ready packet(s) which is still being prepared by driver.

Condition required to begin transmission

1. Register 00h.ST1=0 and Reg00h.ST0=1 for TX local DMA mode or register 00h.ST1=1 and ST0=0 in direct FIFO mode
2. The interframe gap timer has timed out.
3. TX FIFO is filled with a complete packet or is full.
4. If a collision has been detected and backoff timer has expired.

After packet is started to go out to network, TTHD[1:0] will begin to affect packet memory's arbitration if FIFO needs more data from packet memory. (TTHD is not used in duirect FIFO mode) In the TX local DMA mode, the advantage of smaller threshold is to reduce the risk of a potential transmit FIFO underrun error. Such underrun error occurres when data in FIFO is exhausted by transmit while local DMA still has not filled in more data to be transmitted. Since TX FIFO is large enough for the largest normal packet (1518 bytes), therefore, the TTHD and FIFO underrun applied to packets larger than 1518 bytes in the TX local DMA mode. The larger the TTHD, the less aggressive the TX DMA in packet memory arbitration, therefore host and RX DMA may have more bandwidth in packet memory.

When this underrun occurres, packet will be aborted and interrupt will be asserted to get host's attention. FIFOEI (register 09h bit 5) interrupt bit will be set when underrun occures and interrupt to host is asserted if FIFOEIM bit (register 08h bit 5) is also set.

So TTHD can be tuned to improve the target system for best through put in TX local DMA mode.

Collision recovery

During transmission, if a collision is detected before the first 64 bytes of packet has been transmitted, the FIFO will restore the necessary FIFO pointers to retransmit the same packet without fetching the transmitted data from packet memory. An out-of-window collision is a collision occured after 64 bytes of data transmitted. If out-of-window collision occurred, packet will be aborted with interrupt asserted. OWC bit of transmit descriptor is set and device driver needs to resolve such situation and reissue a transmit command so that GMAC can fetch the entire packet from packet memory again for retransmission.

Collision count will be recorded for the current packet in register 04h.CC[3:0] bits. If 15 retransmission each result in a collision, the transmission is aborted and collision count CC[3:0]=1111 and an interrupt will be asserted and TEI interrupt bit is set to indicate such a excessive collision error. If TI interrupt bit is set, then packet is successfully transmitted with collision count=CC[3:0].

After single packet transmission

When a packet(s) transmission is completed, register 00h.ST1 and ST0 are both cleared to 0 automatically by GMAC. Whenever the first packet is sent out, interrupt is asserted for host's attention. Device driver can process this packet's status. In TX local DMA mode, first thing to check is making sure the OWN in the status field bit 7 is 0 which indicates that GMAC has completed the transmission of this packet and the status is valid. Or in direct FIFO mode, check ST1 and ST0 for both 0 which indicates completion of previous transmission. At this point, device driver can proceed with transmit status and other book keeping tasks.

For successful transmission, interrupt is caused by interrupt register bit TI (bit 2 of register 09h) of interrupt register IR, provided that the corresponding enable bit TIM (bit 2 of register 08h) of interrupt enable register IMR is set. In case that an error occured during the transmission, Interrupt register bit TEI will be set instead of TI. Register 09h bit 4 (TEIM) is the interrupt enable bit for TEI. Set TEIM will enable TEI interrupt. Transmission error can be read from register 04h (LTPS register) which records the transmit status of the last packet transmitted. If bit 7 (TERR) of register 04h is set then TEI will be set as well. TERR is a logical OR of underrun error(UF bit). out-of-window collision error (OWC bit), carrier lost error (CRSLOST bit) and excessive collision error (CC[3:0]=1111 and TEI = 1).

Multiple packets transmission (TX local DMA mode only)

If more packets are prepared in the packet memory and all transmit descriptors are set properly (i.e. next packet page pointer, packet length, OWN bit = 1) then a transmit command can send out all these packets in a row. As soon as the first packet transmission is done, interrupt will be asserted to get host's attention. Device driver can serve this interrupt call by processing all the packets that have OWN bit equals to zero in this multiple packets list in packet memory. Device driver can "peek" the OWN bit of next packet's descriptor to see if there are more packet(s) transmitted completely at that point. If OWN bit of next packet's descriptor is zero, then device driver can proceed to next packet after finishing the current packet. When all packets are transmitted successfully or aborted, register 00h. ST1 and ST0 bits are internally reset. This way, packets can be send out in a burst with single transmit command.

Transmit packet assembly format in packet memory

For 16 bit SRAM interface :

D15 D8	D7 D0
Descriptor Byte 1	Descriptor Byte 0
Descriptor Byte 3	Descriptor Byte 2
Destination Address Byte 1	Destination Address Byte 0
Destination Address Byte 3	Destination Address Byte 2
Destination Address Byte 5	Destination Address Byte 4
Source Address Byte 1	Source Address Byte 0
Source Address Byte 3	Source Address Byte 2
Source Address Byte 5	Source Address Byte 4
Type/Length byte 1	Type/Length byte 0
Data byte 1	Data byte 0

For 8 bit SRAM interface :

D7 D0
Descriptor Byte 0
Descriptor Byte 1
Descriptor Byte 2
Descriptor Byte 3
Destination Address Byte 0
Destination Address Byte 1
Destination Address Byte 2
Destination Address Byte 3
Destination Address Byte 4
Destination Address Byte 5
Source Address Byte 0
Source Address Byte 1
Source Address Byte 2
Source Address Byte 3
Source Address Byte 4
Source Address Byte 5
Type/Length byte 0
Type/Length byte 1
Data byte 0

Transmit descriptor format

Bit	Symbol	Description
0	CC0	Collision Count Bit 0 :
1	CC1	Collision Count Bit 1 :
2	CC2	Collision Count Bit 2 :
3	CC3	Collision Count Bit 3 : when CC[3:0] = 1111 and TEI interrupt bit is set, , then it is called excessive collision error which will abort the current packet. If TI interrupt bit is set, then CC[3:0] is the collision count and packet is transmitted successfully.
4	CRSLOST	Carrier Sense Lost : Network carrier signal was lost at some point during the transmission or lost during entire duration or transmission.
5	UF	TX FIFO underflow : TX FIFO is exhausted before TX DMA fill in more data for transmission.
6	OWC	Out of Window Collision : A collision occured after 64 bytes of data had been transmitted. This packet will be aborted.
7	OWN	Packet Buffer ownership indicator: 1: indicate GMAC has access right to current packet's buffer 0: indicate host has access right to current packet's buffer

There are 4 bytes in a descriptor structure for both transmit and receive packet. Transmit descriptor is prepared by device driver before transmitting the packet. The transmit descriptor format is defined as follows :

bit 7	bit 0
Next Packet Page Pointer (bit 7-4)	Next Packet Page Pointer (bit 3-0)
Packet Length (bit 3-0)	Next Packet Page Pointer(bit 11-8)
Packet Length (bit 11-8)	Packet Length (bit 7-4)
Transmit Status (bit 7-4)	Transmit Status (bit 3-0)

4.2 Packet Reception

The local DMA receive channel uses a receive buffer ring structure comprised of a series of contiguous fixed length 256-byte (128 word) buffers for storage of received packets. The location of this receive buffer ring is programmed in two page pointers, a Boundary Page pointer and a Receive High Boundary Page pointer. Ethernet packets consist of a distribution of shorter link control packets and longer data packets, the 256-bytes buffer length provides a good compromise between different packet sizes to best utilizing the memory. Receive buffer ring provides storage for back-to-back packets in a loaded networks. The assignment of buffers for storing packets in managed by GMAC's receive DMA logic. Three basic functions are provided by the receive DMA logic : linking receive buffers for long packets, recovery of buffers when a packet is rejected and recirculation of buffer pages that has been read by the host.

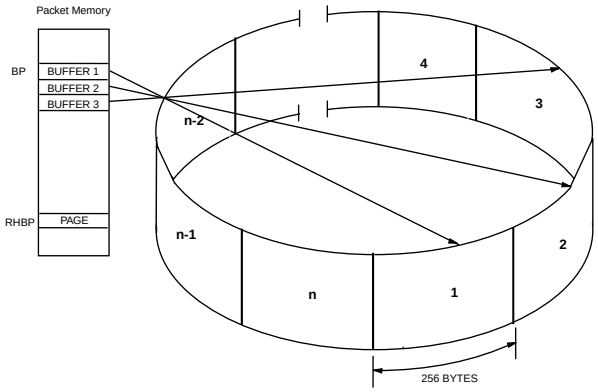


Figure 4.2.1 GMAC Receive Buffer Ring

Initialization of receive buffer ring

Two static page pointer and two working page pointers control the operation of the receive buffer ring . These are Boundary Page (BP) pointer, Receive High Boundary Page (RHBP) pointer, the Receive Read Page (RRP) pointer and Receive Write Page (RWP) pointer. BP register points to the first buffer (page) of the receive buffer ring. RHBP points to the last page of receive buffer ring. RWP register points to the page in which receive DMA logic is storing incoming network data. RRP register points to the page from which host will read next network data. A receive descriptor structure is located at the beginning of the start page of a received packet. If GMAC ever reach the page pointed by RHBP register, it will link the page pointed by BP register as next page, thus forms a "ring" buffer structure.

The size of receive buffer ring is the total buffer space between BP and RHBP register. An internal 8 bit byte counter accounts for MA[7:0] will be used with RWP register to form a physical memory address during receive DMA write operation. This internal 8 bit counter will tracks the actual location within a page. After GMAC is initialized, BP, RWP and RRP should all points to the same page. These registers must be properly initialized before setting NCRA's (register 00h) SR (bit 3) bit to one which enables the receive channel for DMA function.

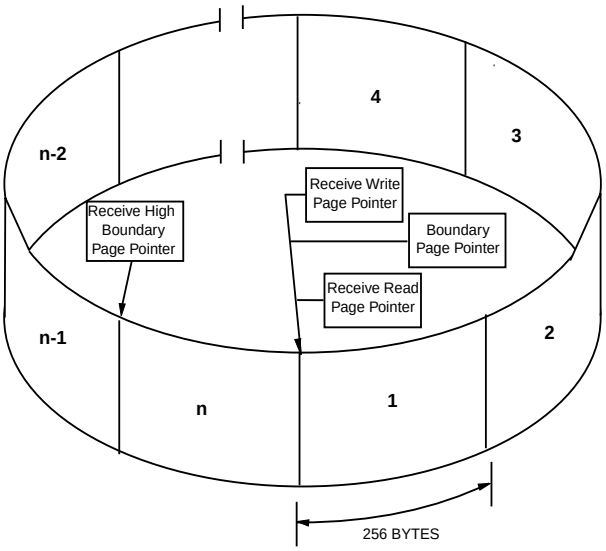


Figure 4.2.2 GMAC Receive Buffer Ring at Initialization

Beginning of reception

After all four page pointers are properly set by device driver (host), register bit NCRA.SR bit can be set to enable reception of packets. When the first packet begins arriving the GMAC begins storing packet at the location pointed to by the RWP register. An offset of 4 bytes (descriptor) is saved in this first page to store receive status corresponding to this packet. Whenever internal byte counter reaches FFh indicating end of a page, RWP will be incremented by 1 automatically if more data is arriving for this packet.

The incoming network address is examined by GMAC to determine whether to accept or reject. If GMAC decided to reject the packet, then receive FIFO will be restored and so is the buffer used. If packet should be accepted and FIFO contains data up to a threshold level which can be programmed by RTHD[1:0] (register 33h bit [3:2]). The smaller the threshold, the earlier the receive DMA logic removing data from FIFO, thus may has lower risk in running into a FIFO overflow situation. The disadvantage of a smaller threshold is that host and transmit channel may be less efficient. So threshold should be chosen to tune for best network throughput. Default value of receive FIFO threshold is 00 meaning 50% of the FIFO is filled up before any receive local DMA can start removing data out of FIFO.

Linking receive buffer pages

If packet length exhausts the first 256-bytes buffer, receive DMA logic will performs a forward link to the next buffer to store the remainder of the packet. A maximum length packet , up to 6 buffers can be linked together. Buffers can not be skipped when linking, therefore a packet will always be stored in contiguous buffers. Before the next page can be linked, receive DMA logic does two comparisons.

The first comparison tests the equality between content of RWP register + 1 and content of RRP register. If equal, the reception is aborted. This is called receive buffer full error. Second comparison tests the equality between RWP register and RHBP register. If equal, the receive DMA will restore RWP to the first buffer in the receive buffer ring pointed by BP register if receive buffer ring is not full.

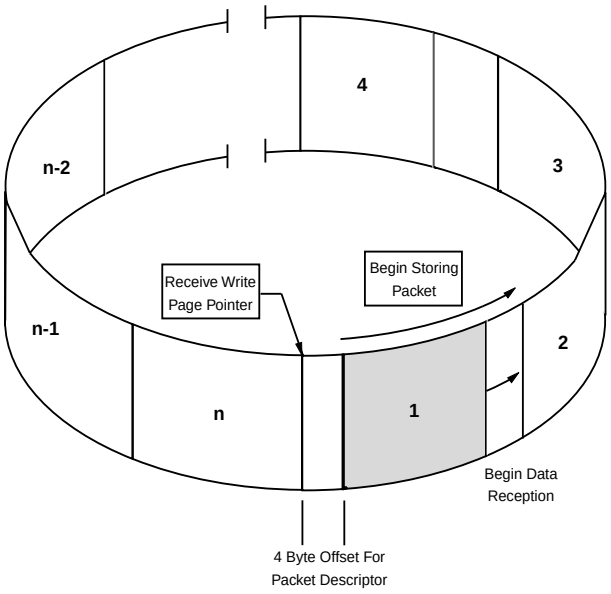


Figure 4.2.3 Received Packet Enters the Receive Buffer Pages

Receive buffer ring full

In a heavily loaded network which may cause overflow of the receive buffer ring, when the last available page is exhausted and more data needs to be stored for the current packet then the receive buffer ring is full but GMAC will continue receiving until RX FIFO is also overflow. At this point, GMAC will do the following actions :

1. Close current received packet with the FO bit (bit 3) and the BF bit (bit 0) of the receive descriptor being set if a minimum of one page is used by this packet.

2. An interrupt may be asserted if the RBFI (register 09h bit 7) interrupt bit is set and the RBFIM bit (register 08h bit 7) is also set.

3. If AUTORCVR is reset, then GMAC can not receive any more packet. All following packets will be lost and MPC (Missed Packet Counter), registers 07h and 06h, will be increment automatically. MPC can be reset by the device driver.

The following procedure is required for device driver to recover from such error situation.

1. Issue the SR=0 (NCRA register bit 3) which will stop RX channel to prevent new data from coming into RX FIFO.

2. Issue RX FIFORST to clean RX FIFO.

3. Remove all the received packets in the packet memory. When buffer ring is empty, RRP=RWP.

4. Clear all receive related interrupt flags and then set the SR bit=1 to resume the receive operation.

Successful reception

Based on the network address filtering modes set up by the device driver, GMAC will determine whether to receive a packet or to reject it. It either branches to a routine to store the packet or to another routine to reclaim the buffers used to store packet. If a packet is successfully received, GMAC will store the receive status, packet length and next packet pointer in the receive descriptor located at the beginning of the first page of the packet and status in LRPS (register 05h) register. Note that the remaining bytes in the last page are discarded and reception of the next packet begins on the next empty 256-byte page boundary. The RWP is then set by GMAC to the next available page in the buffer ring.

Rejected packets

If the packet is a runt packet and PB bit (Pass Bad option, register 01h, bit 3) is reset then it is rejected. The buffer previously used by this rejected packet is reclaimed by resetting the internal byte counter to zero automatically by GMAC. Packet with at least 64 bytes are always received and stored regardless of CRC error status.

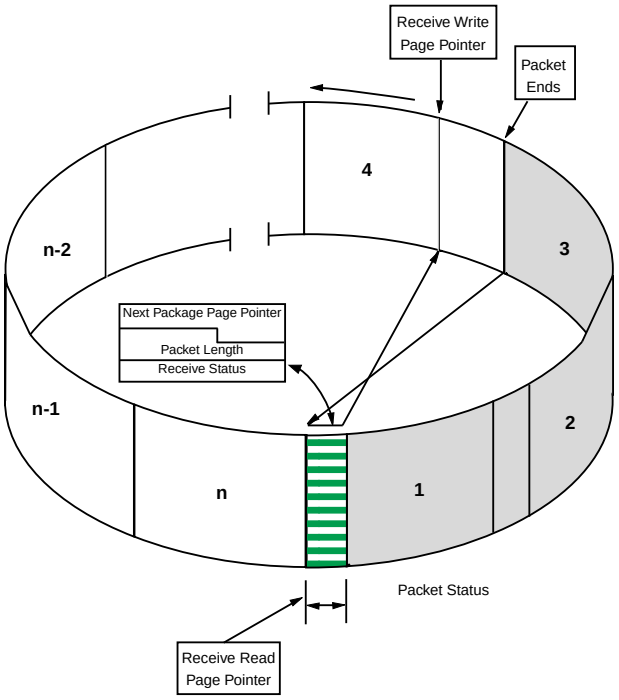


Figure 4.2.4 Termination Of Received Packet-Packet Accepted

Removing packets from the buffer ring

Packets are removed from the ring by the host using the direct host DMA. The actual packet memory address during host DMA is mapped directly from uP address lines. i.e. Host has to control all the addresses during the packet buffer accesses directly. By reading the descriptor device driver will know the size of packet and it can move data up to the last page without updating RRP register. The RRP register will be updated by driver only whenever a packet has been removed. Driver must properly update RRP to next available page, especially if RHBP page is exhausted. in this case, next page should be wrapped around to the beginning (pointed by BP register) of RX buffer ring.

Host page registers RRP and TWP are maintained by driver only. It is recommended that only when a packet has been removed from RX buffer ring, RRP is then incremented by driver so that GMAC will not overwrite a page which belongs to an unprocessed packet. The following is a suggested method for maintaining the receive buffer ring pointer :

1. At initialization, set up BP= RRP=RWP and RHBP to a higher memory page. At the point, receive buffer is empty.

2. Set a software address counter and byte counter, byte counter's LSB byte is reset. The MSB bits [19:8] of the address counter will start from current RRP register, and keeping track of current page, once a packet is removed, then RRP register is updated to next page location.

3. After a packet is stored in the receive buffer ring, GMAC issue interrupt. Device driver will start moving data beginning from the page pointed by RRP register. Reads the packet length and advanced the address counter as the host DMA goes along. Care should be taken if manual page pointer update is used when RHBP page is exhausted or buffer is full.

Receive packet assembly format in packet memory

For 16 bit SRAM interface :

D15 D8	D7 D0
Descriptor Byte 1	Descriptor Byte 0
Descriptor Byte 3	Descriptor Byte 2
Destination Address Byte 1	Destination Address Byte 0
Destination Address Byte 3	Destination Address Byte 2
Destination Address Byte 5	Destination Address Byte 4
Source Address Byte 1	Source Address Byte 0
Source Address Byte 3	Source Address Byte 2
Source Address Byte 5	Source Address Byte 4
Type/Length byte 1	Type/Length byte 0
Data byte 1	Data byte 0

For 8 bit SRAM interface :

D7 D0
Descriptor Byte 0
Descriptor Byte 1
Descriptor Byte 2
Descriptor Byte 3
Destination Address Byte 0
Destination Address Byte 1
Destination Address Byte 2
Destination Address Byte 3
Destination Address Byte 4
Destination Address Byte 5
Source Address Byte 0
Source Address Byte 1
Source Address Byte 2
Source Address Byte 3
Source Address Byte 4
Source Address Byte 5
Type/Length byte 0
Type/Length byte 1
Data byte 0

Receive status in descriptior

PIN#	Symbol	Description
0	BF	RX Packet Buffer Full Error : 1 indicates RX packet buffer is full.
1	CRC	CRC error : caused by corrupted data or dribble byte (s).
2	FAE	Frame Alignment Error : Dribble nibble (s), FAE error might not cause CRC error (e.g. only a dribble nibble is detected by GMAC). FAE error will not set RERR bit.
3	FO	FIFO overrun
4	RW	Receive Watchdog : Set to indicate the frame length exceeds 2048 bytes.
5	MF	Multicast address : Set to indicate current frame has multicast address.
6	RF	Runt Frame : Set to indicate a frame length less than 64 bytes, only meaningful when Reg00h.4 (PB bit)=1 is set.
7	RERR	Receive Error : a logical OR of CRC, FO, BF, RW, RF bit.

There are 4 bytes in a descriptor structure for both transmit and receive packet. Transmit descriptor is prepared by device driver before transmitting the packet. The transmit descriptor format is defined as follows :

bit 7	bit 0
Next Packet Page Pointer (bit 7-4)	Next Packet Page Pointer (bit 3-0)
Packet Length (bit 3-0)	Next Packet Page Pointer(bit 11-8)
Packet Length (bit 11-8)	Packet Length (bit 7-4)
Transmit Status (bit 7-4)	Transmit Status (bit 3-0)

4.3 Packet Structure and 802.3 conformance

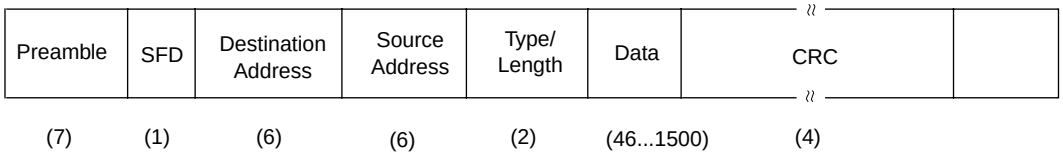
Network speed may be 10 MBPS or 100 MBPS mode. Further more, GMAC supports full duplex mode where transmit and receive process are running independently. A typical Ethernet frame structure is shown below.

Ethernet and IEEE 802.3 Frames

An Ethernet frame format consists of the following:

Field	Description
Preamble	A 7-byte field of 56 alternating 1s and 0s, beginning with a 0.
SFD	A 1-byte field that contains the value 10101011; the MSB is transmitted and received first.
Destination	A 6-byte field that contains the specific station address, the broadcast address. or a multicast address where this frame is directed.
Source	A 6-byte field that contains the specific station address where this frame was sent.
Type/Length	A 2-byte field that indicates whether the frame is in IEEE 802.3 format or Ethernet format. A field greater than 1500 is interpreted as a type field, which defines the type of protocol of the frame. A field smaller than or equal to 1500 is interpreted as a length field, which indi -cates the No. of data bytes in the frame.
Data	A data field consists of 46 to 1500 bytes that is fully transparent. A data field shorter than 46 bytes is allowed, unless padding is disabled (TDES1<23>).
CRC	A frame check sequence is a 32-bit cyclic redundancy check (CRC) value that is computed as a function of the destination address field, source address field, type field and data field. The FCS is appended to each transmitted frame, and used at reception to determine if the receive frame is valid.The figure shows the Ethernet frame format.

Ethernet Frame Format



*Numbers in parentheses indicate field length in bytes.

The CRC polynomial, as specified in the Ethernet specification, is as follows:

$$FCS(X) = X^{31} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X^1 + 1$$

The 32 bits of the CRC value are placed in the FCS field so that the X^{31} term is the right-most bit of the first octet, and the X^0 term is the left-most bit of the last octet. The bits of the CRC are thus transmitted in the order $X^{31}, X^{30}, \ldots X^1, X^0$.

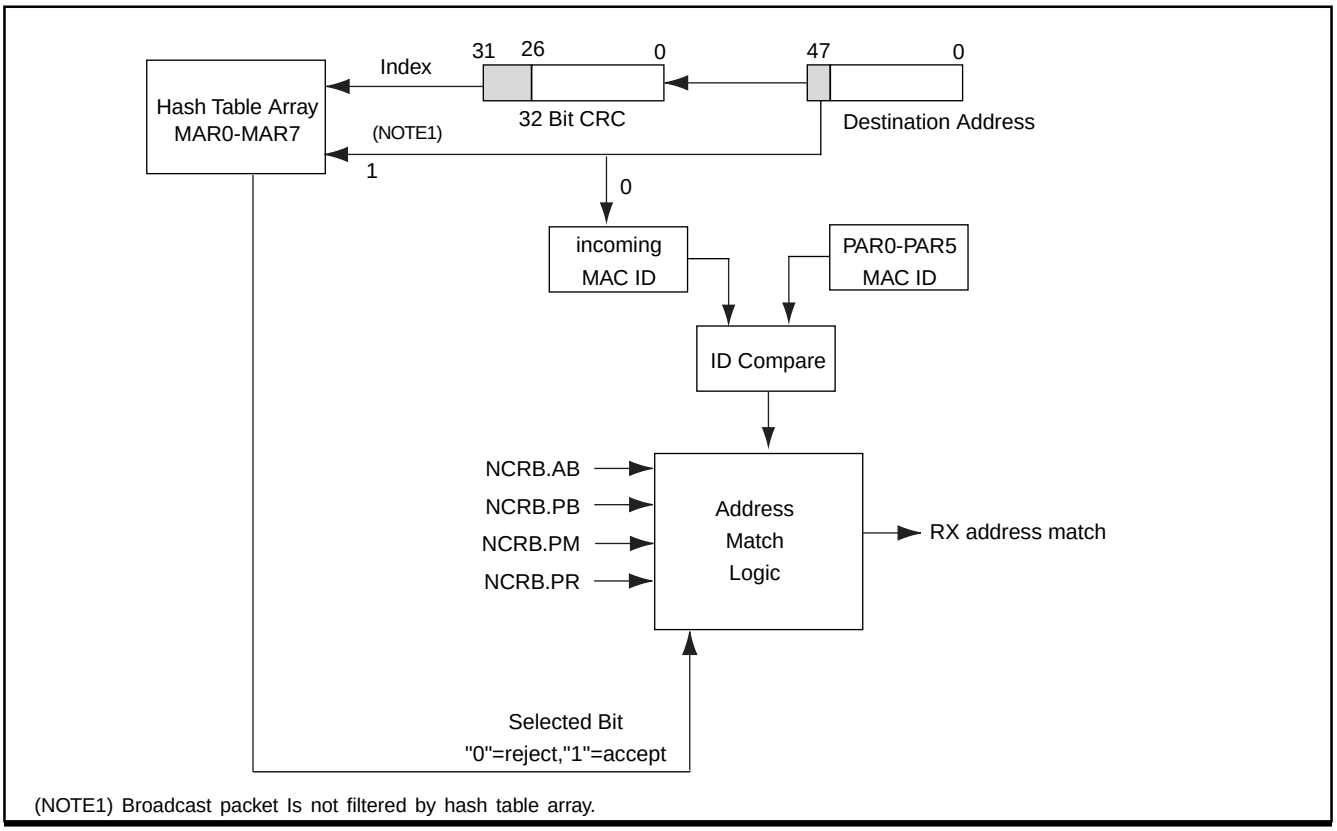
4.4 Network Address Filtering

The first bit of the destination address signifies whether it is a physical address or a multicast address. The receive MAC filters the frame based on the address filtering option described below. Register 01h (NCRB) bit 0 is PR (Promiscuous mode) and bit 2 is PM (Pass Multicast) are used to control the desired address filtering options. Possible Address Filtering Options (all independent of each other options)

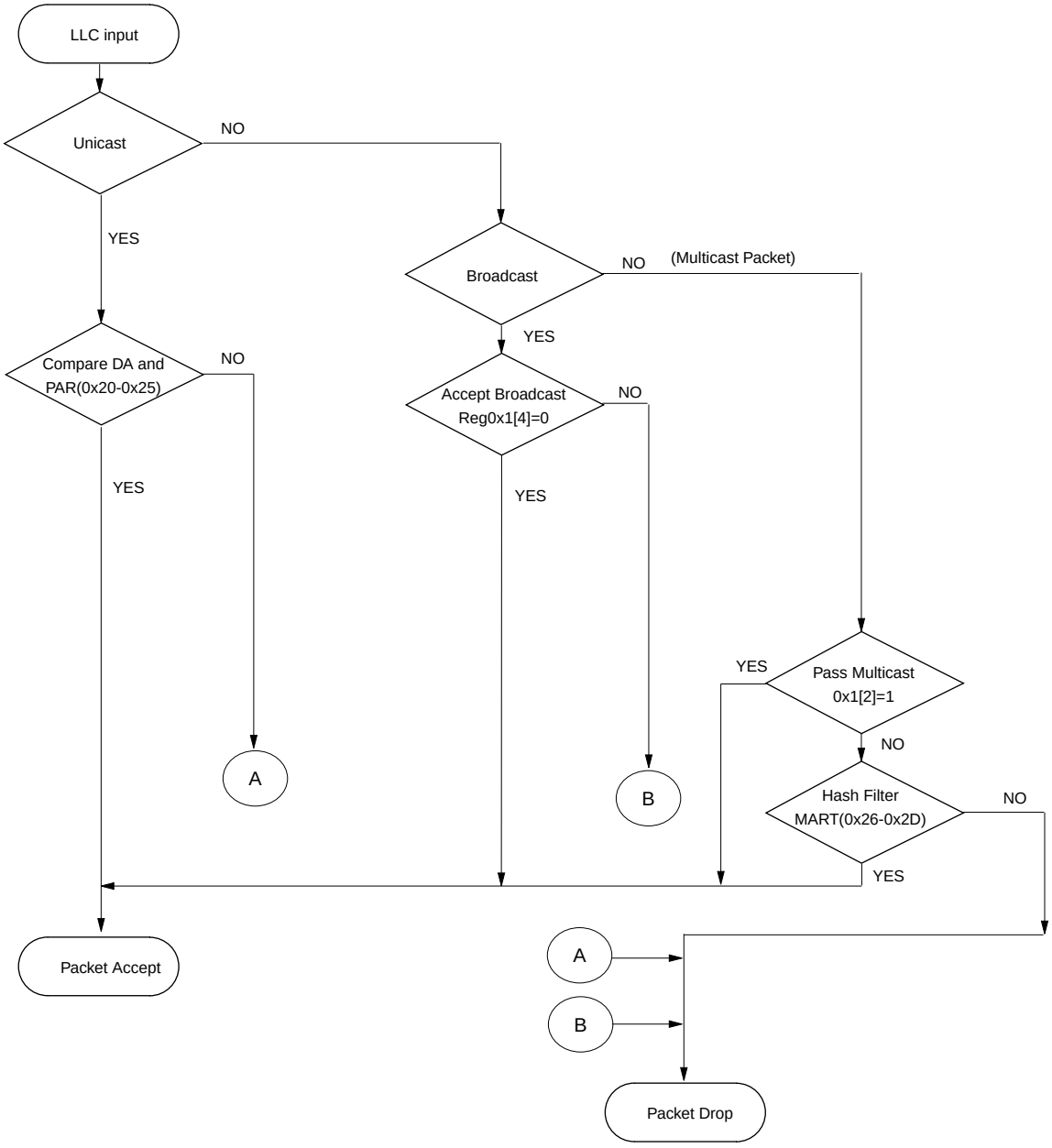
option	Description
1	One physical address perfect filtering , always enabled
2	Unlimited multicast addresses imperfect filtering using hash table.
3	Pass all multicast address
4	Promiscuous Ethernet reception, when set, all valid frames are reecived

If the frame address passes the network address filter, the receive MAC removes the preamble and delivers the frame to the host processor memory. However, if the address does not pass the filter when mismatch is recognized, the receive MAC terminates this reception.

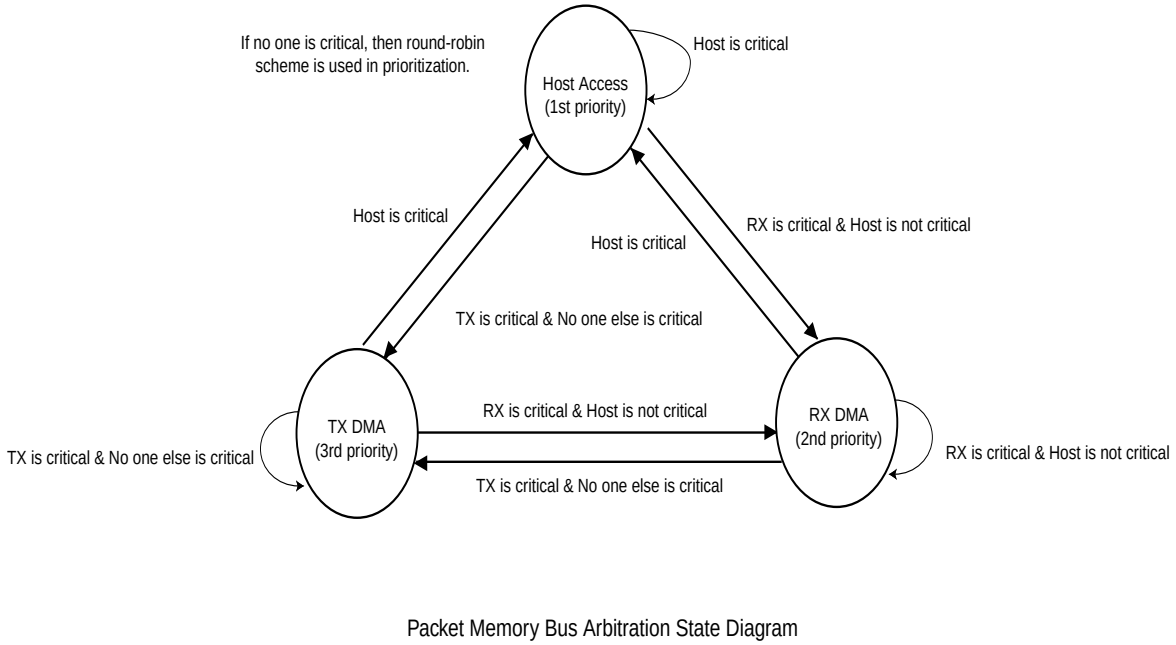
GMAC Network Address Filtering



GMAC's Network Address Filtering Flow Chart



5.0 Host/Local DMAs and packet memory bus arbitration



Packet Memory Bus Arbitration State Diagram

Rules of packet memory access prioritization

rule 1: TX local DMA is said to be "critical" if TX FIFO counter fall below TTHD level. If TX packet is in "stored and forward" mode (TTHD[1:0]=11), then TX local DMA is never critical.

rule 2 : RX local DMA is said to be "critical" if RX FIFO counter rise above RTHD level.

rule 3 : Host access is said to be "critical" if DINTVAL timer is time out.

rule 4 : If all three accesses are critical, then Host has 1st priority, RX local DMA has 2nd priority and TX local DMA has last priority. If no one is critical, then round-robin is used.

5.1 Host DMA

The Host DMA channel is used to both assemble packets for transmission, and to remove received packets from the receive buffer ring . Two registers RRP and TWP are used to control host DMA. The physical address of these DMA are formed by the following rules

For 188/186 modes, HLDA must be 0 during host DMA cycles (HLDA=0 will disable local DMA temporarily). Two Page pointers (RRP, TWP) are to be maintained by host for all host DMA (packets accesses).

Host write

Host write to packet memory is used to prepare a packet for transmission. TWP register is used for addressing the page address of the physical buffer. Update of TWP can only be done by driver. HLDA must be low whenever the host DMA is running. SRDY is used to insert wait states so that local DMA will finish at least one on-chip FIFO burst transfer before host can complete current access cycle to packet buffer.

Host Read

Host read to packet memory is used to remove a packet for receive buffer ring. RRP register is used for addressing the page address of the physical buffer. Update of RRP can only be done by driver. Again, HLDA must be low whenever the host DMA is running. SRDY is used to insert wait states so that local DMA will finish at least one on-chip FIFO burst transfer before host can complete current access cycle to packet buffer.

5.2 Local DMA

Receive FIFO threshold of Receive DMA

Receive FIFO threshold is defined by register 33h bit [3:2] (RTHD[1:0]) is used to control the aggressiveness of receive DMA request in packet memory bus arbitration operation. e.g. default value of RTHD=1/2 the depth of receive FIFO which means whenever the content of FIFO is over 1/2 of FIFO space (it is "critical" since FIFO may soon be full or overrun), when receive FIFO is "critical" then receive DMA will have higher priority over transmit DMA (regardless of whether transmit FIFO is critical or not). If FIFO is not over RTHD level, it is not critical, then transmit DMA may have equal priority as receive DMA or higher priority over receive DMA if transmit FIFO is critical. The larger the receive threshold, the less aggressive the receive DMA because it takes more time for receive DMA to become critical but it also presents a higher risk to become FIFO full or overrun the FIFO space. The smaller the RTHD, the more aggressive the receive DMA is and less risk in running into a FIFO full condition, but it also blocks other access from host and transmit DMA. Since packet memory bandwidth is shared by host, transmit DmA and receive DMA, "tuning" RTHD threshold may be necessary for a best network/system throughput.

Receive FIFO burst length of Receive DMA

Receive FIFO burst length is defined by register 33h bit [7:6] (RBLEN [1:0]) which control the number of data transfers within each and every receive DMA cycle. e.g. dufault receive burst length is 4 which means there will be exactly 4 bytes (or 4 words) transferred in each receive DMA cycle. The larger the RBLEN, the more efficient the receive DMA transfer but it also cause transmit DMA and host DMA to wait more time for packet memory bus release for new access. Tuning receive FIFO burst length may be necessary for a best network/system throughput.

Receive DMA

Receive DMA normally has higher priority over host and transmit DMA. This is due to the receive data can not be reproduced locally, therefore it is more urgent than others. Once receive DMA is granted an access to packet memory, receive DMA conducts a burst write whose length is defined by register 33h bit [7:6] (PBLEN [1:0]). Only when current receive burst transfer is done, arbitrator will release the packet memory bus to next requester.

The physical address of receive DMA is formed by cascading a page address RWP register and an internal byte counter for receive DMA. RWP [11:0] is mapped to MA[19:8] while the internal byte counter is mapped to MA[7:0]. Thus a 20 bit MA is derived. RWP will be automatically updated by GMAC whenever a page is exhausted. If RHBP is exhausted, GMAC will link BP as the next available page into RWP if the BP page is free, otherwise a receive buffer full error occures.

Transmit FIFO threshold of transmit DMA

Transmit FIFO threshold is defined by Register 33h bit [1:0] (TTHD [1:0]). TTHD is used to control the aggressiveness of transmit DMA request in packet memory bus arbitration. e.g. default value of TTHD=1/2 the depth of transmit FIFO which means whenever the content of FIFO falls below 1/2 of FIFO space, the transmit DMA will have higher prority over receive DMA (if receive FIFO is not critical). If transmit FIFO is over TTHD level, then transmit may have equal priority as receive DMA or lower priority to receive DMA (if receive FIFO is critical). The larger the TTHD threshold, the less aggressive the transmit DMA because it takes more time for transmit DMA to become critical of running empty. The small TTHD will result in more aggressive transmit DMA but then it it also more critical, i.e. it takes less time to run transmit FIFO to empty ("underrun error). Since packet memory bandwidth is shared by host, transmit DMA and receive DMA, "tuning" TTHD may be necessary for a best network/system throughput.

Transmit FIFO burst length of transmit DMA

Transmit FIFO burst length is defined by register 33h bit [5:4] (TBLEN [1:0]) which control the number of data transfers within each transmit DMA cycle. e.g. default transmit burst length is 4 which means there will be exactly 4 bytes (or 4 words) transferred in each transmit DMA cycle. The larger the TBLEN, the more efficient the transmit DMA cycle but it also cause transmit DMA and host DMA to wait more time for a packet memory bus release for new access. "Tuning" TBLEN may be necessary for a best network/system throughput.

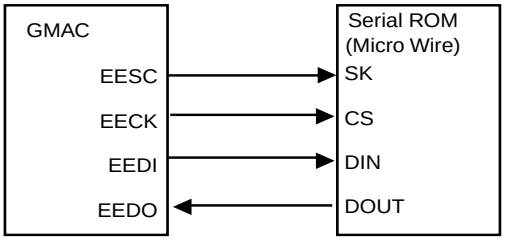
Transmit DMA

Transmit DMA normally has higher priority over host but lower than receive DMA. Once a transmit DMA is granted the access to packet memory, transmit DMA conducts a burst read which is defined by TBLEN [1:0]. Only when current burst transfer is done, arbitrator will release the packet memory bus to next requester.

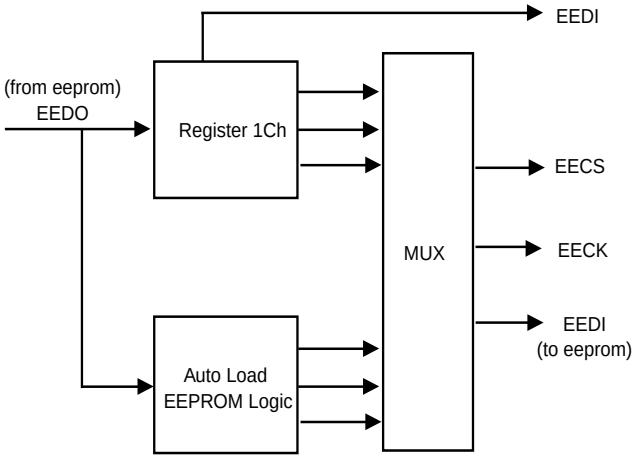
The physical address of transmit DMA is formed by cascading a page address TRP register and an internal byte counter for receive DMA. RWP [11:0] is mapped to MA[19:8] while the internal byte counter is mapped to MA[7:0]. Thus a 20 bit MA bus is derived. TRP will be automatically updated by GMAC whenever a page is exhausted. If RHBP page is exhausted, GMAC will link BP page as the next available page into TRP if the BP page is free.

6.0 Serial ROM (EEPROM) Interface

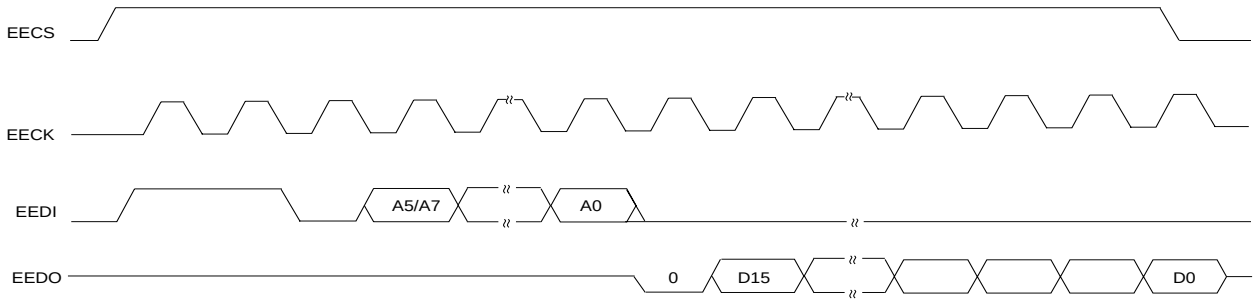
Serial ROM Connection



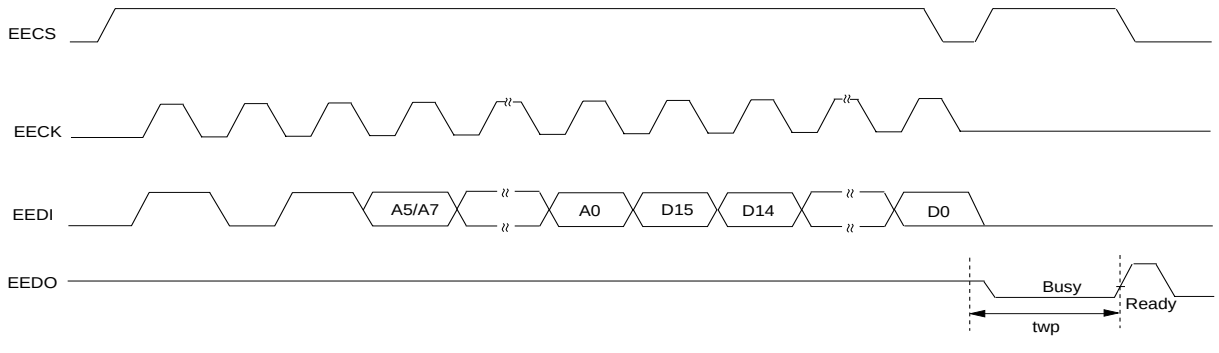
EEDI - Serial ROM (EEPROM) Data In = register 1Ch, bit2
EECK - Serial ROM (EEPROM) Serial Clock = register 1Ch, bit 1
EECS - Serial ROM (EEPROM) Chip Select = register 1Ch, bit 0
EESEL - must be set to enable EEPROM access by register 1Ch, bit 4



Serial ROM Interface Block Diagram



EEPROM Read Cycle



EEPROM Write Cycle

Autoload Function

The Autoload Function is executed only once after hardware reset (pin RSTB from low to high). At that time the Serial ROM interface is controller by GMAC to load the data from Serial ROM into GMAC.

EEPROM Content (suggested)

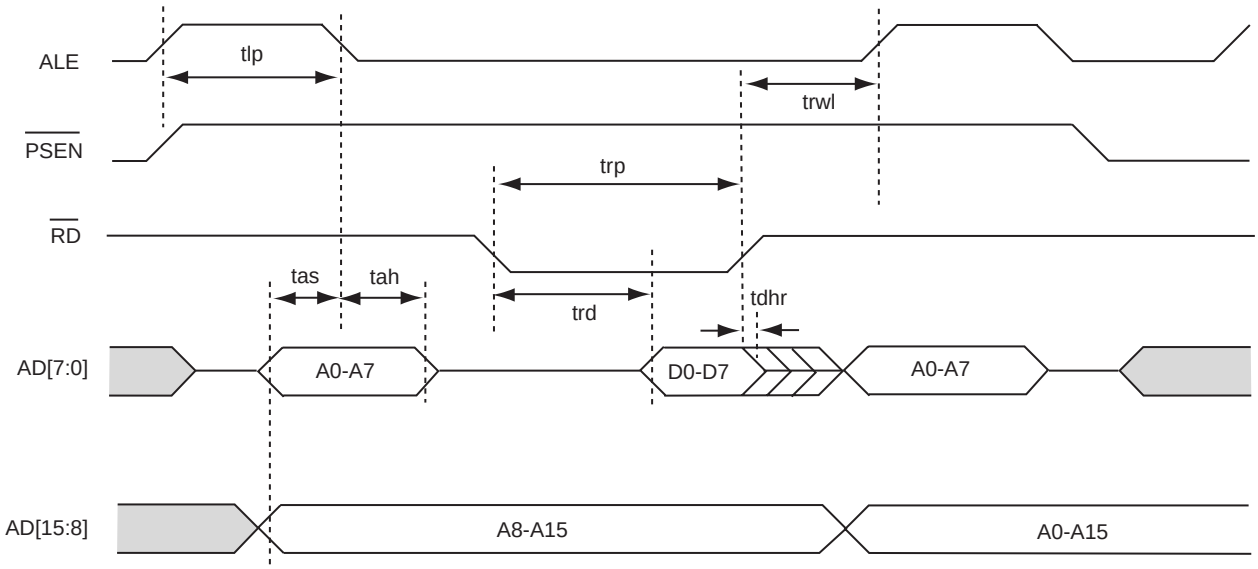
Location	Content
00H	Physical Address Byte 0 : PAR[7:0] (MSB)
01H	Physical Address Byte 1: PAR[15:8]
02H	Physical Address Byte 2 : PAR[23:16]
03H	Physical Address Byte 3 : PAR[31:24]
04H	Physical Address Byte 4 : PAR[39:32]
05H	Physical Address Byte 5 : PAR[47:40]
06H	GMAC Configuration A Register : GCA[7:0] bit 0 : BPSCRM bit 1 : PBW bit 2 : SLOWSRAM bit 3 : ARXERRB bit 4 : MIISEL bit 5 : AUTOPUB bit 6 : TXFIFOCNTEN bit 7 : reserved
07H	reserved
08H-END	Reserved for Software application

6.1 On-Chip Transceiver vs MII Interface

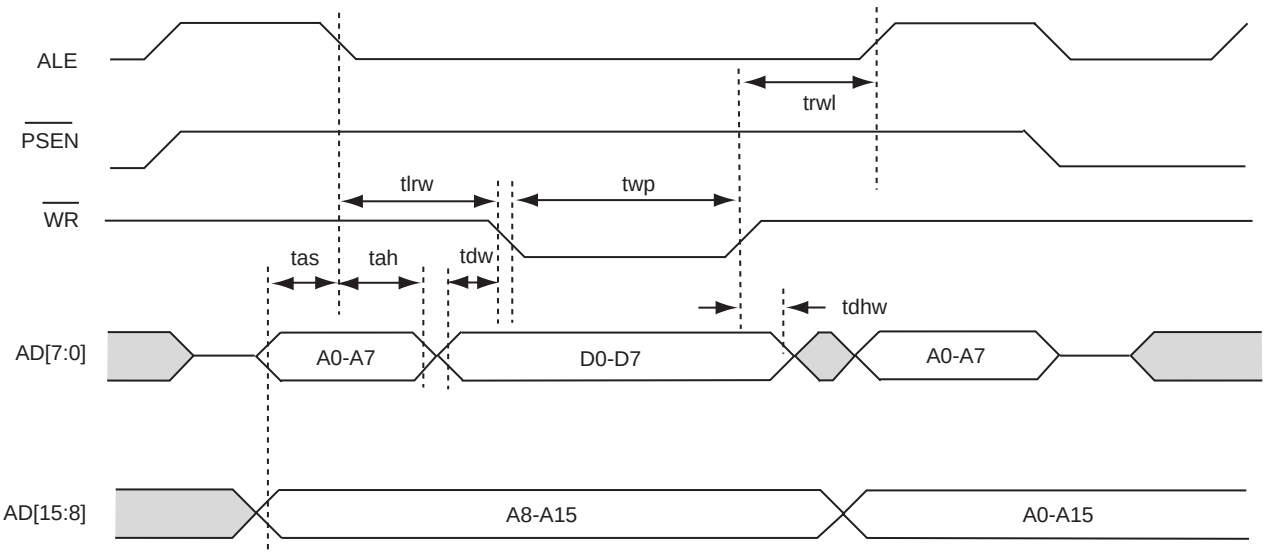
After system reset, GMAC enter its normal mode in which on chip 10/100 fast Ethernet tranceiver is used and immediately Nway auto negotiation will start setting up link in the network. The option of using a 3rd party tranceiver, such as 10/100 fast Ethernet tranceiver or HomePNA tranceiver is possible through the MII (Media Independent Interface) interface. Even if both fast Ethernet connection and HomePNA connection are desired, GMAC can allow user to switch between these two connection through register setup.
When MII mode is chosen, both Nway and on chip tranceiver are isolated from the internal MAC logic, so all data are from and to through the MII interface.

7.0 Timing Diagram and AC specification

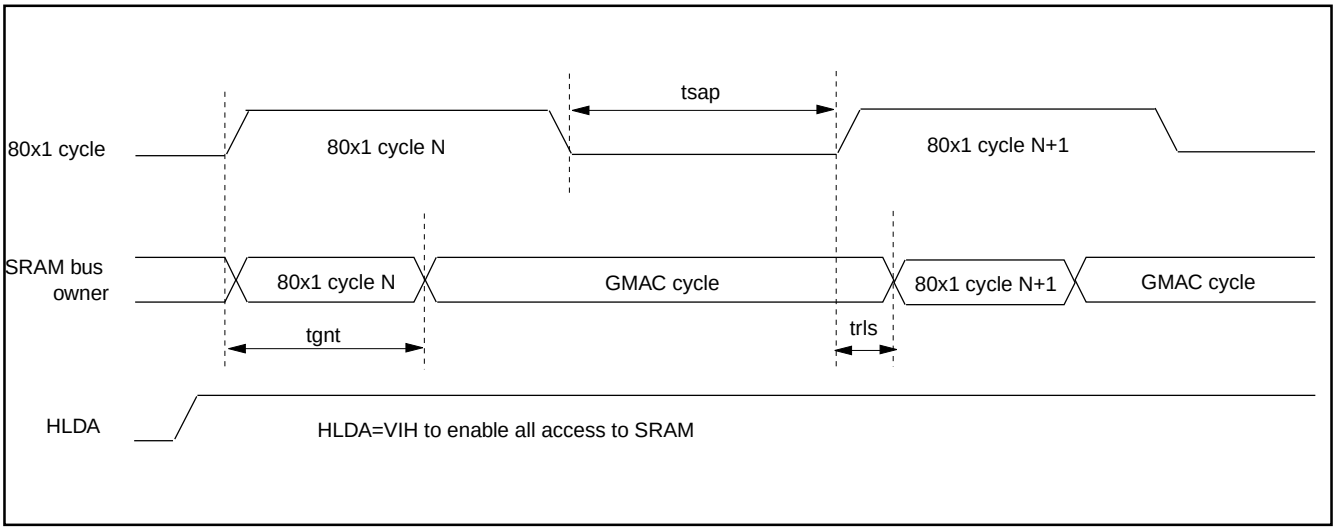
SYMBOL	PARAMETER	12MHZ		16MHZ		24MHZ		40MHZ		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tlp	Ale pulse duration	25	-	25	-	25	-	25	-	ns
tas	Address set-up time to ale	3	-	3	-	3	-	3	-	ns
tah	Address hold time after ale	5	-	5	-	5	-	5	-	ns
trp	RD pulse duration	38	-	38	-	38	-	38	-	ns
twp	WR pulse duration	38	-	38	-	38	-	38	-	ns
trd	RD to valid data input	-	20	-	20	-	20	-	20	ns
tdhr	Data hold time after RD	0	-	0	-	0	-	0	-	ns
tlrw	Time from ale to RD or WR	50	-	50	-	50	-	50	-	ns
trwl	Time from RD or WR high to ale high	10	-	10	-	10	-	10	-	ns
tdw	Data valid to WR transition	5	-	5	-	5	-	5	-	ns
tdhw	Data hold time after WR	0	-	0	-	0	-	0	-	ns



MX98726EC MEMORY READ CYCLE IN 80x1 MODE

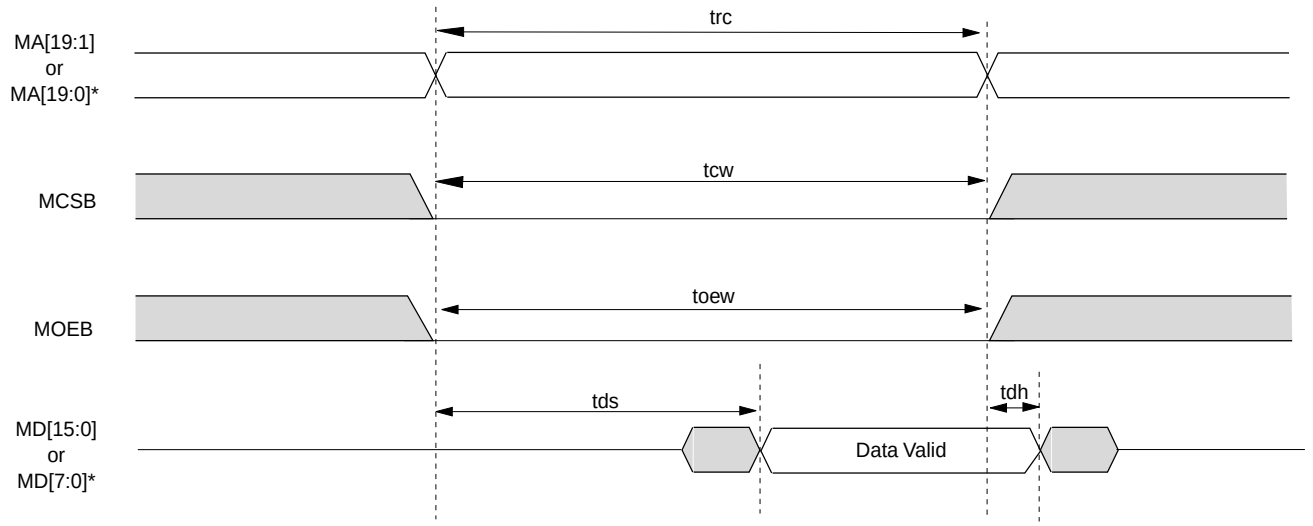


MX98726EC MEMORY WRITE CYCLE IN 80x1 MODE



SYMBOL	PARAMETER	MIN.	MAX.	UNIT
tgap	80x1 cycle recovery time	300		ns
tgnt	GMAC grant valid delay		8	TCLK
tris	GMAC grant release delay		4	TCLK

TCLK=Internal clock running at 50MHz



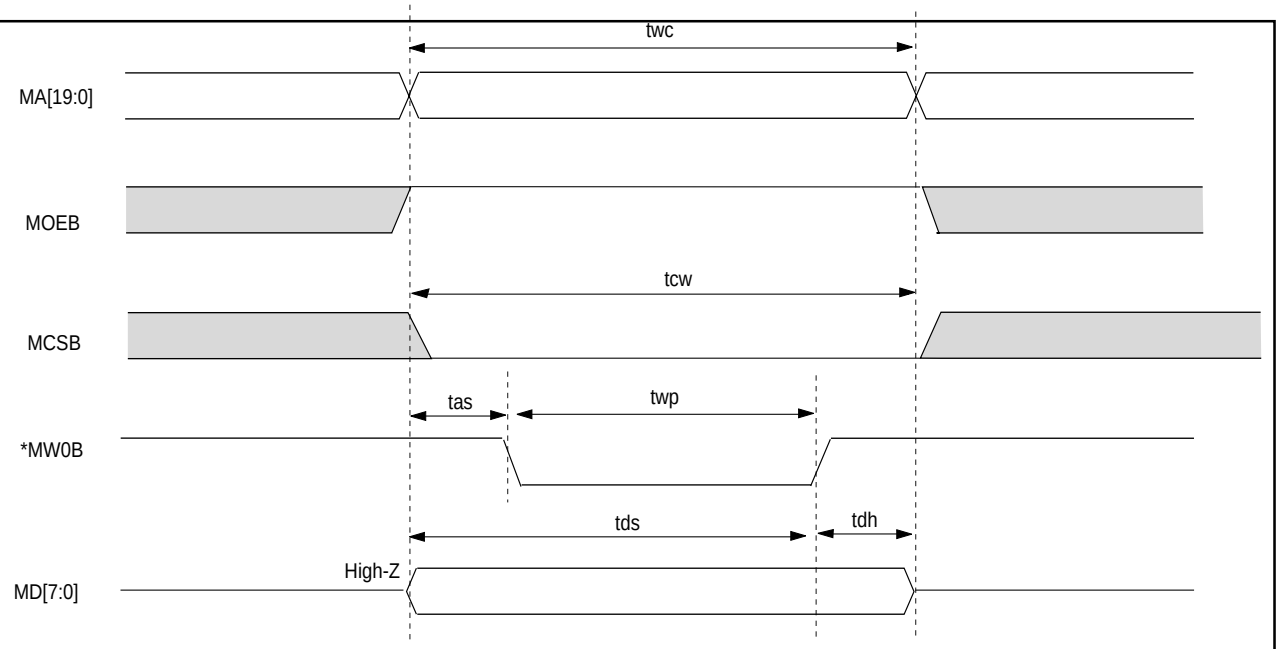
16/8 BIT PACKET MEMORY READ CYCLE

* 8-bit packet memory

READ CYCLE

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read Cycle Time	trc	35	40	ns
Chip Select Pulse Width	tcw	35	40	ns
Output Enable Pulse Width	toew	35	40	ns
Data Hold from Address Change	tdh	-0	-	ns
Data Valid Delay From Address Change	tds	-	25	ns

Note : MA[19:0], MOEB, MCSB are asserted at the same internal clock edge.



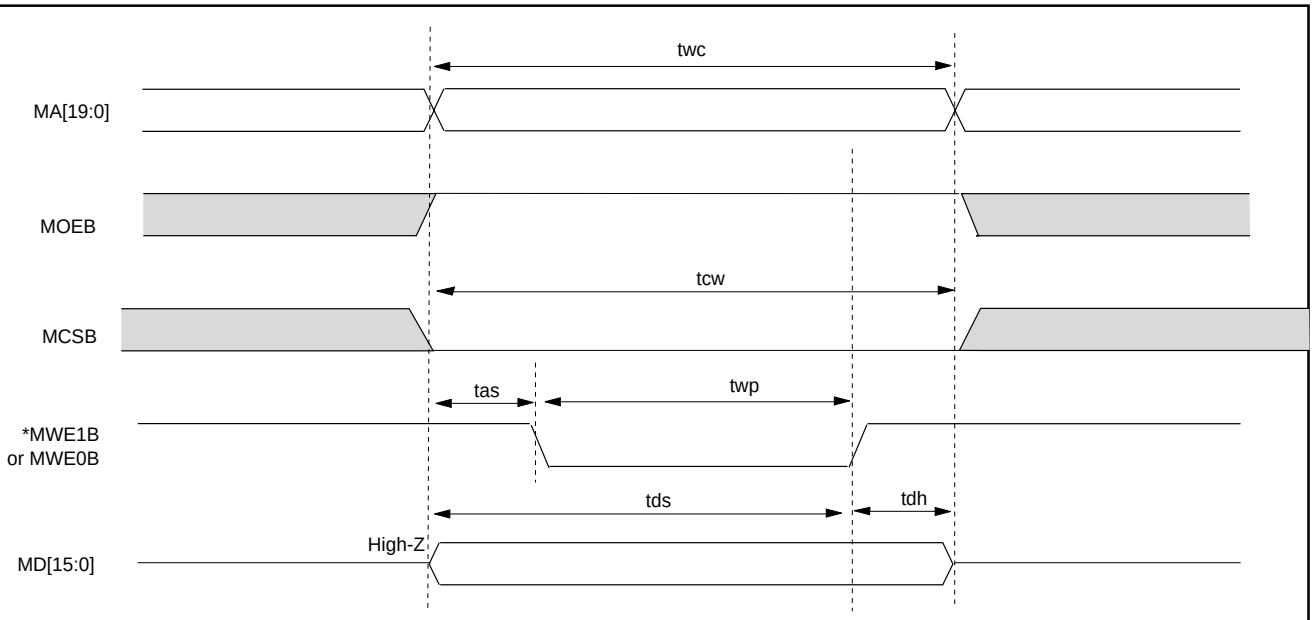
* In byte mode, only MWE0B is used.

8 BIT PACKET MEMORY WRITE CYCLE

WRITE CYCLE

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write Cycle Time	twc	35	40	ns
Chip Select Pulse Wdith	tcw	35	40	ns
Address Set-up Time	tas	5	-	ns
Write Pulse Width (OE-High)	twp	18	-	ns
Data Setup To Write Rising Edge	tds	25	28	ns
Data Hold from MWEB Deassertion	tdh	10	-	ns

Note : MA[19:0], MOEB, MCSB are asserted at the same internal clock edge.



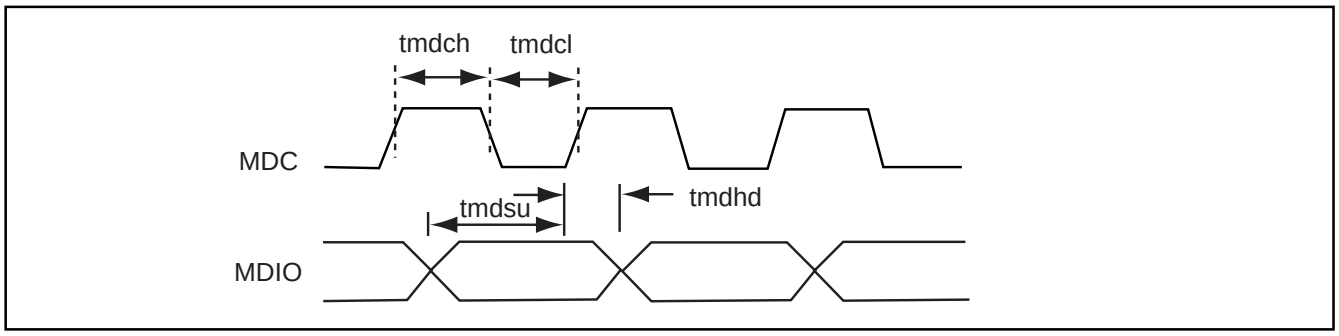
16 BIT PACKET MEMORY WRITE CYCLE

WRITE CYCLE

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write Cycle Time	twc	35	40	ns
Chip Select Pulse Wdith	tcw	35	40	ns
Address Set-up Time	tas	5	-	ns
Write Pulse Width (OE-High)	twp	18	-	ns
Data Setup To Write Rising Edge	tds	25	28	ns
Data Hold from MWEB Deassertion	tdh	10	-	ns

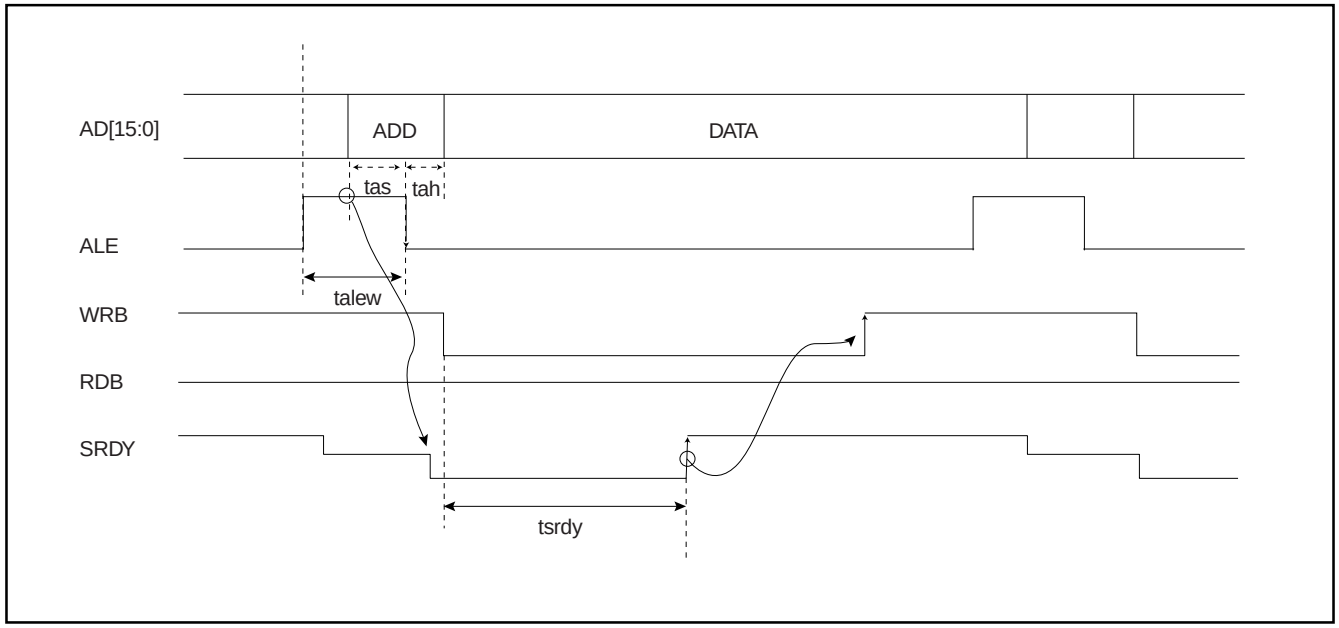
Note : MA[19:0], MOEB, MCSB are asserted at the same internal clock edge.

MII management signal MDIO timing :



Symbol	Parameter	Min	Max	Units
tmdch	MDC high time	200		ns
tmdcl	MDC low time	200		ns
tmdsu	MDIO to MDC high setup time	10		ns
tmdhd	MDIO to MDC high hold time	10		ns

Host Interface timing in 8018X mode :



Symbol	Parameter	Min	Max	Units
tas	Address setup time for ALE	5		ns
tah	Address hold time for ALE	3		ns
tsrdy	SRDY valid delay	45	65	ns
talew	ALE pulse width	25		ns

8.0 DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Units
TTL/PCI Input/Output					
Voh	Minimum High Level Output Voltage	Ioh=-4mA	2.4		V
Vol	Maximum Low Level Output Voltage	Iol=+4mA		0.4	V
Vih	Minimum High Level Input Voltage		2.0		V
Vil	Maximum Low Level Input Voltage			0.8	V
Iin	Input leakage current (No pull-up or pull-down)	Vin=VCC or GND	-1.0	+1.0	uA
Iin(pull-up)	Input leakage current with Internal pull-up	Vin=VCC or GND	-20uA	-70uA	
Iin(pull-down)	Input leakage cruuent with Internal pull-down	Vin=VCC or GND	+20uA	+70uA	
Ioz	Minimum Tri-state Output Leakage Current	Vout=VCC or GND	-10	+10	uA
LED Output Driver					
Vled	LED turn on Output Voltage	Iol=16mA		0.4	V
Idd	Average Supply Current	CKREF=25MHz	160	230	mA
Ianalog	Average Analog Current	Full duplex	120	160	mA
Irx	Average RX Current	Full duplex	50	70	mA
Itx	Average TX Current	Full duplex	70	90	mA
Vdd	Average Supply Voltage		4.75V	5.25V	V
Clock	25MHz±30ppm				

8.1 ABSOLUTE OPERATION CONDITION

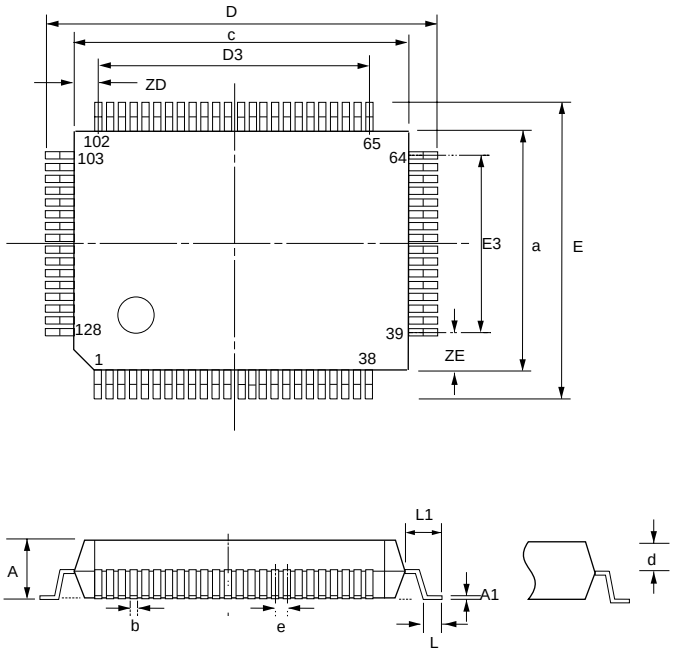
Supply Voltage (VCC)	-0.5V to +7.0V
DC Input Voltage (Vin)	4.75V to 5.25V
DC Output Voltage (Vout)	-0.5V to VCC + 0.5V
Storage Temperature Range (Tstg)	-55℃ to +150℃
Operating Temperature Range	0℃ to 70℃
Operating Surface Temperarure(25℃)	49℃(TYP)
Power Dissipation (PD)	750mW (Typ.)
Lead Temp. (TL) (Soldering, 10 sec)	260℃
ESD Rating (Rzap = 1.5k, Czap = 100pF)	1.0kV
Clamp Diode Current	20mA

9.0 PACKAGE INFORMATION

128-Pin Plastic Quad Flat Pack

ITEM	MILLIMETERS	INCHES
a	14.00±.05	5.512±.002
b	.20 [Typ.]	.08 [Typ.]
c	20.00±.05	7.87±.002
d	1.346	.530
e	.50 [Typ.]	.20 [Typ.]
L1	1.60±.1	.63±.04
L	.80±.1	.31±.04
ZE	.75 [Typ.]	.30 [Typ.]
E3	12.50 [Typ.]	4.92 [Typ.]
E	17.20±.2	6.77±.08
ZD	.75 [Typ.]	.30 [Typ.]
D3	18.50 [Typ.]	7.28 [Typ.]
D	23.20±.2	9.13±.08
A1	.25±.1 min.	.01±.04 min.
A	3.40±.1 max.	1.34±.04 max.
Note	Short Lead	Short Lead

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
0.9.6	Changed to V 0.9.6 added revision history	P53	July/28/1999
0.9.6	added register 30h description	P17	
0.9.6	added register 30h description	P18	
0.9.6	add register 40h-43h as reserved.	P21	
0.9.6	LRPS register , add "notes".	P12	
0.9.6	add MAC address filtering flow chart	P35	
0.9.6	12K changed to 10K. 1.5K changed to 1.4K	P7	
0.9.6	RLBP changed to RHBP	P14	
0.9.6	add "RHBP" short hand to register 1A, 1B h	P15	
0.9.6	rename network address filtering registers (MAR)	P17	
0.9.6	change 12K to 10K	P48	
0.9.7	modify MISC Control Register	P21	Dec/28/1999
0.9.7	add Write TX FIFO Data Port register	P22	
0.9.7	add Read Data register	P22	
0.9.7	add MISC Control Register 2	P22	
0.9.7	add Host Receive Packet Counter	P23	
0.9.7	add Host DMA Fragment Counter	P23	
0.9.8	contents modify	P10,31	Apr/06/2000
0.9.9	MX98726A --> MX98726EC		May/31/2000
	add features	P1	
	modify internal block diagram	P2	
	add combo application	P3	
	modify pin configuration and description	P4	
	modify pin description (pin 70~73)	P5	
	modify packet buffer interface (pin 4~7)	P6	
	modify miscellaneous (pin 83, 84)	P7	
	modify network control register (bit 1.5)	P10	
	modify GMAC test register	P11	
	modify receive interrupt timer	P15	
	modify NWY configuration register (bit 30.2, 30.[5:3]	P18	
	modify GMAC configuration a register (bit 32.4)	P18	
	modify GMAC configuration b register (bit 33.5-4, 33.7-6)	P19	
	modify MISC control register (bit 3D.0, 3D.6, 3D.7)	P22	
	modify receive buffer ring full	P32	
	modify GMAC network address filtering	P36	
	add 6.1 On-Chip Transceiver vs MII Interface	P44	
	add Management Signal timing MDIO source	P50	
	add Management Signal timing MDIO source	P51	
	IOB description modified	P14	Jun/05/2000
	add "on chip registers addressing scheme" paragraph and	P24,25	
	add "more receive bandwidth without using TX Ring Buffer" paragraph		
	modify miscellaneous description (pin 42,43)	P7	Jul/03/2000
1.0	change Reg 0.1, 0.2 descriptions	P9	Jul/13/2000
	add Reg 1C.6 and 1C.7 descriptions	P16	
	change Reg 30.0 FD bit description	P18	
	add Reg 33.4, 33.5 and 33.6 descriptions	P20	
	enhance Reg 3D.6 description	P22	
	0.3 SR*Start Transmit-->Receive	P09	Nov/15/2000

REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
1.1	add 8.1 ABSOLUTE OPERATION CONDITION	P51	JAN/15/2001
1.1	update internal pull-up & pull-down information	P5,6,7	FEB/28/2001
	enhance TWP description	P14	
	modify RXINTT register description	P15	
	enhance Figure 4.0	P25	
	remove TBLEN description	P27	
	remove RBLEN description	P31	
	add pull-up & pull-down DC current remore software programming interface section (application note has such info)	P41	
	add memory read&write cycle in 80x1 mode picture	P46,47	
	add host interface timing in 8018x mode	P51	

TOP SIDE MARKING

MX98726EC	line 1 : MX98726 is MXIC parts No. "E" :PQFP "C" : commercial grade
C9930	line 2 : Assembly Date Code.
TA777001	line 3 : Wafer Lot No.
38BAX	line 4 : "38B" : revision code, "A" : bonding option "X" : no used
TAIWAN	line 5 : State

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