

DATA SHEET

PDTC114E series

NPN resistor-equipped transistor;

$R1 = 10\text{ k}\Omega$, $R2 = 10\text{ k}\Omega$

Product specification
Supersedes data of 1999 May 31

2003 Apr 10

NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 10 k Ω

PDTC114E series

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	50	V
I _O	output current (DC)	–	100	mA
R1	bias resistor	10	–	k Ω
R2	bias resistor	10	–	k Ω

DESCRIPTION

NPN resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP COMPLEMENT
	PHILIPS	EIAJ		
PDTC114EE	SOT416	SC-75	09	PDTA114EE
PDTC114EEF	SOT490	SC-89	09	PDTA114EEF
PDTC114EK	SOT346	SC-59	04	PDTA114EK
PDTC114EM	SOT883	SC-101	DS	PDTA114EM
PDTC114ES	SOT54 (TO-92)	SC-43	TC114E	PDTA114ES
PDTC114ET	SOT23	–	*16 ⁽¹⁾	PDTA114ET
PDTC114EU	SOT323	SC-70	*09 ⁽¹⁾	PDTA114EU

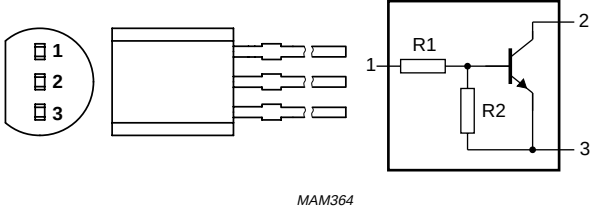
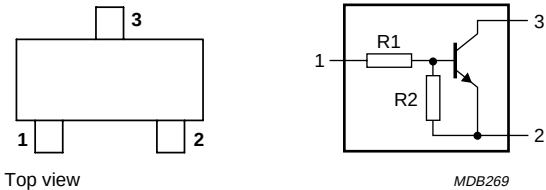
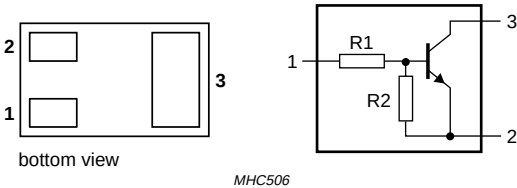
Note

- * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

NPN resistor-equipped transistor;
R1 = 10 kΩ, R2 = 10 kΩ

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTC114ES	 MAM364	1 2 3	base collector emitter
PDTC114EE PDTC114EEF PDTC114EK PDTC114ET PDTC114EU	 Top view MDB269	1 2 3	base emitter collector
PDTC114EM	 bottom view MHC506	1 2 3	base emitter collector

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PDTC114E series

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _I	input voltage				
	positive		–	+40	V
	negative		–	–10	V
I _O	output current (DC)		–	100	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT54	note 1	–	500	mW
	SOT23	note 1	–	250	mW
	SOT346	note 1	–	250	mW
	SOT323	note 1	–	200	mW
	SOT416	note 1	–	150	mW
	SOT490	notes 1 and 2	–	250	mW
	SOT883	notes 2 and 3	–	250	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	in free air		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT416	note 1	833	K/W
	SOT490	notes 1 and 2	500	K/W
	SOT883	notes 2 and 3	500	K/W

Notes

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2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

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CHARACTERISTICS

$T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{\text{CB}} = 50\text{ V}$; $I_{\text{E}} = 0$	–	–	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{\text{CE}} = 30\text{ V}$; $I_{\text{B}} = 0$	–	–	1	μA
		$V_{\text{CE}} = 30\text{ V}$; $I_{\text{B}} = 0$; $T_{\text{j}} = 150\text{ }^{\circ}\text{C}$	–	–	50	μA
I_{EBO}	emitter-base cut-off current	$V_{\text{EB}} = 5\text{ V}$; $I_{\text{C}} = 0$	–	–	400	μA
h_{FE}	DC current gain	$V_{\text{CE}} = 5\text{ V}$; $I_{\text{C}} = 5\text{ mA}$	30	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_{\text{C}} = 10\text{ mA}$; $I_{\text{B}} = 0.5\text{ mA}$	–	–	150	mV
$V_{\text{i(off)}}$	input-off voltage	$I_{\text{C}} = 100\text{ }\mu\text{A}$; $V_{\text{CE}} = 5\text{ V}$	–	1.1	0.8	V
$V_{\text{i(on)}}$	input-on voltage	$I_{\text{C}} = 10\text{ mA}$; $V_{\text{CE}} = 0.3\text{ V}$	2.5	1.8	–	V
$R1$	input resistor		7	10	13	$\text{k}\Omega$
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C_{c}	collector capacitance	$I_{\text{E}} = i_{\text{e}} = 0$; $V_{\text{CB}} = 10\text{ V}$; $f = 1\text{ MHz}$	–	–	2.5	pF

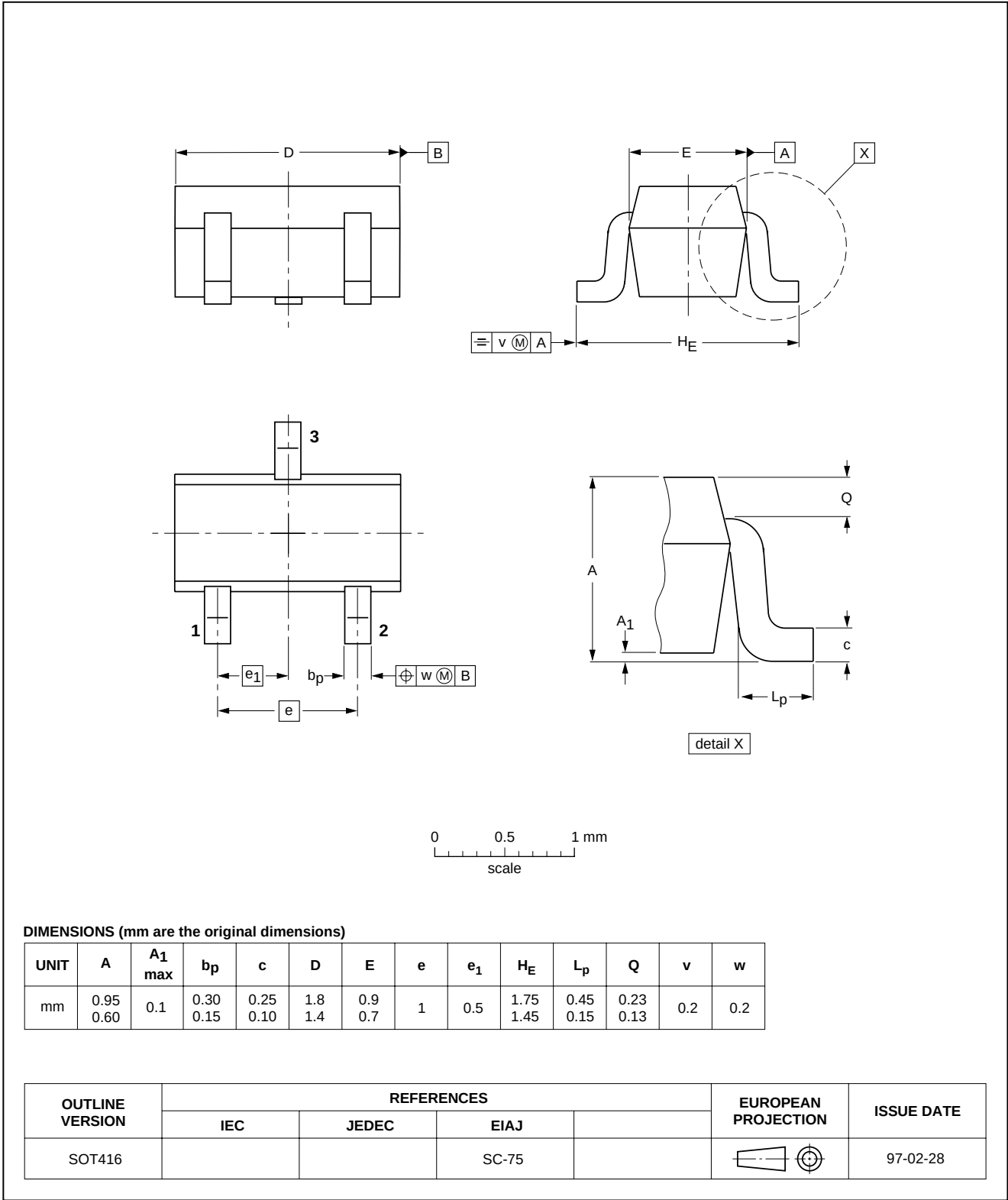
NPN resistor-equipped transistor;
R1 = 10 kΩ, R2 = 10 kΩ

PDTC114E series

PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT416

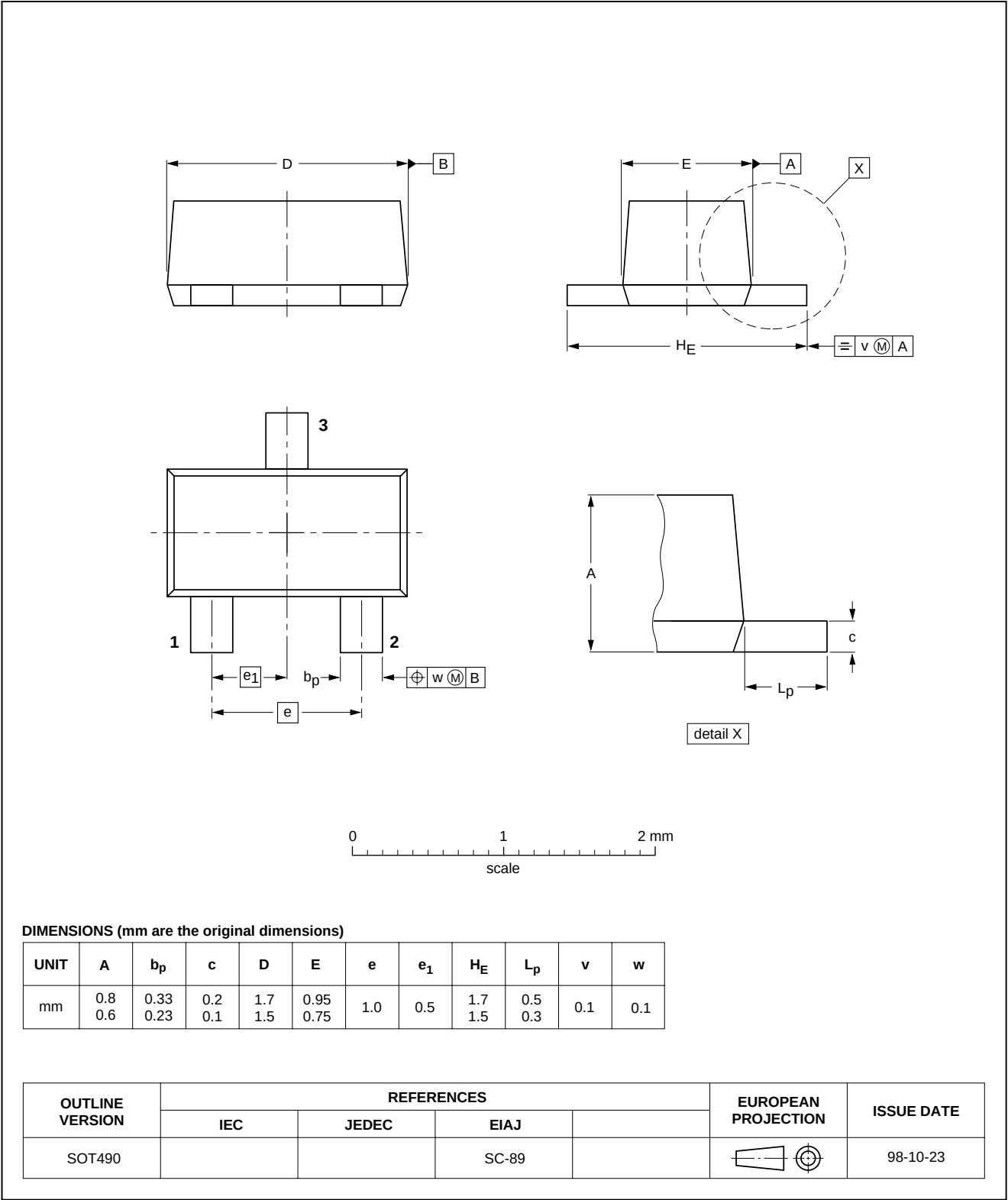


NPN resistor-equipped transistor;
R1 = 10 kΩ, R2 = 10 kΩ

PDTC114E series

Plastic surface mounted package; 3 leads

SOT490

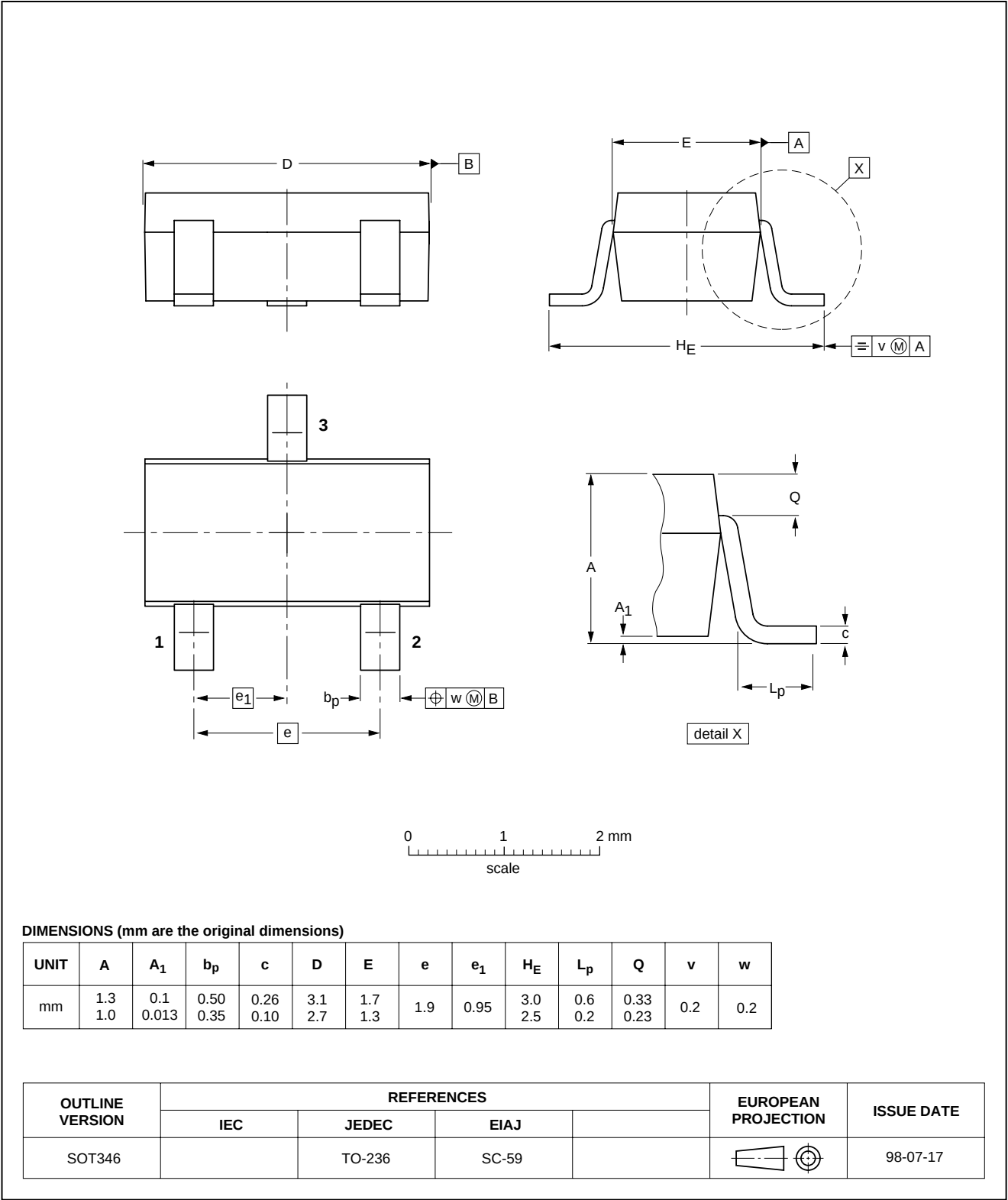


NPN resistor-equipped transistor;
R1 = 10 kΩ, R2 = 10 kΩ

PDTC114E series

Plastic surface mounted package; 3 leads

SOT346

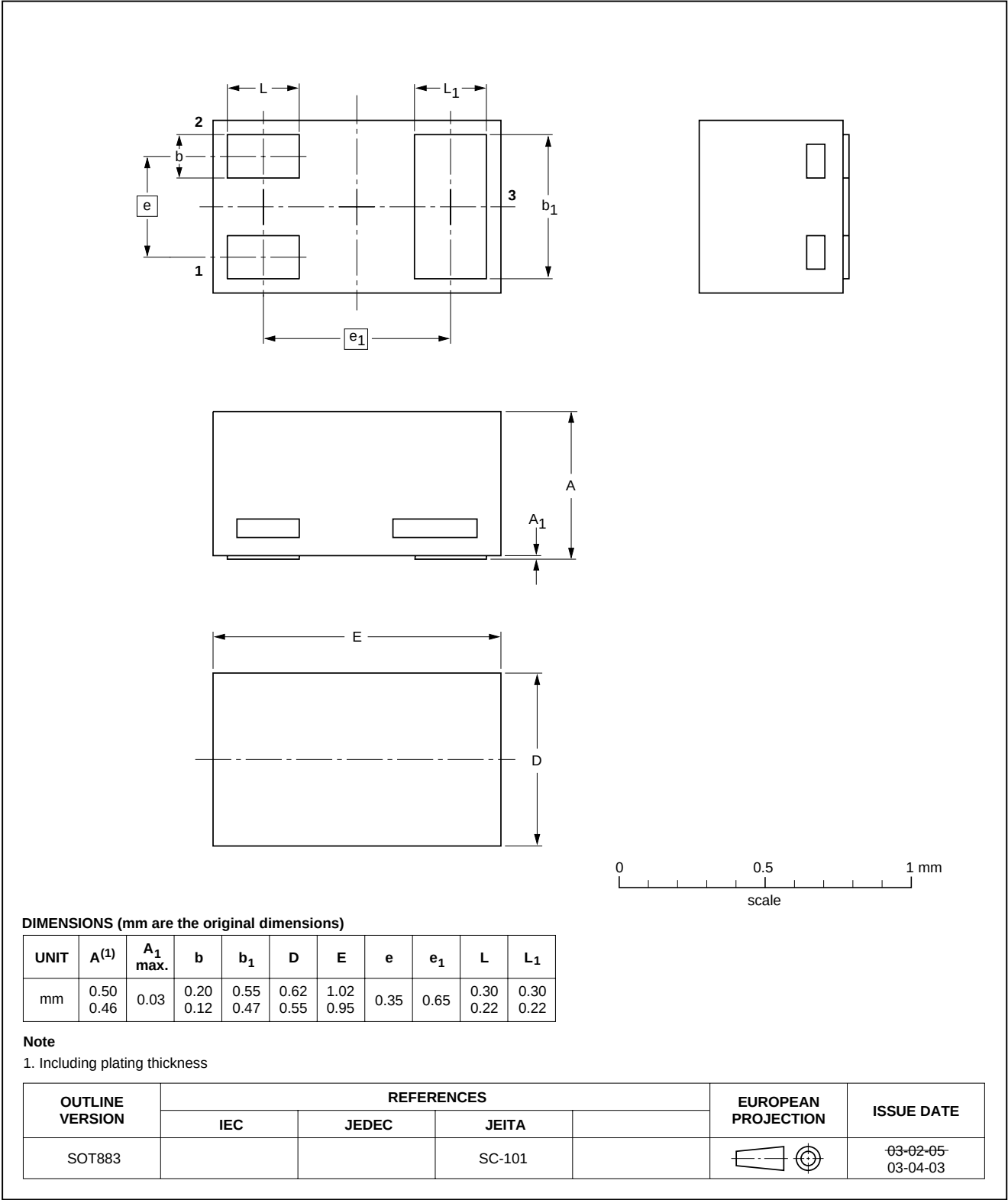


NPN resistor-equipped transistor;
R1 = 10 kΩ, R2 = 10 kΩ

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Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883

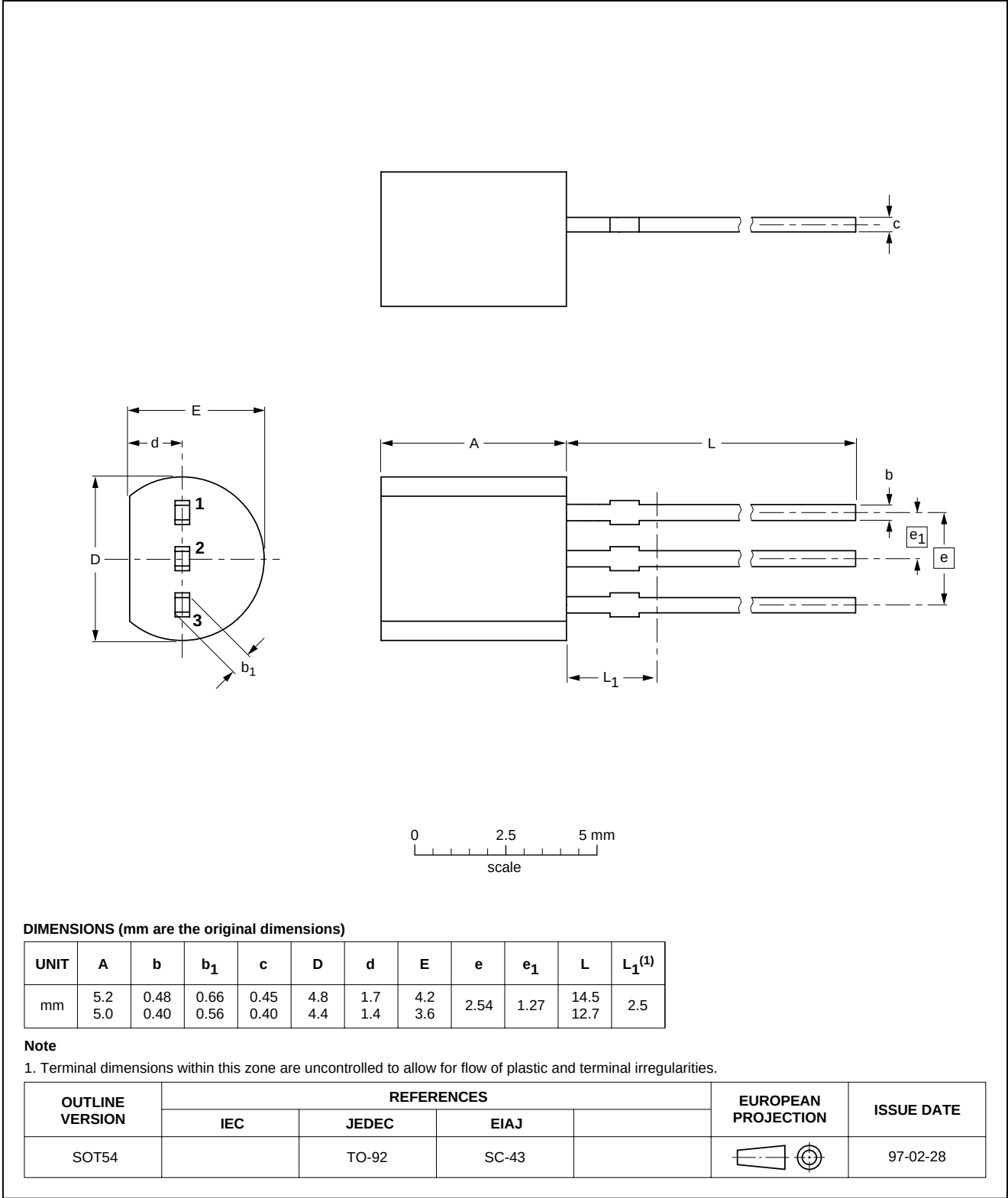


NPN resistor-equipped transistor;
R1 = 10 kΩ, R2 = 10 kΩ

PDTC114E series

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

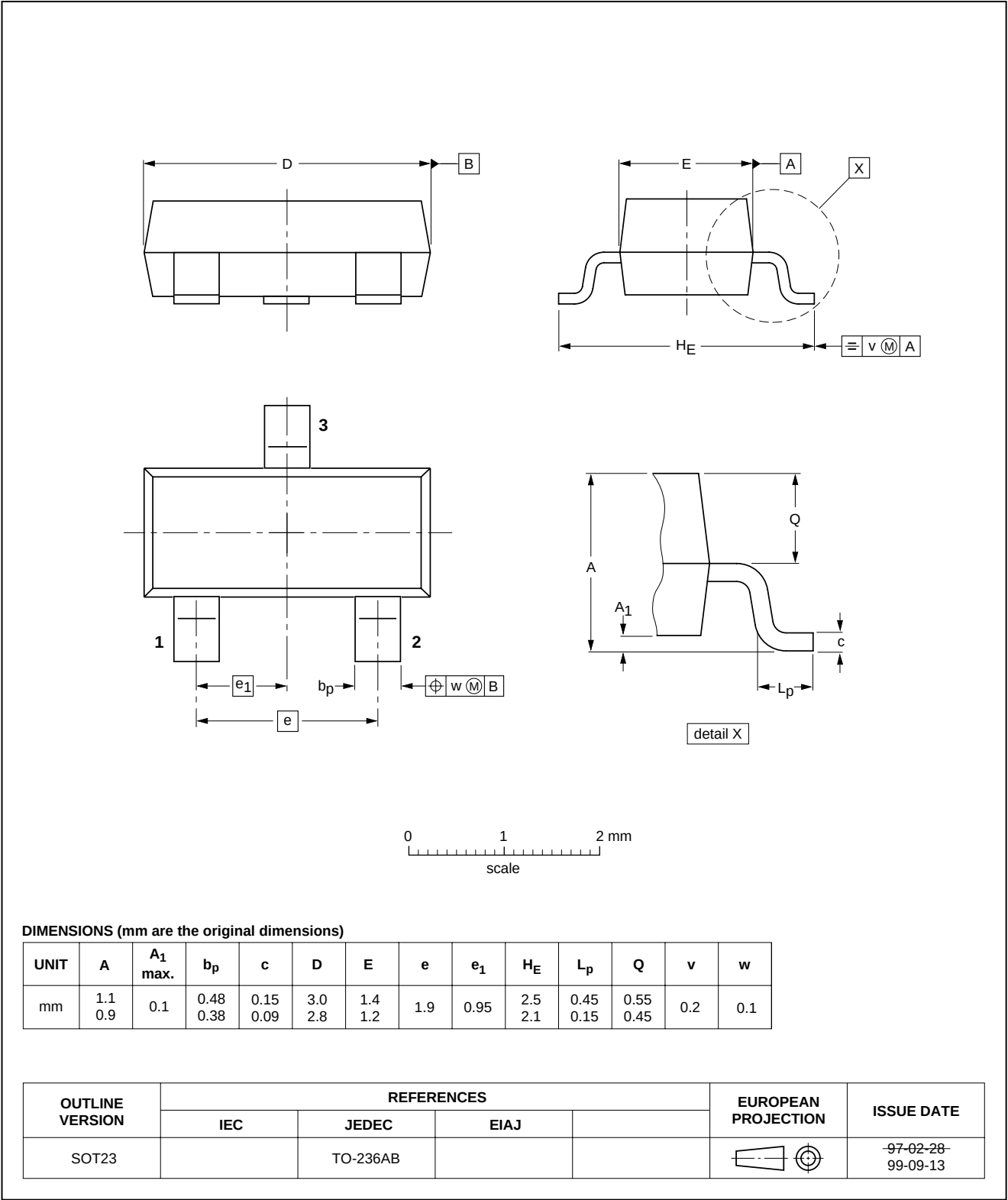


NPN resistor-equipped transistor;
R1 = 10 kΩ, R2 = 10 kΩ

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Plastic surface mounted package; 3 leads

SOT23

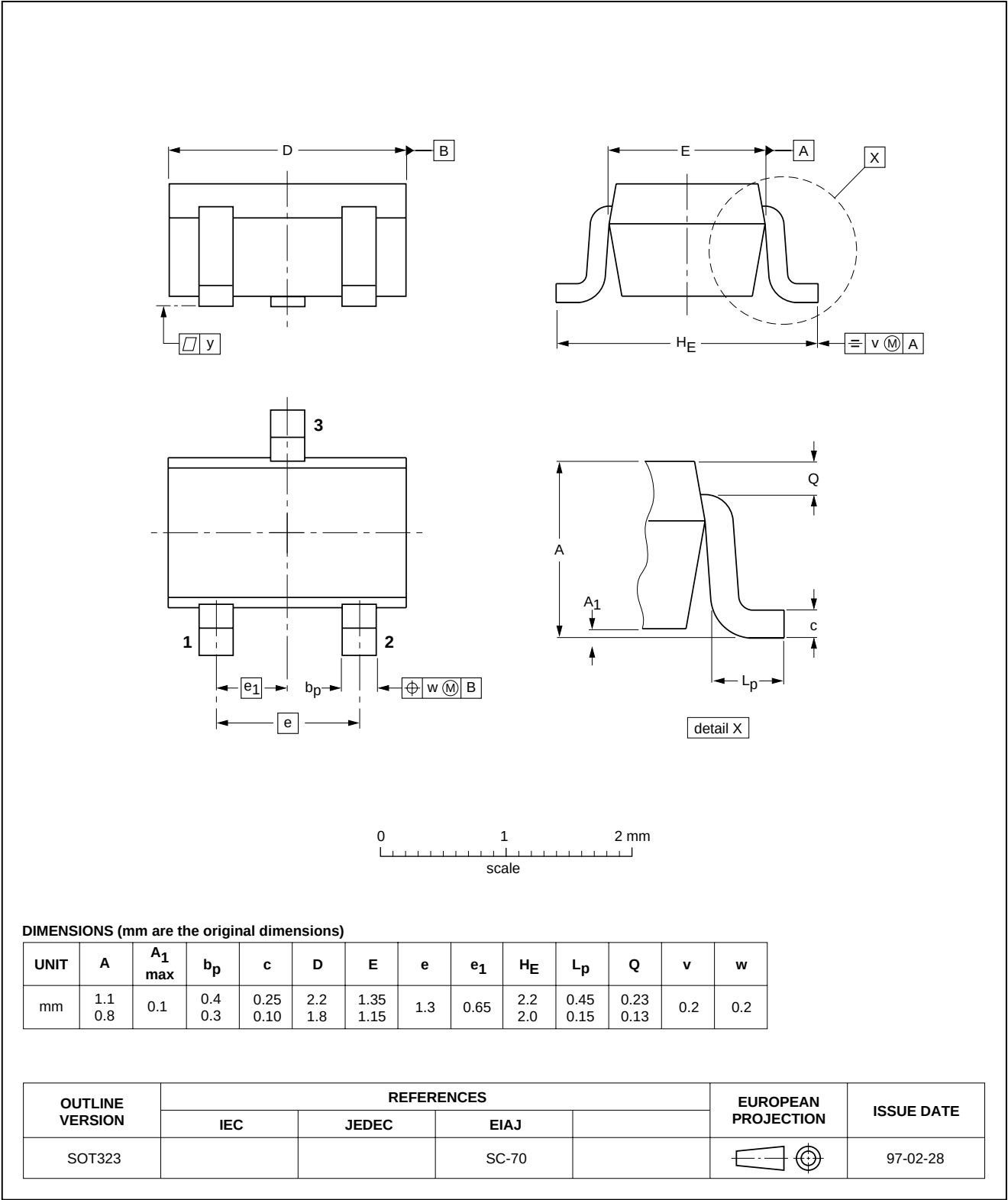


NPN resistor-equipped transistor;
R1 = 10 kΩ, R2 = 10 kΩ

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Plastic surface mounted package; 3 leads

SOT323



NPN resistor-equipped transistor;
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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

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NOTES

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NOTES

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Contact information

For additional information please visit <http://www.semiconductors.philips.com>. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to: sales.addresses@www.semiconductors.philips.com.

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