19-3257; Rev 0; 4/04

EVALUATION KIT AVAILABLE

4A Ultra-Low-Input-Voltage LDO Regulators

General Description

The MAX8556/MAX8557 low-dropout linear regulators operate from input voltages as low as 1.425V and are able to deliver up to 4A of continuous output current with a typical dropout voltage of only 100mV. The output voltage is adjustable from 0.5V to V_{IN} - 0.2V.

Designed with an internal p-channel MOSFET pass transistor, the MAX8556/MAX8557 maintain a low 800µA typical supply current, independent of the load current and dropout voltage. Using a p-channel MOSFET eliminates the need for an additional external supply or a noisy internal charge pump. Other features include a logic-controlled shutdown mode, built-in soft-start, short-circuit protection with foldback current limit, and thermal-overload protection. The MAX8556 features a POK output that transitions high when the regulator output is within ±10% of its nominal output voltage. The MAX8557 offers a power-on reset output that transitions high 140ms after the output has achieved 90% of its nominal output voltage.

The MAX8556/MAX8557 are available in a 16-pin thin QFN 5mm x 5mm package with exposed paddle.

Applications

Servers and Storage Devices

Networking

Base Stations

Optical Modules

Point-of-Load Supplies

ATE

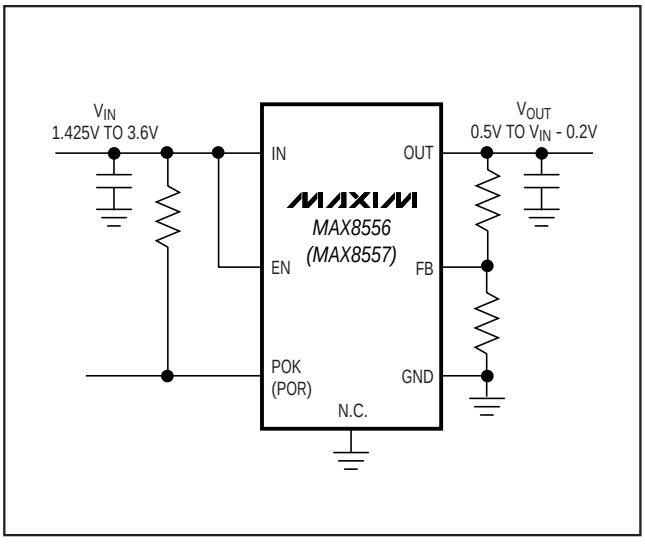
Features

- **1.425V to 3.6V Input Voltage Range**
- **Guaranteed 4A Output Current**
- **±1% Output Accuracy Over Load/Line/ Temperature**
- **100mV Dropout at 4A Load (typ)**
- **Built-In Soft-Start**
- **800µA (typ) Operating Supply Current**
- **150µA (max) Shutdown Supply Current**
- **Short-Circuit Current Foldback Protection**
- **Thermal-Overload Protection**
- **±10% Power-OK (MAX8556)**
- **140ms Power-On Reset Output (MAX8557)**
- **Fast Transient Response**
- **16-Pin Thin QFN 5mm x 5mm Package**

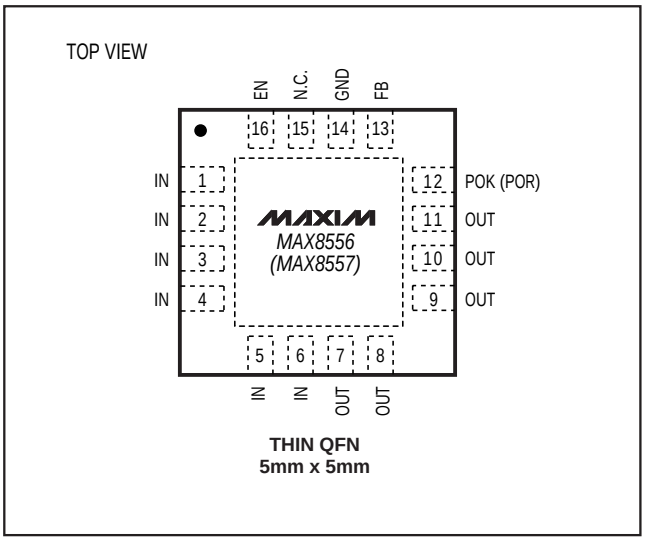
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	FEATURE
MAX8556ETE	-40°C to +85°C	16 Thin QFN 5mm X 5mm	POK
MAX8557ETE	-40°C to +85°C	16 Thin QFN 5mm X 5mm	POR

Typical Operating Circuit



Pin Configuration



THIN QFN
5mm x 5mm

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

4A Ultra-Low-Input-Voltage LDO Regulators

ABSOLUTE MAXIMUM RATINGS

IN, EN, POK, POR to GND .....-0.3V to +4V
FB, OUT to GND .....-0.3V to (V_{IN} + 0.3V)
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin Thin QFN (derate 33.3mW/°C above +70°C) (Note 1).....2666.7mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Maximum power dissipation is obtained using JEDEC JESD51-5 and JESD51-7 standards.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EN} = V_{IN} = 1.8V, V_{OUT} = 1.5V, I_{OUT} = 2mA, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted. Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN						
Input Voltage Range			1.425		3.600	V
Input Undervoltage Lockout	V_{IN} rising, 70mV hysteresis		1.30	1.35	1.40	V
	V_{IN} falling		1.23	1.28	1.33	
OUT						
Output Voltage Range			0.5		3.4	V
Load Regulation	I_{OUT} = 2mA to 4A			0.1		%/A
Line Regulation	V_{IN} = 1.425V to 3.6V, V_{OUT} = 1.225V		-0.15	0	+0.15	%/V
Dropout Voltage	V_{IN} = 1.425V, I_{OUT} = 4A, V_{FB} = 480mV			100	200	mV
Regulated Output-Voltage Current Limit	V_{IN} = 3.6V, V_{OUT} = 3V, V_{FB} = 460mV		5	7	9	A
Load Capacitance	ESR < 50mA		16		120	µF
FB						
FB Threshold Accuracy (Note 3)	V_{OUT} = 1.225V to 3V, V_{IN} = V_{OUT} + 0.2V to 3.6V, I_{OUT} = 2mA to 4A		495	500	505	mV
FB Input Bias Current	V_{FB} = 0.5V, V_{IN} = 3.6V			0.001	1	µA
GND						
GND Supply Current	V_{IN} = 1.425V to 3.6V, V_{OUT} = 1.225V			800	1600	µA
	Dropout, V_{IN} = 3.6V, V_{FB} = 480mV			1000	2000	
GND Shutdown Current	V_{IN} = 3.6V, EN = GND				150	µA
POK						
FB Power-OK Fault Threshold	FB moving out of regulation, V_{IN} = 1.425V to 3.6V, 10mV hysteresis	FB high	540	550	560	mV
		FB low	440	450	460	
POK Output Voltage, Low	V_{FB} = 0.4V or 0.6V, I_{POK} = 2mA			25	200	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{EN} = V_{IN} = 1.8V, V_{OUT} = 1.5V, I_{OUT} = 2mA, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted. Note 2)

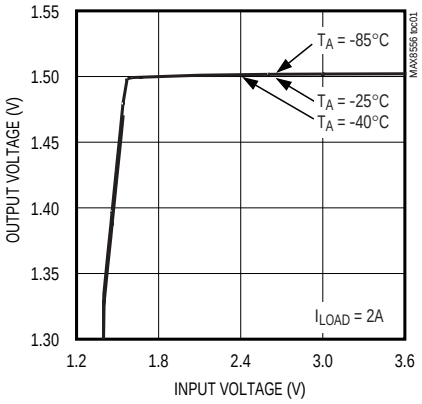
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POK Output Current, High	V_{POK} = 3.6V V_{FB} = 0.5			0.001	1	µA
POK Delay Time	From FB rising to POK high		25	50	100	µs
EN						
Enable Input Threshold	V_{IN} = 1.425V to 3.6V	EN rising			1.25	V
		EN falling	0.4			
Enable Input Bias Current	V_{EN} = 0V or 3.6V		-1		+1	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	Output on and off	T_J rising		+160		°C
		T_J falling		+115		
POR						
FB Power-On Reset Fault Threshold	FB falling, V_{IN} = 1.425V to 3.6V, 10mV hysteresis		440	450	460	mV
POR Output Voltage, Low	V_{FB} = 0.4V, I_{POR} = 2mA			25	200	mV
POR Output Current, High	V_{POR} = 3.6V, V_{FB} = 0.5V			0.001	1	µA
POR Rising Delay Time	FB rising to POR high impedance		100	140	200	ms
SOFT-START						
Soft-Start Time				100		µs

Note 2: Specifications to -40°C are guaranteed by design and not production tested.
Note 3: Minimum supply voltage for output accuracy must be at least 1.425V.

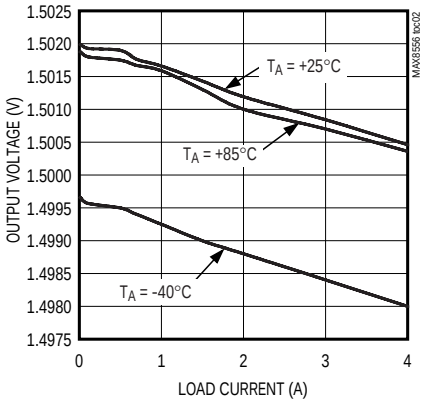
Typical Operating Characteristics

(V_{EN} = V_{IN} = +1.8V, V_{OUT} = +1.5V, I_{OUT} = 4A, C_{OUT} = 20µF, C_{IN} = 20µF, and T_A = +25°C, unless otherwise noted.)

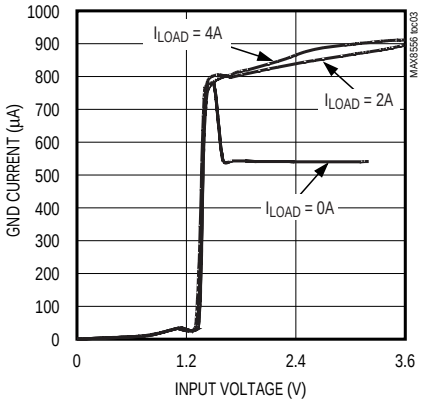
OUTPUT VOLTAGE vs. INPUT VOLTAGE



OUTPUT VOLTAGE vs. LOAD CURRENT



GND CURRENT vs. INPUT VOLTAGE

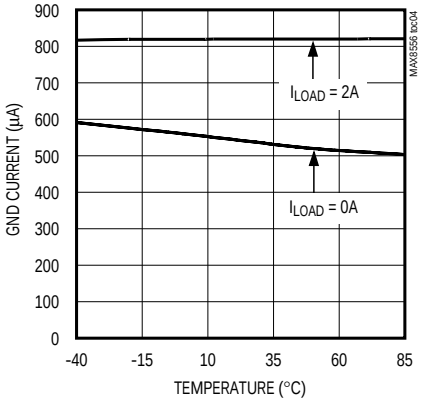


4A Ultra-Low-Input-Voltage LDO Regulators

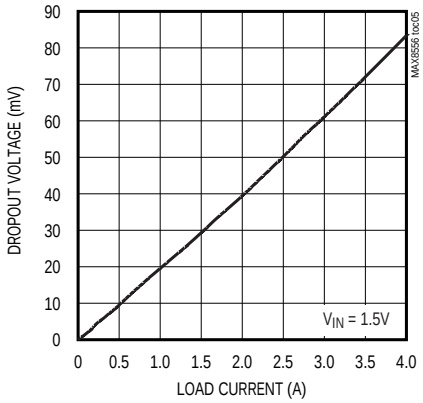
Typical Operating Characteristics (continued)

(V_{EN} = V_{IN} = +1.8V, V_{OUT} = +1.5V, I_{OUT} = 4A, C_{OUT} = 20µF, C_{IN} = 20µF, and T_A = +25°C, unless otherwise noted.)

GND CURRENT vs. TEMPERATURE

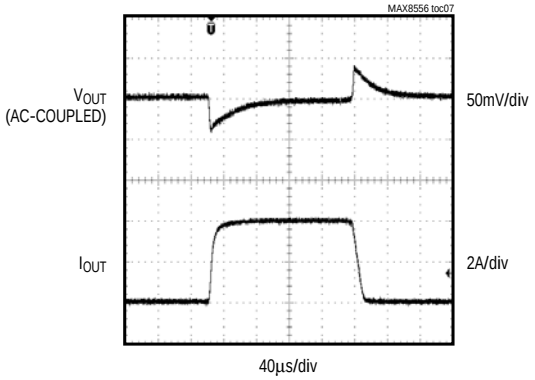


DROPOUT VOLTAGE vs. LOAD CURRENT

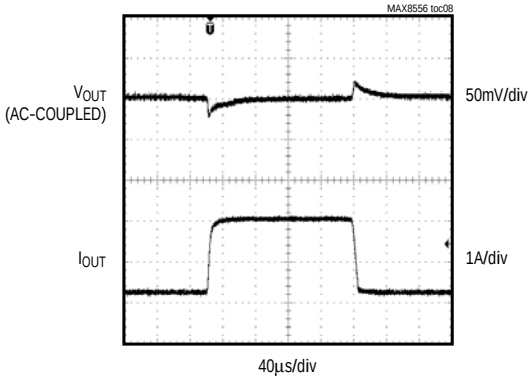


LINE-TRANSIENT RESPONSE

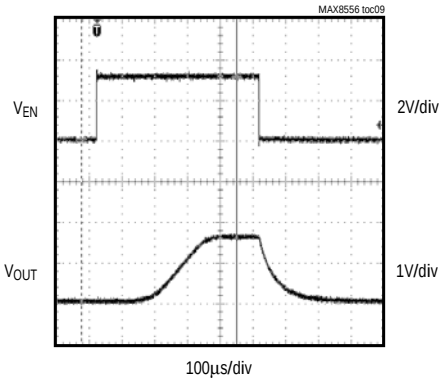
4A LOAD-TRANSIENT RESPONSE



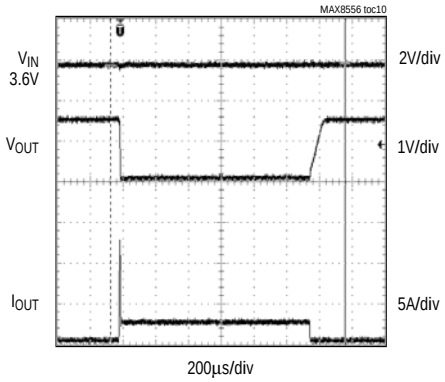
2A LOAD-TRANSIENT RESPONSE



ENABLE WAVEFORMS



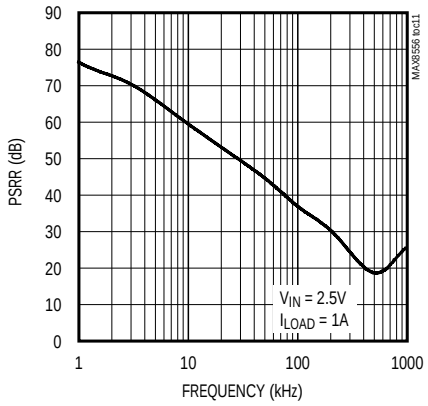
SHORT-CIRCUIT WAVEFORMS



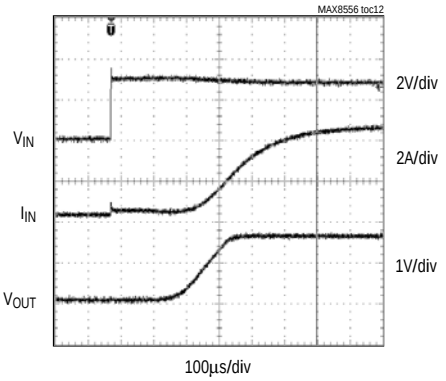
Typical Operating Characteristics (continued)

(V_{EN} = V_{IN} = +1.8V, V_{OUT} = +1.5V, I_{OUT} = 4A, C_{OUT} = 20µF, C_{IN} = 20µF, and T_A = +25°C, unless otherwise noted.)

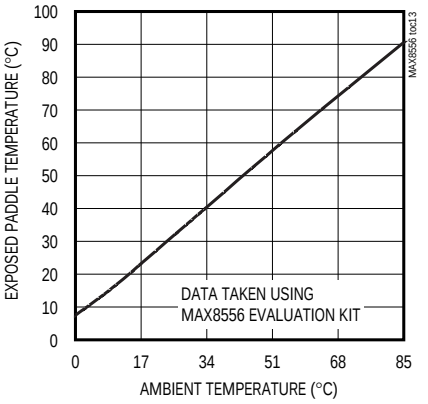
PSRR vs. FREQUENCY



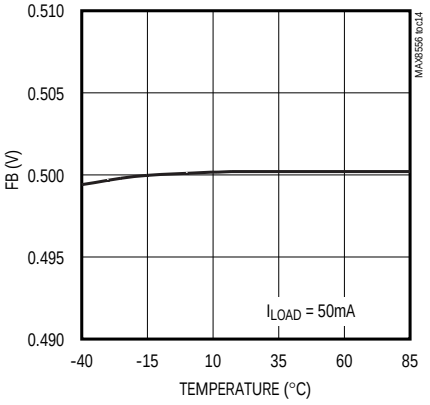
STARTUP WAVEFORMS



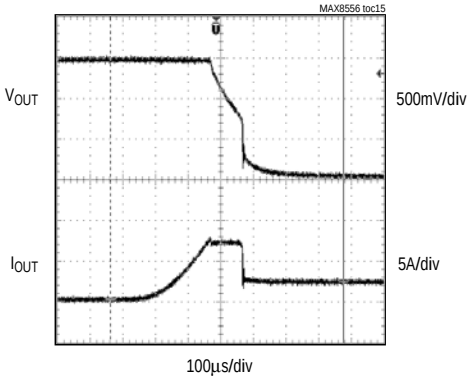
EXPOSED PADDLE TEMPERATURE vs. AMBIENT TEMPERATURE



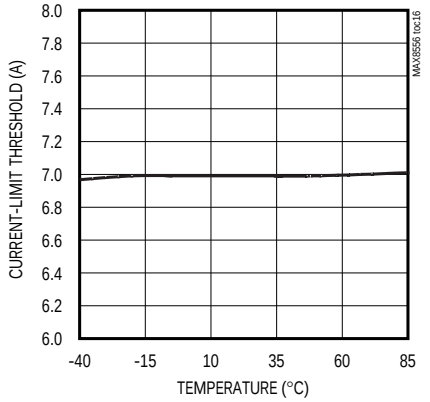
FB REGULATION vs. TEMPERATURE



FOLDBACK CURRENT-LIMIT WAVEFORMS



CURRENT-LIMIT THRESHOLD vs. TEMPERATURE

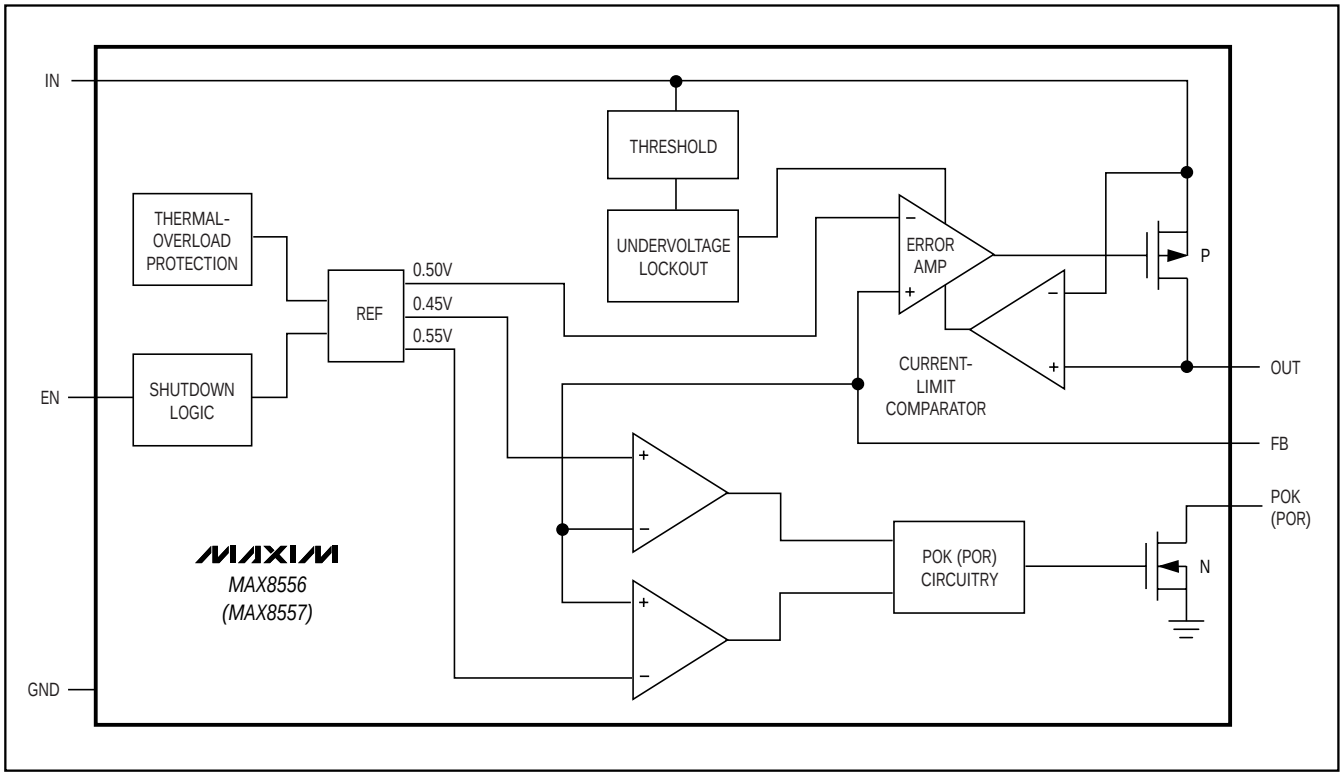


4A Ultra-Low-Input-Voltage LDO Regulators

Pin Description

PIN	NAME	FUNCTION
1–6	IN	LDO Input. Connect to a 1.425V to 3.6V input voltage. Bypass with a 22µF ceramic capacitor to GND.
7–11	OUT	LDO Output. Bypass with 2 x 10µF ceramic capacitors to GND. A smaller capacitance can be used if the maximum load current is less than 4A.
12	POK (MAX8556)	Power-OK Output. Open-drain output that pulls low when V_{OUT} is outside ±10% of the expected regulation voltage or when EN is low. POK is high impedance when V_{OUT} is within ±10% of the nominal output voltage. Connect a resistor from POK to a logic supply of less than 3.6V.
	POR (MAX8557)	Power-On Reset. Open-drain output goes high impedance 140ms after the output is above 90% of its nominal regulation voltage. POR pulls low immediately after an output fault or when EN is low. Connect a resistor from POR to a logic supply of less than 3.6V.
13	FB	Feedback Input. V_{FB} is regulated to 0.5V. Connect to the center tap of a resistor-divider from output to GND to set the desired output voltage.
14	GND	Ground
15	N.C.	Connect to GND or Floating
16	EN	Enable Input. Connect to GND or a logic low to shut down the device. Connect to IN or a logic high for normal operation.
EP	—	Exposed Paddle. Connect to GND and to a ground plane for heatsinking.

Block Diagram



Detailed Description

The MAX8556/MAX8557 low-dropout linear regulators are capable of delivering up to 4A from low-input voltage supplies ranging from 1.425V to 3.6V with only 200mV of dropout (max). The PMOS output stage can be driven from input voltages down to 1.425V without sacrificing stability or transient performance. Supply current is not a significant function of load or input headroom because this regulator has a PMOS output device.

The MAX8556/MAX8557 are fully protected from an output short circuit by current-limiting and thermal-overload circuitry. The low-power shutdown mode reduces supply current to 0.2µA (typ) to maximize battery life in portable applications. The MAX8556 includes an open-drain power-OK signal (POK) that goes high when the regulator output is within ±10% of its nominal output voltage. The MAX8557 includes an open-drain power-on-reset output (POR) that goes high 140ms after the output has risen above 90% of its nominal value.

Internal P-Channel Pass Transistor

The MAX8556/MAX8557 feature a 25mΩ p-channel MOSFET pass transistor. Unlike similar designs using pnp pass transistors, p-channel MOSFETs require no base drive, which reduces quiescent current; pnp-based regulators also waste considerable current in dropout when the pass transistor saturates, and use high base-drive currents under large loads. The MAX8556/MAX8557 do not suffer from these problems and consume only 800µA (typ) of quiescent current under heavy loads, as well as in dropout.

Short-Circuit/Thermal Fault Protection

The MAX8556/MAX8557 are fully protected from output short circuits through current-limiting and thermal-overload circuitry. When the output is shorted to ground, the output current is foldback limited to 3A (max). Under these conditions, the device quickly heats up. When the junction temperature reaches +160°C, the thermal-overload circuitry turns off the output, allowing the device to cool. When the junction cools to +115°C, the output turns back on and attempts to establish regulation. Current limiting and thermal protection continue until the fault is removed.

Shutdown Mode

The MAX8556/MAX8557 feature a low-power shutdown mode that reduces quiescent current to 0.2µA (typ). Drive EN low to disable the voltage reference, error amplifier, gate-drive circuitry, and pass transistor, and pull the output low with 5k impedance. Drive EN high or connect to IN for normal operation.

Power-OK Output (POK, MAX8556 Only)

The MAX8556 features a power-OK (POK) output to indicate the status of the output. POK is high impedance when the regulator output is within ±10% of its nominal output voltage. If the output voltage falls/rises outside this range or the IC experiences thermal fault, POK is internally pulled low. This open-drain output requires an external pullup resistor to V_{IN} or another logic supply below 3.6V. For glitch immunity, an internal delay circuit prevents the output from switching for 50µs (typ) after the trip threshold is initially reached. POK is low when the IC is in shutdown mode.

Power-On Reset (POR, MAX8557 Only)

The MAX8557 features a power-on reset output that goes high impedance 140ms (typ) after the output reaches 90% of its nominal value. This open-drain output requires an external pullup resistor to V_{IN} or another logic supply less than 3.6V. When the output falls below 90% of the nominal output voltage or the IC experiences a thermal fault, POR immediately transitions low. POR is low when the IC is in shutdown mode.

Operating Region and Power Dissipation

The maximum power dissipation depends on the thermal resistance of the IC package and the circuit board, the temperature difference between the die junction and ambient air, and the rate of ambient airflow. The power dissipated by the IC is $P = I_{OUT} \times (V_{IN} - V_{OUT})$. Proper PC board layout can increase the allowed power dissipation by dissipating heat in the board instead of the package. See the *Thermal Considerations in PC Board Layout* section for more details.

4A Ultra-Low-Input-Voltage LDO Regulators

Applications Information

Output Voltage Selection

The MAX8556/MAX8557 feature an adjustable output voltage from 0.5V to 3.4V. Set the output voltage using an external resistor-divider from the output to GND with FB connected to the center tap as shown in Figures 1 and 2. Choose R3 ≤ 1kΩ for light-load stability. Determine R2 using the following equation:

$$R2 = R3 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{OUT} is the desired output voltage and V_{FB} is 0.5V.

Capacitor Selection and Regulator Stability

Capacitors are required at the MAX8556/MAX8557 inputs and outputs for stable operation over the full temperature range and with load currents up to 4A. Connect 2 x 10µF capacitors between IN and GND and 2 x 10µF low equivalent-series-resistance (ESR) capacitors between OUT and GND. The input capacitor (C_{IN}) lowers the source impedance of the input supply. If the MAX8556/MAX8557s' input is close to the output of the source supply, a smaller input capacitance can be used. Otherwise, 2 x 10µF ceramic input capacitors are recommended. The output capacitor's (C_{OUT}) ESR affects output noise and may affect output stability. Use output capacitors with an ESR of 0.05Ω or less to ensure stability and optimum transient dropout. For good output transient performance, use the following formula to select a minimum output capacitance:

$$C_{OUT} = I_{OUT(MAX)} \times 1\mu F / 200mA$$

Noise, PSRR, and Transient Response

The MAX8556/MAX8557 are designed to operate with low dropout voltages and low quiescent currents while still maintaining low noise, good transient response, and high AC rejection (see the *Typical Operating Characteristics* for a plot of Power-Supply Rejection Ratio (PSRR) vs. Frequency). When operating from noisy sources, improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output bypass capacitors and through passive filtering techniques. The MAX8556/MAX8557 load-transient response graphs (see the *Typical Operating Characteristics*) show two components of the output response: a DC shift from the output impedance due to the load current change, and the transient response. A typical transient overshoot for a step change in the load current from 40mA to 4A is 40mV. Use an output capacitance from 20µF to 120µF to attenuate the overshoot.

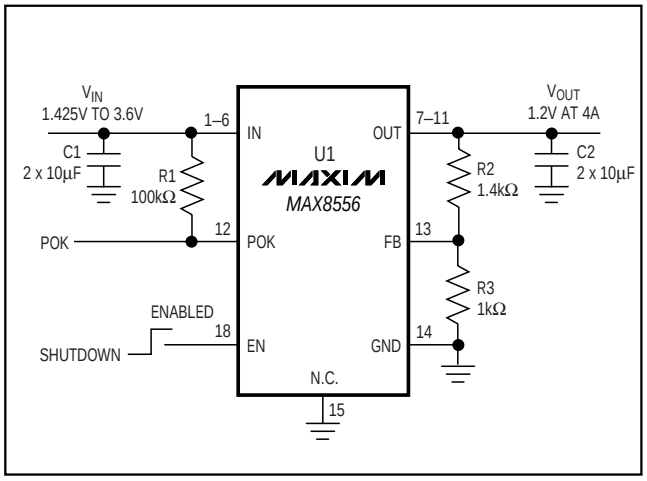


Figure 1. MAX8556 Typical Application Circuit

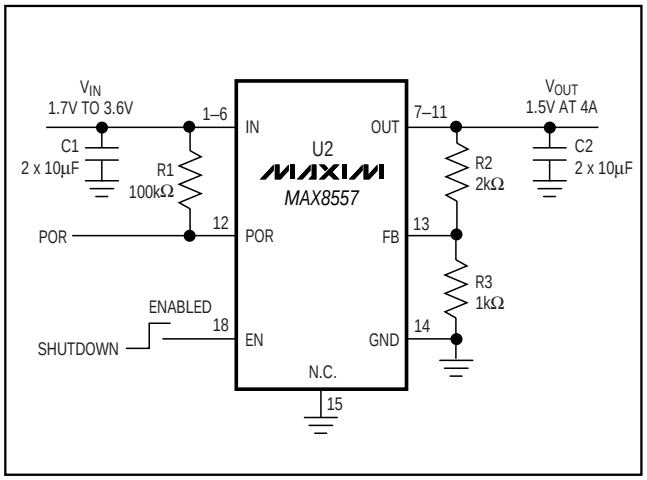


Figure 2. MAX8557 Typical Application Circuit

Thermal Considerations in PC Board Layout

How much power the package can dissipate strongly depends on the mounting method of the IC to the PC board and the copper area for cooling. Using the JEDEC test standard, the maximum power dissipation allowed in the package is 2667mW. This data is obtained with +70°C ambient temperature and +150°C maximum junction temperature. The test board has dimensions of 3in x 3in with four layers of 2oz copper and FR-4 material with 62mil finished thickness. Nine thermal vias are used under the thermal paddle with a diameter of 12mil and 1mil plated copper thickness. Top and bottom layers are used to route the traces. Two middle layers are solid copper and isolated from the nine thermal vias.

More power dissipation can be handled by the package if great attention is given during PC board layout. For example, using the top and bottom copper as a heatsink and connecting the thermal vias to one of the middle layers (GND) transfers the heat from the package into the board more efficiently, resulting in lower junction temperature at high power dissipation in some MAX8556/MAX8557 applications. Furthermore, the solder mask around the IC area on both top and bottom layers can be removed to radiate the heat directly into the air. The maximum allowable power dissipation in the IC is as follows:

$$P_{MAX} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JC} + \theta_{CA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature (+150°C), T_A is the ambient air temperature, θ_{JC} (1.7°C/W for the 16-pin TQFN) is the thermal resistance from the junction to the case, and θ_{CA} is the thermal resistance from the case to the surrounding air through the PC board, copper traces, and the package materials. θ_{CA} is directly related to system level variables and can be modified to increase the maximum power dissipation. The TQFN package has an exposed thermal pad on its underside. This pad provides a low thermal resistance path for heat transfer into the PC board. This low thermally resistive path carries a majority of the heat away from the IC. The PC board is effectively a heatsink for the IC.

The exposed paddle should be connected to a large ground plane for proper thermal and electrical performance. The minimum size of the ground plane is dependent upon many system variables. To create an efficient path, the exposed paddle should be soldered to a thermal landing, which is connected to the ground plane by thermal vias. The thermal landing should be at least as large as the exposed paddle and can be made larger depending on the amount of free space from the exposed paddle to the other pin landings.

A sample layout is available on the MAX8556 evaluation kit to speed designs.

Chip Information

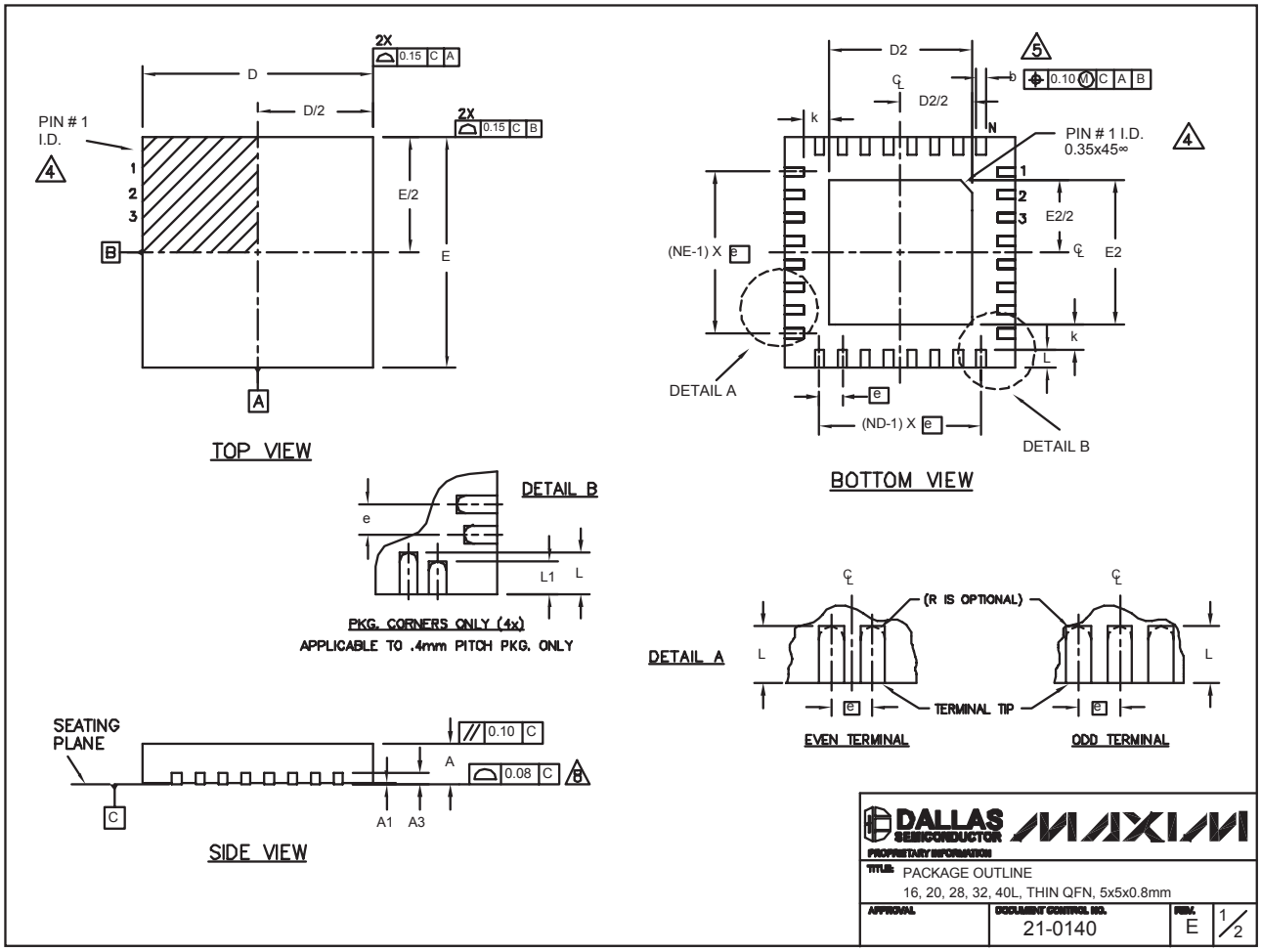
TRANSISTOR COUNT: 3137
PROCESS: BiCMOS

4A Ultra-Low-Input-Voltage LDO Regulators

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	-	0.05	
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60	
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-			

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	YES
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	NO
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	YES
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
16, 20, 28, 32, 40L, THIN QFN, 5x5x0.8mm

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	21-0140	E	2/2

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