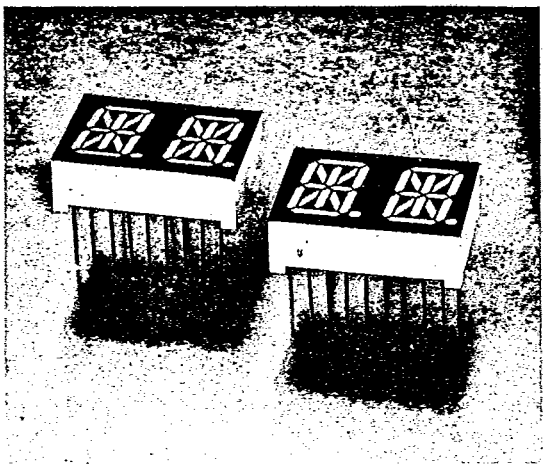
LITE-ON LED SPECIALIST

LTM-8647A SERIES

0.54" 2-CHARACTER 14-SEGMENT ALPHANUMERIC DISPLAY WITH MOS I.C. DRIVER

FEATURES

- 0.54 INCH (13.8mm) DIGIT HEIGHT, 14-SEGMENT CHARACTER.
- WIDE SUPPLY VOLTAGE OPERATION.
- SERIES DATA INPUT.
- CONSTANT CURRENT DRIVERS.
- CONTINUOUS BRIGHTNESS CONTROL.
- SOLID STATE RELIABILITY, LONG OPERATION LIFE.
- WIDE VIEWING ANGLE.
- CHOICE OF FIVE BRIGHT COLORS-RED/BRIGHT RED/GREEN/ORANGE/HIGH EFFICIENCY RED.
- TTL COMPATIBLE.



INTELLIGENT DISPLAY & LED DISPLAYS WITH DRIVER IC BUILT-IN

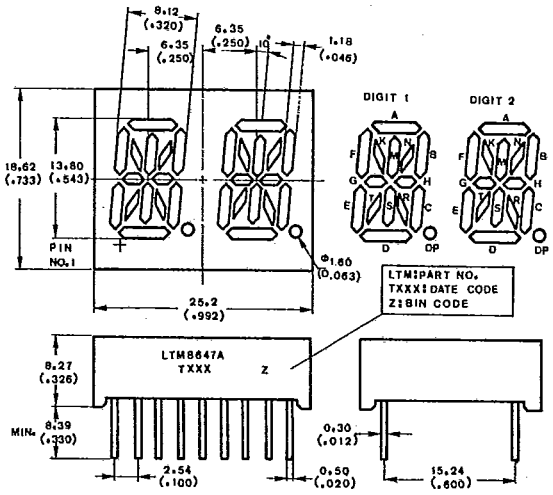
DESCRIPTION

The LTM-8647A series are dual character 14-segment alphanumeric display modules, having a built-in M5450 MOS integrated circuits. The integrated circuit contains series data input, 35 bit shift registers, 34 LED driver outputs and a brightness control. The red devices utilized LED chips which are made from GaAsP on a GaAs substrate. The bright red and green devices utilized LED chips which are made from GaP on a transparent GaP substrate. The orange and high efficiency red devices utilized LED chips which are made from GaAsP on a transparent GaP substrast. The MOS integrated circuits produced with N-channel silicon gate technology. Red and bright red displays have black face and red segment color. Green and orange displays have gray face and white segment color. High efficiency red displays have red face and red segment color.

DEVICES

PART NO. LTM-					DESCRIPTION
RED	BRIGHT RED	GREEN	ORANGE	HI.-EFF. RED	
8647AR	8647AP	8647AG	8647AE	8647AHR	Dual Character, with I.C. Driver

PACKAGE DIMENSIONS



NOTE: All dimensions are in $\frac{\text{millimeters}}{\text{(inches)}}$, tolerance is $\frac{\text{0.25mm}}{\text{(0.010")}}$ unless otherwise noted.

PACKAGE PIN CONNECTION

PIN NO.	CONNECTION	PIN NO.	CONNECTION
1	Bit 32 Output	10	No. Pin
2	Bit 33 Output	11	No. Pin
3	Bit 34 Output	12	No. Pin
4	Data Input	13	Vss* 1
5	Clock Input	14	Vss* 1
6	Data Enable	15	No. Pin
7	V_{DD}	16	No. Pin
8	V_{LED}	17	Bit 31 Output
9	Brt Control	18	No. Pin

NOTE: Pin 13 & 14 are internally connected.

ABSOLUTE MAXIMUM RATING AT T_A = 25°C

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage *1	V_{DD}	–0.3	15	V
Input Voltage	VI	–0.3	15	V
Off State Output Voltage	Vo (off)		15	V
LED Supply Voltage	V_{LED}	2.8	3.5	V
Power Dissipation of IC *2	P_D (IC)		350	mW
Supply Current	I_{DD}		7	mA
operating Temperature Range	Top	–20	+60	°C
Storage Temperature Range	Tstg	–20	+60	°C
Solder Temperature 1/16 Inch Below Seating Plane for 3 Seconds at 260°C				

NOTES: 1. All voltages are with respect to Vss (GND)
2. Power dissipation of IC is given by $P_D = (V_{LED} - V_F) \bullet (I_F) \bullet (\text{No. of Segments}) + (7mA) \bullet V_{DD})$
*V_F is LED forward voltage.

INTELLIGENT DISPLAY & LED DISPLAYS WITH DRIVER IC BUILT-IN

RECOMMENDED OPERATING CONDITION AT T_A = 25°C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Voltage	V_{DD}	4.75		13.2	V	
Input Voltage						
Logical "0" Level		–0.3		0.8	V	±10μA Input Bias
Logical "1" Level	VI	2.2		V_{DD}	V	4.75V < V < 5.25V
Logical "1" Level		V_{DD}-2		V_{DD}	V	V_{DD} > 5.25V
Brightness Input Current	I_B	0	0.75	mA		
Brightness Input Voltage	V_B	3		4.3	V	Input Current = 750μA
Off State Voltage	Vo (off)			13.2	V	
Output Sink Current						
Segment Off				10	μA	I_B = 0μA
Segment On			3		mA	I_B = 100μA
			6		mA	I_B = 200μA
Input Clock Frequency	F_{CLOCK}	0		0.5	MHZ	
Output Matching	Io			±20	%	

ELECTRICAL/OPTICAL CHARACTERISTICS AT T_A = 25°C

LTM-8647AR

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv	200	400		μcd	I_B = 0.4 mA
Peak Emission Wavelength	λp		655		nm	I_B = 0.4 mA
Spectral Line Half-Width	Δλ		24		nm	I_B = 0.4 mA
Luminous Intensity Matching Ratio	Iv-m			2.1		I_B = 0.4 mA

Note: The BIN brightness classification see page 4-28, category B

LTM-8647AP

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv	300	650		μcd	I_B = 0.4 mA
Peak Emission Wavelength	λp		697		nm	I_B = 0.4 mA
Spectral Line Half-Width	Δλ		90		nm	I_B = 0.4 mA
Luminous Intensity Matching Ratio	Iv-m			2.1		I_B = 0.4 mA

Note: The BIN brightness classification see page 4-28, category B

LTM-8647AG

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv	600	1800		μcd	I_B = 0.4 mA
Peak Emission Wavelength	λp		565		nm	I_B = 0.4 mA
Spectral Line Half-Width	Δλ		30		nm	I_B = 0.4 mA
Luminous Intensity Matching Ratio	Iv-m			2.1		I_B = 0.4 mA

Note: The BIN brightness classification see page 4-28, category B

LTM-8647AE

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv	600	1800		μcd	I_B = 0.4 mA
Peak Emission Wavelength	λp		630		nm	I_B = 0.4 mA
Spectral Line Half-Width	Δλ		40		nm	I_B = 0.4 mA
Luminous Intensity Matching Ratio	Iv-m			2.1		I_B = 0.4 mA

Note: The BIN brightness classification see page 4-28, category B

LTM-8647AHR

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv	600	1800		μcd	IB = 0.4 mA
Peak Emission Wavelength	λp		635		nm	IB = 0.4 mA
Spectral Line Half-Width	Δλ		40		nm	IB = 0.4 mA
Luminous Intensity Matching Ratio	Iv-m			2:1		IB = 0.4 mA

Note: The BIN brightness classification see page 4-28, category B

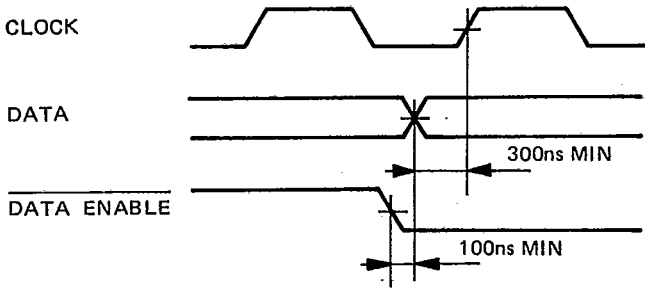
FUNCTIONAL DESCRIPTION

Serial data transfer from the data source to the display driver is accomplished with 2 signals serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complet, thus providing nonmultiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

Brightness of display is determined by control the output current of LED display. A InF capacitor should be connected to brightness control, Pin 9 to prevent possible oscillations. The output current is typically 25 times greater than the current into Pin 9 which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 1 shows the input data format. A start bit of logical "1" preceed the 35 bits of data. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generaled which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for master portion of the first register, thus allowing continous operation.

There must be a complete set of 36 clocks or the shift registers won't clear. When power is first applied to the chip an internal power ON reset signal is generated which reset all registers and all latches. The START bit and first clock return the chip on its normal operation. Bit 1 is the first following the start bit and it will appear on the segment A of the digit 1. A logical "1" at the input will turn on the appropriate LED. Figure 2 shows the timing relationship between data, clock, and DATA ENABLE. A max. clock frequency of 0.5 MHz is assumed.



FIGURE/Input data format. FIG. 1 Input data format.

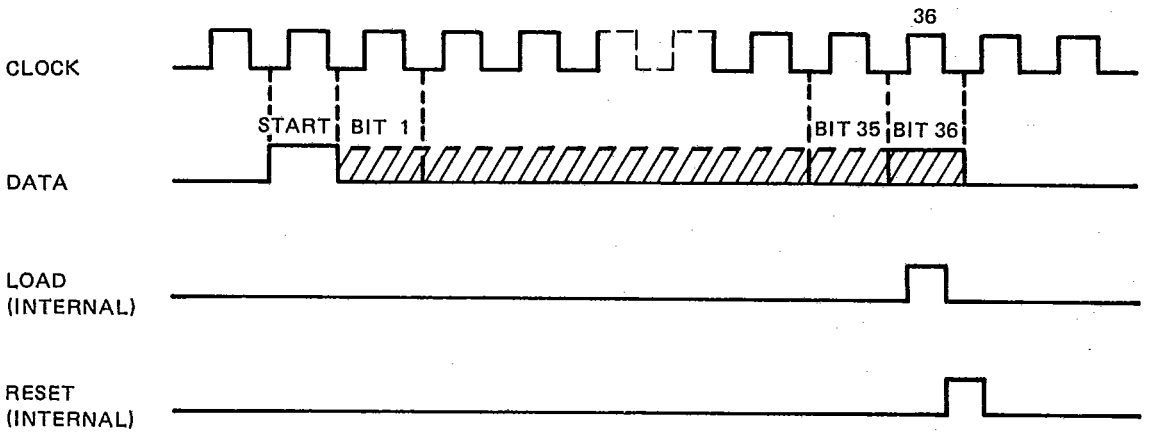


FIG. 2 Timing relationship

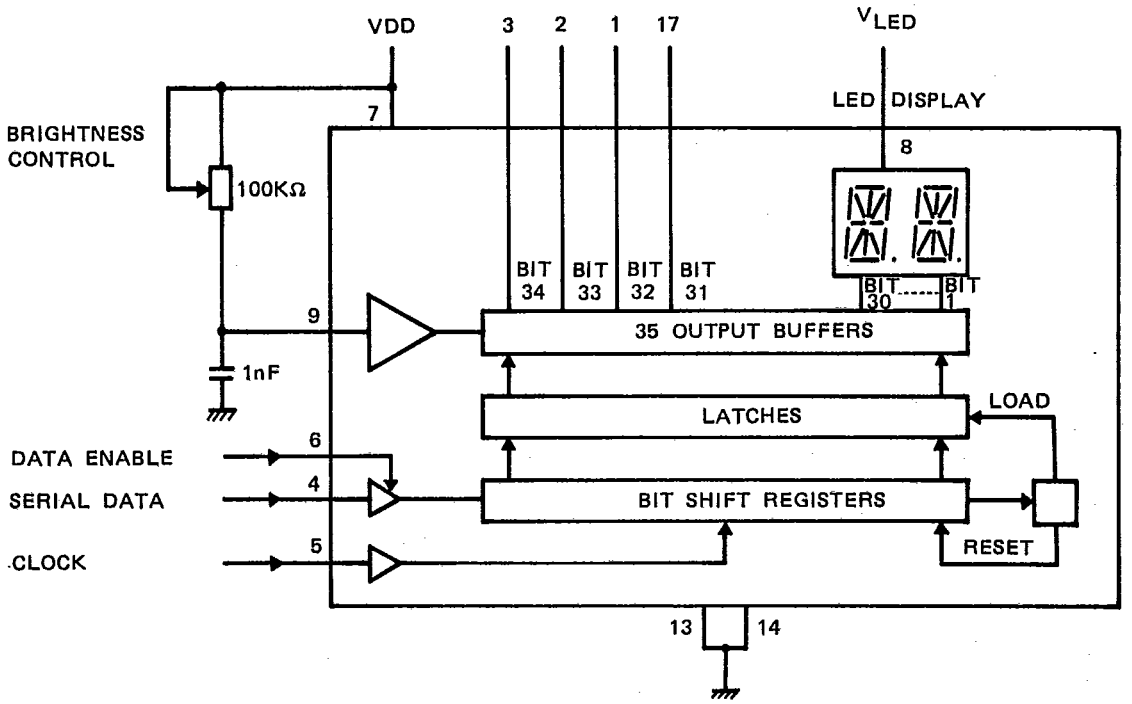


FIG. 3 Internal Block Diagram

TABLE I SERIAL DATA INPUT SEQUENCE

BIT	DIGIT	SEGMENT	BIT	DIGIT	SEGMENT
1	2	A	18	1	D
2	2	B	19	1	E
3	2	C	20	1	F
4	2	D	21	1	G
5	2	E	22	1	H
6	2	F	23	1	K
7	2	G	24	1	M
8	2	H	25	1	N
9	2	K	26	1	R
10	2	M	27	1	S
11	2	N	28	1	T
12	2	R	29	1	DP
13	2	S	30	2	DP
14	2	T	31		PIN 17
15	1	A	32		PIN 1
16	1	B	33		PIN 2
17	1	C	34		PIN 3