Dual HDMI Fast Switching Receiver with 12-Bit, 170 MHz Video and Graphics Digitizer and 3D Comb Filter Decoder

ADV7842

FEATURES

- Dual HDMI® 1.4a fast switching receiver
- HDMI support
  - 3D TV support
  - Content type bits
  - CEC 1.4-compatible
  - Extended colorimetry
- 256-ball, 17 mm × 17 mm BGA package
- HDMI 225 MHz receiver
  - Xpressview fast switching of HDMI ports
- 3D video format support including frame packing 1080p 24 Hz, 720p 50 Hz, 720p 60 Hz
  - Full colorimetry support including sYCC601, Adobe RGB, Adobe YCC 601
  - 36-/30-bit Deep Color and 24-bit color support
  - HDCP 1.4 support with internal HDCP keys
  - Adaptive HDMI equalizer
  - Integrated CEC controller
  - HDMI repeater support
  - 5 V detect and hot plug assert for each HDMI port
  - HDMI audio support including HBR and DSD
  - Advanced audio mute feature
  - Flexible digital audio output interfaces
  - Supports up to 5 S/PDIF outputs
  - Supports up to 4 I^2S outputs
- Video and graphics digitizer
  - Four 170 MHz, 12-bit ADCs
  - 12-channel analog input mux
  - 525i-/625i-component analog input
  - 525p-/625p-component progressive scan support
  - 720p-/1080i-/1080p-component HDTV support
  - Low refresh rates (24 Hz/25 Hz/30 Hz) support for 720p/1080p
  - Digitizes RGB graphics up to 1600 × 1200 at 60 Hz (UXGA)
  - SCART fast blank support
- 3D video decoder
  - NTSC/PAL/SECAM color standards support
  - NTSC/PAL 2D/3D motion detecting comb filter
  - Advanced time-base correction (TBC) with frame synchronization
  - Interlaced-to-progressive conversion for 525i and 625i
  - IF compensation filters
  - Vertical peaking and horizontal peaking filters
  - Robust synchronization extraction for poor video source
- Advanced VBI data slicer
- General
  - Highly flexible 36-bit pixel output interface
  - Internal EDID RAM for HDMI and graphics
  - Dual STDI (standard identification) function support
  - Any-to-any, 3 × 3 color space conversion (CSC) matrix
  - 2 programmable interrupt request output pins
  - Simultaneous analog processing and HDMI monitoring

APPLICATIONS

- Advanced TVs
  - PDP HDTVs, LCD TVs (HDTV ready)
  - LCD/DLP® rear projection HDTVs
  - CRT HDTVs, LCoS™ HDTVs
- AVR video receivers
- LCD/DLP front projectors
- HDTV STBs with PVR
- Projectors

FUNCTIONAL BLOCK DIAGRAM

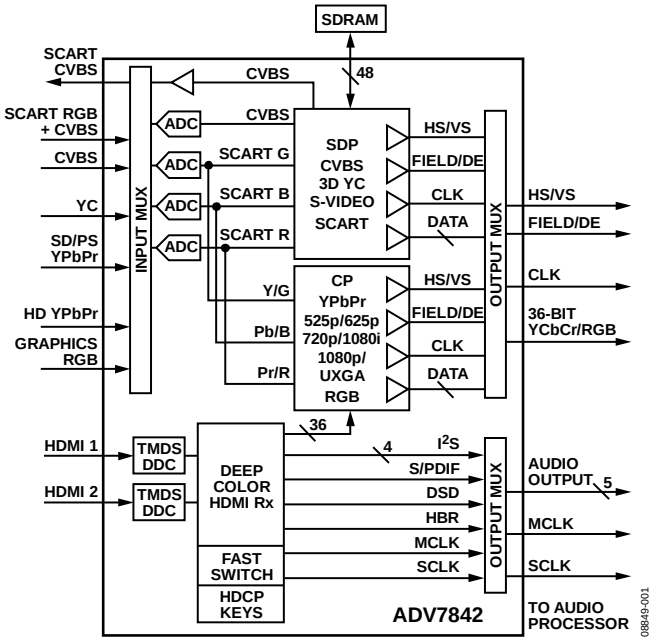

Figure 1.

Advantiv® Advanced Television Solutions by Analog Devices

Xpressview™ Fast Switching Technology by Analog Devices

Rev. B

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REVISION HISTORY

1/11—Rev. SpA to Rev. B

Updated Revision Number ... Universal
Updated Publication Code ... 28

10/10—Rev. Sp0 to Rev. SpA

Changes to Product Title and Features Section ... 1
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6/10—Revision Sp0: Initial Version

GENERAL DESCRIPTION

The ADV7842 is a high quality, single-chip, 2:1 multiplexed HDMI™ receiver and graphics digitizer with an integrated multiformat video decoder.

The ADV7842 incorporates a dual input HDMI 1.4-compatible receiver that supports all HDTV formats up to 1080p and display resolutions up to UXGA (1600 × 1200 at 60 Hz).

The ADV7842 incorporates Xpressview™ fast switching on both input HDMI ports. Using the Analog Devices, Inc., hardware-based HDCP engine that minimizes software overhead, Xpressview technology allows fast switching between any HDMI input ports in less than 1 second.

The ADV7842 supports all mandatory HDMI 1.4 3D TV formats in addition to all HDTV formats up to 1080p, 36-bit Deep Color.

The ADV7842 also integrates an HDMI v1.4 CEC controller that supports the capability discovery and control (CDC) feature.

The ADV7842 offers a flexible audio output port for the audio data decoded from the HDMI stream. HDMI audio formats, including super audio CD (SACD) via DSD and HBR are supported.

Each HDMI port has dedicated 5 V detect and hot plug assert pins. The HDMI receiver also includes an integrated equalizer that ensures robust operation of the interface with cable lengths up to 30 meters. The HDMI receiver has advanced audio functionality, such as a mute controller, that prevents audible extraneous noise in the audio output.

The multiformat 3D comb filter decoder supports the conversion of PAL, NTSC, and SECAM standards in the form of a composite or an S-Video input signal into a digital ITU-R BT.656 format. SCART and overlay functionality are enabled by the ability of the ADV7842 to process CVBS and standard definition RGB signals simultaneously.

The ADV7842 contains one main component processor (CP) that processes YPbPr and RGB component formats, including RGB graphics. The CP also processes the video signals from the HDMI receiver. The ADV7842 can operate in dual HDMI and analog input mode, thus allowing for fast switching between the ADCs and HDMI.

The ADV7842 supports the decoding of a component RGB/YPbPr video signal into a digital YCbCr or RGB pixel output stream. The support for component video includes 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, and 1250i standards, as well as many other SMPTE and HD standards.

The ADV7842 supports graphics digitization. The ADV7842 is capable of digitizing RGB graphics signals from VGA to UXGA rates and converting them into a digital RGB or YCbCr pixel output stream. Internal EDID is available for one graphic port.

Fabricated in an advanced CMOS process, the ADV7842 is provided in a 17 mm × 17 mm, 256-ball, BGA, surface-mount, RoHS-compliant package and is specified over the −10°C to +70°C temperature range.

DETAILED FUNCTIONAL BLOCK DIAGRAM

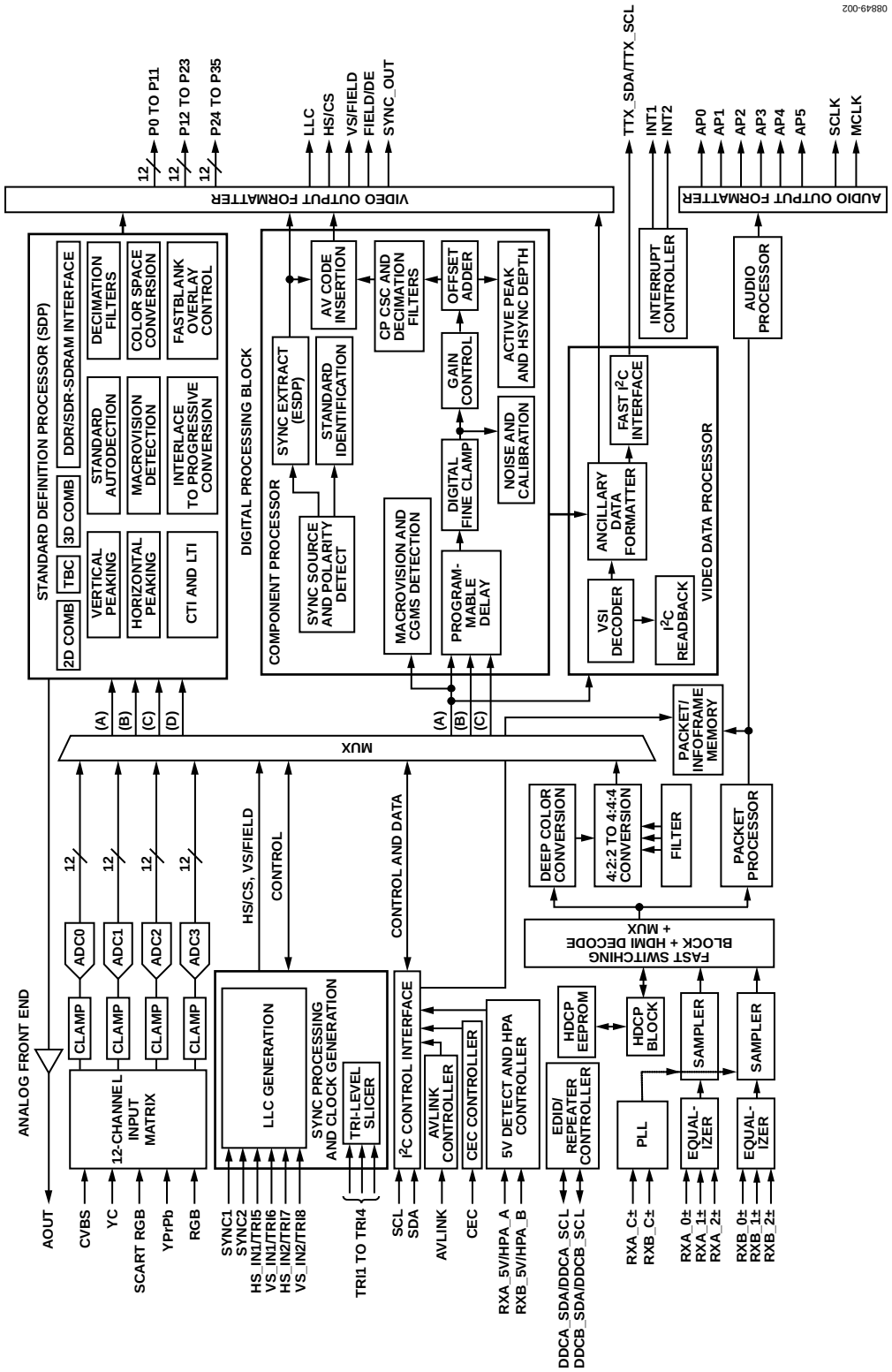


Figure 2. Detailed Functional Block Diagram

SPECIFICATIONS

AVDD = 1.8 V ± 5%, CVDD = 1.8 V ± 5%, DVDD = 1.8 V ± 5%, PVDD = 1.8 V ± 5%, DVDDIO = 3.3 V ± 5%, TVDD = 3.3 V ± 5%, VDD_SDRAM = 3.2 V to 3.4 V (SDR), VDD_SDRAM = 2.35 V to 2.65 V (DDR). T_{MIN} to T_{MAX} = −10°C to +70°C, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
Resolution (Each ADC)	N				12	Bits
Integral Nonlinearity	INL	27 MHz (at a 12-bit level)		−3.0 to +8.0		LSB
		54 MHz (at a 12-bit level)		−3.0 to +8.0		LSB
		74.25 MHz (at a 12-bit level)		−4.0 to +7.0		LSB
		108 MHz (at a 11-bit level)		−3.5 to +8.0		LSB
		170 MHz (at a 9-bit level)		−0.7 to +1.5		LSB
Differential Nonlinearity	DNL	27 MHz (at a 12-bit level)		−0.7 to +0.8		LSB
		54 MHz (at a 12-bit level)		−0.7 to +0.8		LSB
		75 MHz (at a 12-bit level)		−0.7 to +0.8		LSB
		108 MHz (at a 11-bit level)		−0.7 to +0.8		LSB
		170 MHz (at a 9-bit level)		−0.6 to +0.5		LSB
DIGITAL INPUTS						
Input High Voltage	V_{IH}	XTALN and XTALP pins	1.2			V
Input Low Voltage	V_{IL}	XTALN and XTALP pins			0.4	V
	V_{IH}	Other digital inputs	2			V
	V_{IL}	Other digital inputs			0.8	V
Input Current	I_{IN}	$\overline{\text{RESET}}$ pin			±60	µA
		EP_MISO pin			±60	µA
		SPDIF_IN pin			±60	µA
		TEST4 pin			±60	µA
		TEST6 pin			±60	µA
		Other digital inputs			±10	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL INPUTS (5 V TOLERANT)[1]						
Input High Voltage	V_{IH}		2.6			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}		−82		+82	µA
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}		2.4			V
Output Low Voltage	V_{OL}				0.4	V
High Impedance Leakage Current	I_{LEAK}			10		µA
Output Capacitance	C_{OUT}				20	pF

[1] The following pins are 5 V tolerant: HS_IN1/TRI5, HS_IN2/TRI7, VS_IN1/TRI6, VS_IN2/TRI8, RXA_5V, RXB_5V, DDCA_SCL, DDCA_SDA, DDCB_SCL, and DDCB_SDA.

POWER SPECIFICATIONS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS						
Digital Core Power Supply	VDD	1.75	1.8	1.85	V	
Digital I/O Power Supply	DVDDIO	3.14	3.3	3.46	V	
SDRAM Power Supply	VDD_SDRAM	3.2	3.3	3.4	V	SDR memory
	VDD_SDRAM	2.35	2.5	2.65	V	DDR memory
PLL Power Supply	PVDD	1.71	1.8	1.89	V	
Analog Power Supply	AVDD	1.71	1.8	1.89	V	
Terminator Power Supply	TVDD	3.14	3.3	3.46	V	
Comparator Power Supply	CVDD	1.71	1.8	1.89	V	
CURRENT CONSUMPTION[1, 2, 3]						
Digital Core Supply Current	I_{VDD}		155	220	mA	Analog 1080p sampling at 148 MHz
			148	196	mA	RGB graphics sampling at 162 MHz
			285	343	mA	RGB graphics sampling at 162 MHz in simultaneous mode with both background ports enabled
			163	176	mA	HDMI 1080p: 12-bit Deep Color
			216	273	mA	HDMI 1080p: 12-bit Deep Color in simultaneous mode with both background ports enabled
			194	230	mA	CVBS processing
			332	378	mA	CVBS processing in simultaneous mode with both background ports enabled
			57	72	mA	SD 576i component processing
			197	224	mA	SD 576i component processing in simultaneous mode with both background ports enabled
			270	289	mA	SCART processing
			404	435	mA	SCART processing in simultaneous mode with both background ports enabled
Digital I/O Supply Current	I_{DVDDIO}		51	109	mA	Analog 1080p sampling at 148 MHz
			41	129	mA	RGB graphics sampling at 162 MHz
			45	117	mA	RGB graphics sampling at 162 MHz in simultaneous mode with both background ports enabled
			27	32	mA	HDMI 1080p: 12-bit Deep Color
			22	150	mA	HDMI 1080p: 12-bit Deep Color in simultaneous mode with both background ports enabled
			9	11	mA	CVBS processing
			10	11	mA	CVBS processing in simultaneous mode with both background ports enabled
			8	11	mA	SD 576i component processing
			8	11	mA	SD 576i component processing in simultaneous mode with both background ports enabled
			10	11	mA	SCART processing
			10	12	mA	SCART processing in simultaneous mode with both background ports enabled

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
PLL Supply Current	I_{PVDD}		28	30	mA	Analog 1080p sampling at 148 MHz
			25	27	mA	RGB graphics sampling at 162 MHz
			25	28	mA	RGB graphics sampling at 162 MHz in simultaneous mode with both background ports enabled
			35	36	mA	HDMI 1080p: 12-bit Deep Color
			35	38	mA	HDMI 1080p: 12-bit Deep Color in simultaneous mode with both background ports enabled
			34	37	mA	CVBS processing
			35	37	mA	CVBS processing in simultaneous mode with both background ports enabled
			22	24	mA	SD 576i component processing
			22	24	mA	SD 576i component processing in simultaneous mode with both background ports enabled
			34	37	mA	SCART processing
			35	37	mA	SCART processing in simultaneous mode with both background ports enabled
Analog Supply Current	I_{AVDD}		279	295	mA	Analog 1080p sampling at 148 MHz
			281	297	mA	RGB graphics sampling at 162 MHz
			285	301	mA	RGB graphics sampling at 162 MHz in simultaneous mode with both background ports enabled
			0.1	0.3	mA	HDMI 1080p: 12-bit Deep Color
			0.1	0.3	mA	HDMI 1080p: 12-bit Deep Color in simultaneous mode with both background ports enabled
			85	89	mA	CVBS processing
			86	91	mA	CVBS processing in simultaneous mode with both background ports enabled
			267	281	mA	SD 576i component processing
			270	285	mA	SD 576i component processing in simultaneous mode with both background ports enabled
			283	294	mA	SCART processing
			286	301		SCART processing in simultaneous mode with both background ports enabled
Terminator Supply Current[4]	I_{TVDD}		85	95	mA	One port connected
			120	135	mA	Two ports connected
Comparator Supply Current	I_{CVDD}		120	130	mA	HDMI 1080p: 12-bit Deep Color
			220	250	mA	HDMI 1080p: 12-bit Deep Color in simultaneous mode with both background ports enabled
Memory Interface Supply Current	I_{VDD_SDRAM}		28	35	mA	CVBS input sampling at 54 MHz
Power-Down Currents[5]	I_{DVDDIO}			0.1	mA	
	I_{VDD_SDRAM}			2.6	mA	
	I_{VDD}			10	mA	
	I_{AVDD}			0.1	mA	
	I_{CVDD}			0.5	mA	
	I_{TVDD}			1.1	mA	
	I_{PVDD}			1.7	mA	
Power-Up Time	t_{PWRUP}		25		ms	

[1] All maximum current values are guaranteed by characterization to assist in power supply design.
[2] Typical current consumption values are recorded with nominal voltage supply levels, SMPTE bar video pattern, and at room temperature.
[3] Maximum current consumption values are recorded with maximum rated voltage supply levels, MoireX video pattern, and at maximum rated temperature.
[4] Termination power supply includes TVDD current consumed off chip.
[5] Power-down mode entered by setting Bit POWER_DOWN high.

ANALOG SPECIFICATIONS

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLAMP CIRCUITRY[1]					
Input Impedance	Clamps switched off		10		MΩ
Analog (AIN1 – AIN12)					
ADC Midscale (CML)			0.91		V
ADC Full-Scale Level			CML + 0.55		V
ADC Zero-Scale Level			CML – 0.55		V
ADC Dynamic Range			1.1		V
Clamp Level (When Locked)	Component input, Y signal		CML – 0.12		V
	Component input, Pr signal		CML		V
	Component input, Pb signal		CML		V
	PC RGB input (R, G, B signals)		CML – 0.12		V
	CVBS input		CML – 0.205		V
	SCART RGB input (R, G, B signals)		CML – 0.205		V
	S-Video input (Y Signal)		CML – 0.205		V
	S-Video input (C Signal)		CML		V
Large Clamp Source Current	SDP only		0.3		mA
Large Clamp Sink Current	SDP only		0.4		mA
Fine Clamp Source Current	SDP only		9		µA
Fine Clamp Sink Current	SDP only		8		µA

[1] Specified for external clamp capacitor of 100 nF.

VIDEO SPECIFICATIONS

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS						
Differential Phase	DP	CVBS input (modulated five-step)		0.6		Degrees
Differential Gain	DG	CVBS input (modulated five-step)		0.8		%
Luma Nonlinearity	LNL	CVBS input (modulated five-step)		0.9		%
NOISE SPECIFICATIONS		Measured at 27 MHz LLC				
SNR Unweighted		Luma ramp		63		dB
SNR Unweighted		Luma flat field		64		dB
Analog Front-End Crosstalk				60		dB
LOCK TIME SPECIFICATIONS (SDP)						
Horizontal Lock Range				±5		%
Vertical Lock Range			40		70	Hz
Subcarrier Lock Range	f_{SC}			±0.8		kHz
Color Lock-In Time				60		Lines
Sync Depth Range[1]			20		200	%
Color Burst Range			1		200	%
Vertical Lock Time				300		ms
Horizontal Lock Time				100		Lines
CHROMA SPECIFICATIONS (SDP)						
Chroma Amplitude Error				0.9		%
Chroma Phase Error				0.3		Degrees
Chroma Luma Intermodulation				0.3		%

[1] Nominal synchronization depth is 300 mV at 100% of the synchronization depth range.

TIMING CHARACTERISTICS

Data and I²C Timing Characteristic

Table 5.

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK AND CRYSTAL						
Crystal Frequency, XTAL				28.63636		MHz
Crystal Frequency Stability					±50	ppm
Horizontal Sync Input Frequency			10		110	kHz
LLC Frequency Range			12.825		170	MHz
I²C PORTS						
SCL Frequency					400	kHz
SCL Minimum Pulse Width High	t_1		600			ns
SCL Minimum Pulse Width Low	t_2		1.3			µs
Start Condition Hold Time	t_3		600			ns
Start Condition Setup Time	t_4		600			ns
SDA Setup Time	t_5		100			ns
SCL and SDA Rise Time	t_6				1000	ns
SCL and SDA Fall Time	t_7				300	ns
Stop Condition Setup Time	t_8		0.6			µs
TTX I²C PORTS						
SCL Frequency					3.4	MHz
SCL Minimum Pulse Width High	t_1		60			ns
SCL Minimum Pulse Width Low	t_2		160			ns
Start Condition Hold Time	t_3		160			ns
Start Condition Setup Time	t_4		160			ns
SDA Setup Time	t_5		10			ns
SCL and SDA Rise Time	t_6		10		80	ns
SCL and SDA Fall Time	t_7		10		80	ns
Stop Condition Setup Time	t_8		160			ns
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark-Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS[2]						
Data Output Transition Time SDR (SDP)	t_{11}	End of valid data to negative clock edge		2.9	4.6	ns
Data Output Transition Time SDR (SDP)	t_{12}	Negative clock edge to start of valid data		0.2	0.6	ns
Data Output Transition Time SDR (CP)	t_{13}	End of valid data to negative clock edge		1.5	2.2	ns
Data Output Transition Time SDR (CP)	t_{14}	Negative clock edge to start of valid data		0.1	0.3	ns
I²S PORT, MASTER MODE						
SCLK Mark-Space Ratio	t_{15}:t_{16}		45:55		55:45	% duty cycle
LRCLK Data Transition Time	t_{17}	End of valid data to negative SCLK edge			10	ns
LRCLK Data Transition Time	t_{18}	Negative SCLK edge to start of valid data			10	ns
I2Sx Data Transition Time	t_{19}	End of valid data to negative SCLK edge			5	ns
I2Sx Data Transition Time	t_{20}	Negative SCLK edge to start of valid data			5	ns

[1] Guaranteed by characterization.
[2] With the DLL block on output clock bypassed.

TIMING DIAGRAMS

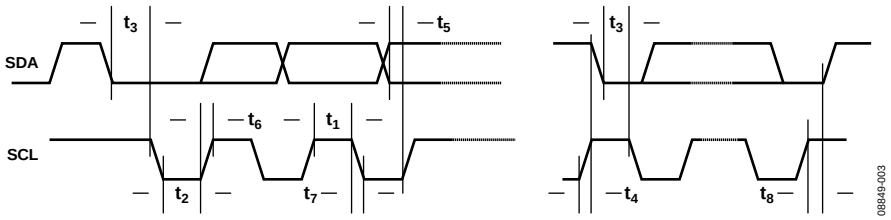


Figure 3. I²C Timing

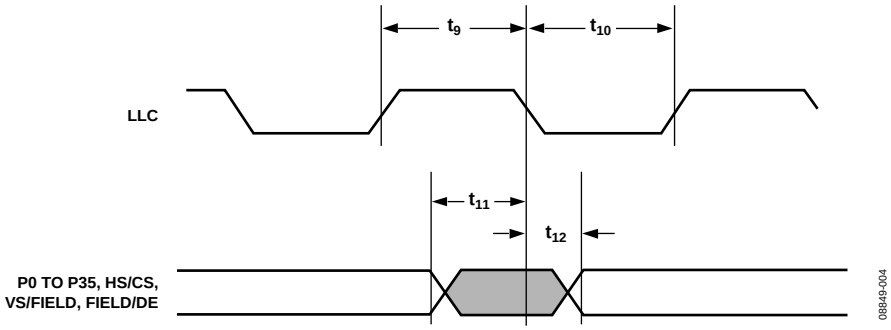


Figure 4. Pixel Port and Control SDR Output Timing (SDP)

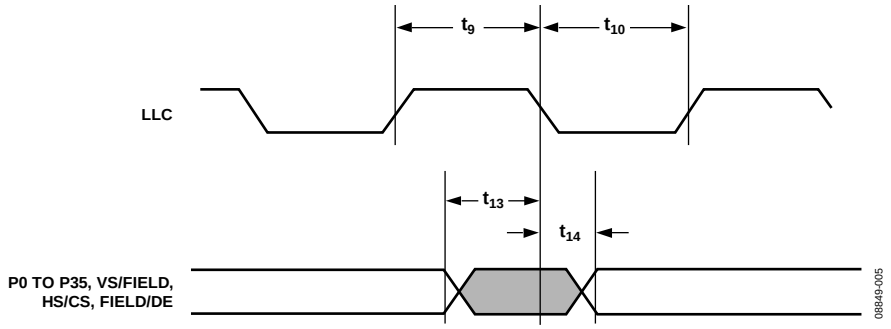
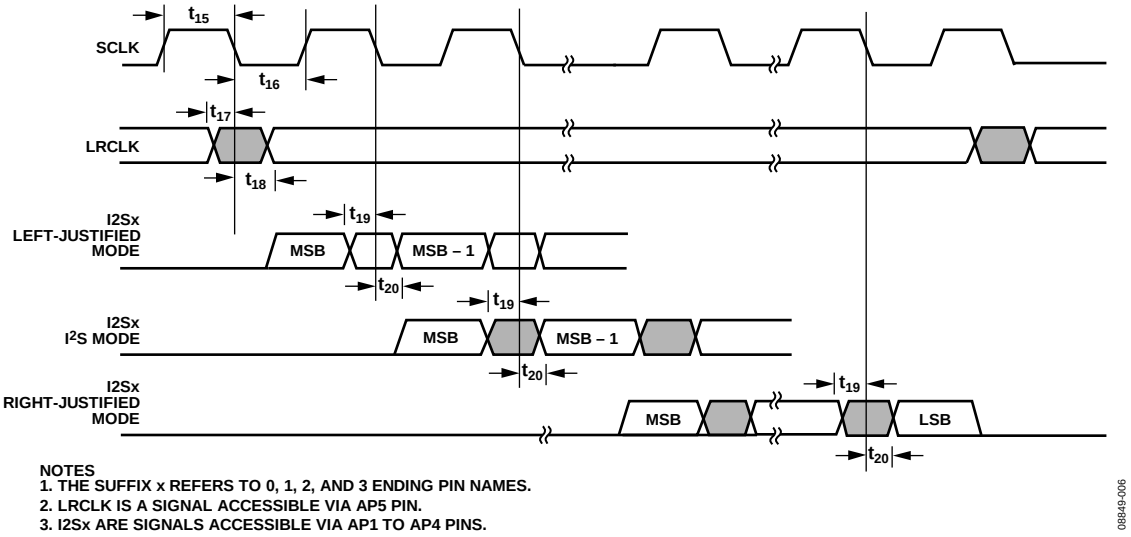


Figure 5. Pixel Port and Control SDR Output Timing (CP)



NOTES
1. THE SUFFIX x REFERS TO 0, 1, 2, AND 3 ENDING PIN NAMES.
2. LRCLK IS A SIGNAL ACCESSIBLE VIA AP5 PIN.
3. I2Sx ARE SIGNALS ACCESSIBLE VIA AP1 TO AP4 PINS.

Figure 6. I²S Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD to GND	2.2 V
VDD to GND	2.2 V
PVDD to GND	2.2 V
DVDDIO to GND	4.0 V
VDD_SDRAM to GND	4.0 V
CVDD to GND	2.2 V
TVDD to GND	4.0 V
AVDD to PVDD	−0.3 V to +0.3 V
AVDD to VDD	−0.3 V to +0.3 V
TVDD to CVDD	−0.3 V to +2.2 V
DVDDIO to VDD_SDRAM	−0.3 V to +3.3 V
VDD_SDRAM to AVDD	−0.3 V to +2 V
VDD_SDRAM to VDD	−0.3 V to +2 V
Digital Inputs Voltage to GND	−0.3 V to DVDDIO + 0.3 V
Digital Outputs Voltage to GND	−0.3 V to DVDDIO + 0.3 V
5 V Tolerant Digital Inputs to GND[1]	5.5 V
Analog Inputs to GND	−0.3 V to AVDD + 0.3 V
XTALN and XTALP to GND	−0.3 V to PVDD + 0.3 V
Maximum Junction Temperature ($T_{J\,MAX}$)	125°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

[1] The following inputs are 3.3 V inputs but are 5 V tolerant: HS_IN1/TRI5, HS_IN2/TRI7, VS_IN1/TRI6, VS_IN2/TRI8, DDCA_SCL, DDCA_SDA, DDCB_SCL and DDCB_SDA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the ADV7842, the user is advised to turn off unused sections of the part.

Due to PCB metal variation, and therefore variation in PCB heat conductivity, the value of θ_{JA} may differ for various PCBs.

The most efficient measurement solution is obtained using the package surface temperature to estimate the die temperature because this eliminates the variance associated with the $_{JA}\theta$ value.

The maximum junction temperature ($T_{J\,MAX}$) of 125°C must not be exceeded. The following equation calculates the junction temperature using the measured package surface temperature and applies only when no heat sink is used on the device under test (DUT):

$$T_J = T_S + \left(\Psi_{JT} \times W_{TOTAL}\right)$$

where:
T_S is the package surface temperature (°C).
Ψ_{JT} = 0.5°C/W for the 256-ball BGA.

$$W_{TOTAL} = (PVDD \times I_{PVDD}) + (0.4 \times TVDD \times I_{TVDD}) + (CVDD \times I_{CVDD}) + (AVDD \times I_{AVDD}) + (VDD \times I_{VDD}) + (A \times DVDDIO \times I_{DVDDIO}) + (VDD_SDRAM \times I_{VDD_SDRAM})$$

where:
0.4 reflects the 40% of TVDD power that is dissipated on the part itself.
A = 0.5 when the output pixel clock is >74 MHz.
A = 0.75 when the output pixel clock is ≤74 MHz.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

POWER SUPPLY SEQUENCING

POWER-UP SEQUENCE

The recommended power-up sequence of the ADV7842 is as follows:

1. 3.3 V supplies
2. 2.5 V supply (applies only if using DDR memory)
3. 1.8 V supplies

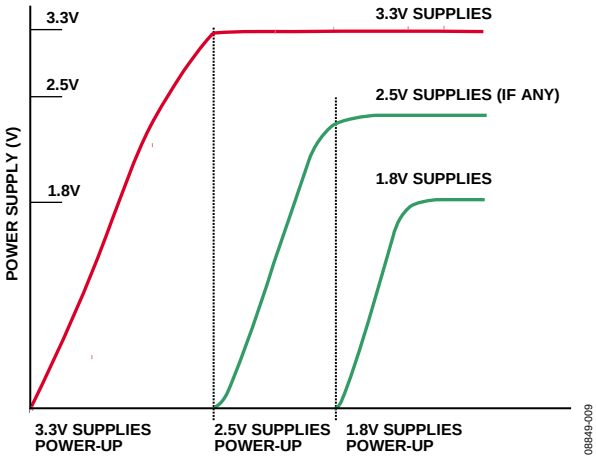


Figure 7. Recommended Power-Up Sequence

Notes

Reset should be held low while the supplies are being powered up.

- 3.3 V supplies should be powered up first.
- 2.5 V supply should be powered after the 3.3 V supplies are established but before the 1.8 V supplies.
- 1.8 V supplies should be powered up last.

The ADV7842 can alternatively be powered up by simultaneously asserting all supplies.

In this case, care must be taken to ensure that a lower rated supply does not go above a higher rated supply level, because the supplies are being established.

POWER-DOWN SEQUENCE

The ADV7842 supplies can be deasserted simultaneously as long as a higher rated supply does not go below a lower rated supply.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	GND	P3	P1	P0	TVDD	RXB_2–	RXB_1–	RXB_0–	RXB_C–	GND	RXA_2–	RXA_1–	RXA_0–	RXA_C–	TVDD	GND	A
B	P5	P4	P2	SYNC_OUT	TVDD	RXB_2+	RXB_1+	RXB_0+	RXB_C+	GND	RXA_2+	RXA_1+	RXA_0+	RXA_C+	TVDD	XTALP	B
C	P7	P6	VS/FIELD	HS/CS	GND	HPA_B	HPA_A	RXB_5V	RXA_5V	$\overline{\text{PWRDN1}}$	TEST8	CVDD	CVDD	CVDD	GND	XTALN	C
D	P9	P8	EP_MISO	FIELD/DE	GND	CEC	DDCB_SDA	DDCB_SCL	DDCA_SDA	DDCA_SCL	RTERM	CVDD	VGA_SCL	VGA_SDA	PVDD	PVDD	D
E	GND	P10	$\overline{\text{EP_CS}}$	EP_MOSI	GND	GND	GND	GND	GND	GND	CVDD	CVDD	HS_IN2/TRI7	VS_IN2/TRI8	REFP	REFN	E
F	P12	P11	EP_SCK	TTX_SCL	DVDDIO	GND	GND	GND	GND	GND	GND	AVDD	AIN12	AIN11	TRI4	TRI3	F
G	P14	P13	TTX_SDA	MCLK	DVDDIO	GND	GND	GND	GND	GND	GND	AVDD	AIN10	SYNC4	AIN9	AIN8	G
H	P16	P15	AP0	AP5	DVDDIO	GND	GND	GND	GND	GND	GND	AVDD	TRI1	TRI2	AIN7	SYNC3	H
J	P18	P17	SCLK	AP4	DVDDIO	GND	VDD	GND	GND	GND	GND	AVDD	AIN6	AIN4	SYNC2	GND	J
K	P20	P19	AP3	AP1	DVDDIO	VDD	VDD	VDD	VDD	GND	GND	AVDD	AIN5	VS_IN1/TRI6	AIN2	AIN3	K
L	P22	P21	SCL	AP2	DVDDIO	VDD	VDD	VDD	VDD	GND	GND	AVDD	AOUT	HS_IN1/TRI5	AIN1	SYNC1	L
M	GND	P23	SDA	INT1	DVDDIO	VDD_SDRAM	VDD_SDRAM	VDD_SDRAM	VDD_SDRAM	VDD_SDRAM	GND	GND	GND	GND	GND	GND	M
N	LLC	P24	INT2	TEST4	$\overline{\text{RESET}}$	TEST6	SDRAM_A8	SDRAM_A4	SDRAM_A0	$\overline{\text{SDRAM_CS}}$	SDRAM_LDQS	SDRAM_DQ4	SDRAM_DQ15	SDRAM_DQ11	SDRAM_CK	SDRAM_CKE	N
P	P25	P26	TEST5	AVLINK	TEST7	SDRAM_A11	SDRAM_A7	SDRAM_A3	SDRAM_A10	$\overline{\text{SDRAM_RAS}}$	SDRAM_DQ7	SDRAM_DQ3	SDRAM_VREF	SDRAM_DQ12	SDRAM_UDQS	$\overline{\text{SDRAM_CK}}$	P
R	P27	P28	P30	P32	P34	SDRAM_A9	SDRAM_A6	SDRAM_A2	SDRAM_BA1	$\overline{\text{SDRAM_CAS}}$	SDRAM_DQ6	SDRAM_DQ2	SDRAM_DQ0	SDRAM_DQ13	SDRAM_DQ9	SDRAM_DQ8	R
T	GND	P29	P31	P33	P35	GND	SDRAM_A5	SDRAM_A1	SDRAM_BA0	$\overline{\text{SDRAM_WE}}$	SDRAM_DQ5	GND	SDRAM_DQ1	SDRAM_DQ14	SDRAM_DQ10	GND	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

08849-007

Figure 8. Pin Configuration (Top View)

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	GND	Ground	Ground.
A2	P3	Digital video output	Video Pixel Output Port.
A3	P1	Digital video output	Video Pixel Output Port.
A4	P0	Digital video output	Video Pixel Output Port.
A5	TVDD	Power	Terminator Supply Voltage (3.3 V).
A6	RXB_2−	HDMI input	Digital Input Channel 2 Complement of Port B in the HDMI Interface.
A7	RXB_1−	HDMI input	Digital Input Channel 1 Complement of Port B in the HDMI Interface.
A8	RXB_0−	HDMI input	Digital Input Channel 0 Complement of Port B in the HDMI Interface.
A9	RXB_C−	HDMI input	Digital Input Clock Complement of Port B in the HDMI Interface.
A10	GND	Ground	Ground.
A11	RXA_2−	HDMI input	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
A12	RXA_1−	HDMI input	Digital Input Channel 1 Complement of Port A in the HDMI Interface.
A13	RXA_0−	HDMI input	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
A14	RXA_C−	HDMI input	Digital Input Clock Complement of Port A in the HDMI Interface.
A15	TVDD	Power	Terminator Supply Voltage (3.3 V).
A16	GND	Ground	Ground.
B1	P5	Digital video output	Video Pixel Output Port.
B2	P4	Digital video output	Video Pixel Output Port.
B3	P2	Digital video output	Video Pixel Output Port.
B4	SYNC_OUT	Miscellaneous digital	Sliced Synchronization Output
B5	TVDD	Power	Terminator Supply Voltage (3.3 V).
B6	RXB_2+	HDMI input	Digital Input Channel 2 True of Port B in the HDMI Interface.
B7	RXB_1+	HDMI input	Digital Input Channel 1 True of Port B in the HDMI Interface.
B8	RXB_0+	HDMI input	Digital Input Channel 0 True of Port B in the HDMI Interface.
B9	RXB_C+	HDMI input	Digital Input Clock True of Port B in the HDMI Interface.
B10	GND	Ground	Ground.
B11	RXA_2+	HDMI input	Digital Input Channel 2 True of Port A in the HDMI Interface.
B12	RXA_1+	HDMI input	Digital Input Channel 1 True of Port A in the HDMI Interface.
B13	RXA_0+	HDMI input	Digital Input Channel 0 True of Port A in the HDMI Interface.
B14	RXA_C+	HDMI input	Digital Input Clock True of Port A in the HDMI Interface.
B15	TVDD	Power	Terminator Supply Voltage (3.3 V).
B16	XTALP	Miscellaneous analog	Input pin for 28.63636 MHz crystal or external 1.8V, 28.63636 MHz Clock Oscillator Source to Clock the ADV7842.
C1	P7	Digital video output	Video Pixel Output Port.
C2	P6	Digital video output	Video Pixel Output Port.
C3	VS/FIELD	Digital video output	Vertical Synchronization/Field Synchronization. VS is a vertical synchronization output signal in the CP and HDMI processor. FIELD is a field synchronization output signal in all interlaced video modes. VS or FIELD can be configured for this pin.
C4	HS/CS	Digital video output	Horizontal Synchronization/Composite Synchronization. HS is a horizontal synchronization output signal in the CP and HDMI processor. CS (composite synchronization) signal is a single signal containing both horizontal and vertical synchronization pulses. HS or CS can be configured for this pin.
C5	GND	Ground	Ground.
C6	HPA_B	Miscellaneous digital	Hot Plug Assert Signal Output for HDMI Port B.
C7	HPA_A	Miscellaneous digital	Hot Plug Assert Signal Output for HDMI Port A.
C8	RXB_5V	HDMI input	5 V Detect Pin for Port B in the HDMI Interface.
C9	RXA_5V	HDMI input	5 V Detect Pin for Port A in the HDMI Interface.
C10	$\overline{\text{PWRDN1}}$	Miscellaneous digital	Controls the Power-Up of the ADV7842. Should be connected to a digital 3.3 V I/O supply to power up the ADV7842.
C11	TEST8	Test pin	Tie this pin to ground via 4.7 kΩ resistor.
C12	CVDD	Power	Comparator Supply Voltage (1.8 V).
C13	CVDD	Power	Comparator Supply Voltage (1.8 V).
C14	CVDD	Power	Comparator Supply Voltage (1.8 V).

Pin No.	Mnemonic	Type	Description
C15	GND	Ground	Ground.
C16	XTALN	Miscellaneous analog	Input Pin for 28.63636 MHz Crystal.
D1	P9	Digital video output	Video Pixel Output Port.
D2	P8	Digital video output	Video Pixel Output Port.
D3	EP_MISO	Digital input	SPI Master In/Slave Out for External EDID Interface.
D4	FIELD/DE	Miscellaneous digital	Data Enable (DE). DE is a signal that indicates active pixel data. Field Synchronization Output Signal in All Interlaced Video Modes (FIELD). DE or FIELD can be configured for this pin.
D5	GND	Ground	Ground.
D6	CEC	Digital input/output	Consumer Electronic Control Channel.
D7	DDCB_SDA	Digital input/output	HDCP Slave Serial Data Port B. DDCB_SDA is a 3.3 V input/output that is 5 V tolerant.
D8	DDCB_SCL	Digital input	HDCP Slave Serial Clock Port B. DDCB_SCL is a 3.3 V input that is 5 V tolerant.
D9	DDCA_SDA	Digital input/output	HDCP Slave Serial Data Port A. DDCA_SDA is a 3.3 V input/output that is 5 V tolerant.
D10	DDCA_SCL	Digital input	HDCP Slave Serial Clock Port A. DDCA_SCL is a 3.3 V input that is 5 V tolerant.
D11	RTERM	Miscellaneous analog	Sets Internal Termination Resistance. A 500 Ω resistor between this pin and GND should be used.
D12	CVDD	Power	Comparator Supply Voltage (1.8 V).
D13	VGA_SCL	Miscellaneous digital	DDC Port Serial Clock Input for VGA
D14	VGA_SDA	Miscellaneous digital	DDC Port Serial Data Input/Output for VGA
D15	PVDD	Power	PLL Supply Voltage (1.8 V).
D16	PVDD	Power	PLL Supply Voltage (1.8 V).
E1	GND	Ground	Ground.
E2	P10	Digital video output	Video Pixel Output Port.
E3	$\overline{\text{EP_CS}}$	Digital output	SPI Chip Select for External EDID Interface.
E4	EP_MOSI	Digital output	SPI Master Out/Slave In for External EDID Interface.
E5	GND	Ground	Ground.
E6	GND	Ground	Ground.
E7	GND	Ground	Ground.
E8	GND	Ground	Ground.
E9	GND	Ground	Ground.
E10	GND	Ground	Ground.
E11	CVDD	Power	Comparator Supply Voltage (1.8 V).
E12	CVDD	Power	Comparator Supply Voltage (1.8 V).
E13	HS_IN2/TRI7	Miscellaneous analog	HS on Graphics Port 2 (HS_IN2). The HS input signal is used for 5-wire timing mode. Trilevel/Bilevel Input on the SCART or D-terminal Connector (TRI7). (Selection available via the I^2C.)
E14	VS_IN2/TRI8	Miscellaneous analog	VS on Graphics Port 2 (VS_IN2). The VS input signal is used for 5-wire timing mode. Trilevel/Bilevel Input on the SCART or D-Terminal Connector (TRI8). (Selection available via the I^2C.)
E15	REFP	Miscellaneous analog	Internal Voltage Reference Output.
E16	REFN	Miscellaneous analog	Internal Voltage Reference Output.
F1	P12	Digital video output	Video Pixel Output Port.
F2	P11	Digital video output	Video Pixel Output Port.
F3	EP_SCK	Digital output	SPI Clock for External EDID Interface.
F4	TTX_SCL	Miscellaneous digital	Fast I^2C Interface for Teletext Data Extraction. TTX_SCL is used as the I^2C port serial clock input.
F5	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
F6	GND	Ground	Ground.
F7	GND	Ground	Ground.
F8	GND	Ground	Ground.
F9	GND	Ground	Ground.
F10	GND	Ground	Ground.
F11	GND	Ground	Ground.
F12	AVDD	Power	Analog Supply Voltage (1.8 V).

Pin No.	Mnemonic	Type	Description
F13	AIN12	Analog video input	Analog Video Input Channel.
F14	AIN11	Analog video input	Analog Video Input Channel.
F15	TRI4	Miscellaneous analog	Trilevel or Bilevel Input on the SCART or D-Type Connector. (Selection available via the I^2C.)
F16	TRI3	Miscellaneous analog	Trilevel or Bilevel Input on the SCART or D-Type Connector. (Selection available via the I^2C.)
G1	P14	Digital video output	Video Pixel Output Port.
G2	P13	Digital video output	Video Pixel Output Port.
G3	TTX_SDA	Miscellaneous digital	Fast I^2C Interface for Teletext Data Extraction. TTX_SDA is used as the I^2C port serial data input/output pins.
G4	MCLK	Miscellaneous	Audio Master Clock Output.
G5	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
G6	GND	Ground	Ground.
G7	GND	Ground	Ground.
G8	GND	Ground	Ground.
G9	GND	Ground	Ground.
G10	GND	Ground	Ground.
G11	GND	Ground	Ground.
G12	AVDD	Power	Analog Supply Voltage (1.8 V).
G13	AIN10	Analog video input	Analog Video Input Channel.
G14	SYNC4	Miscellaneous analog	This is a synchronization on green or luma input (SOG/SOY) used in embedded synchronization mode. User configurable.
G15	AIN9	Analog video input	Analog Video Input Channel.
G16	AIN8	Analog video input	Analog Video Input Channel.
H1	P16	Digital video output	Video Pixel Output Port.
H2	P15	Digital video output	Video Pixel Output Port.
H3	AP0	Miscellaneous	Audio Output Pin.
H4	AP5	Miscellaneous	Audio Output Pin.
H5	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
H6	GND	Ground	Ground.
H7	GND	Ground	Ground.
H8	GND	Ground	Ground.
H9	GND	Ground	Ground.
H10	GND	Ground	Ground.
H11	GND	Ground	Ground.
H12	AVDD	Power	Analog Supply Voltage (1.8 V).
H13	TRI1	Miscellaneous analog	Trilevel or Bilevel Input on the SCART or D-Type Connector. (Selection available via I^2C.)
H14	TRI2	Miscellaneous analog	Trilevel or Bilevel Input on the SCART or D-Type Connector. (Selection available via I^2C.)
H15	AIN7	Analog video input	Analog Video Input Channel.
H16	SYNC3	Miscellaneous analog	This is a synchronization on green or luma input (SOG/SOY) used in embedded synchronization mode. User configurable.
J1	P18	Digital video output	Video Pixel Output Port.
J2	P17	Digital video output	Video Pixel Output Port.
J3	SCLK	Miscellaneous digital	Audio Serial Clock Output.
J4	AP4	Miscellaneous	Audio Output Pin.
J5	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
J6	GND	Ground	Ground.
J7	VDD	Power	Digital Core Supply Voltage (1.8 V).
J8	GND	Ground	Ground.
J9	GND	Ground	Ground.
J10	GND	Ground	Ground.
J11	GND	Ground	Ground.
J12	AVDD	Power	Analog Supply Voltage (1.8 V).
J13	AIN6	Analog video input	Analog Video Input Channel.

Pin No.	Mnemonic	Type	Description
J14	AIN4	Analog video input	Analog Video Input Channel.
J15	SYNC2	Miscellaneous analog	This is a synchronization on green or luma input (SOG/SOY) used in embedded synchronization mode. User configurable.
J16	GND	Ground	Ground.
K1	P20	Digital video output	Video Pixel Output Port.
K2	P19	Digital video output	Video Pixel Output Port.
K3	AP3	Miscellaneous	Audio Output Pin.
K4	AP1	Miscellaneous	Audio Output Pin.
K5	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
K6	VDD	Power	Digital Core Supply Voltage (1.8 V).
K7	VDD	Power	Digital Core Supply Voltage (1.8 V).
K8	VDD	Power	Digital Core Supply Voltage (1.8 V).
K9	VDD	Power	Digital Core Supply Voltage (1.8 V).
K10	GND	Ground	Ground.
K11	GND	Ground	Ground.
K12	AVDD	Power	Analog Supply Voltage (1.8 V).
K13	AIN5	Analog video input	Analog Video Input Channel.
K14	VS_IN1/TRI6	Miscellaneous analog	VS on Graphics Port 1 (VS_IN1). The VS input signal is used for 5-wire timing mode. Trilevel/Bilevel Input on the SCART or D-Terminal Connector (TRI6). (Selection available via the I^2C.)
K15	AIN2	Analog video input	Analog Video Input Channel.
K16	AIN3	Analog video input	Analog Video Input Channel.
L1	P22	Digital video output	Video Pixel Output Port.
L2	P21	Digital video output	Video Pixel Output Port.
L3	SCL	Miscellaneous digital	I^2C Port Serial Clock Input. SCL is the clock line for the control port.
L4	AP2	Miscellaneous	Audio Output Pin.
L5	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
L6	VDD	Power	Digital Core Supply Voltage (1.8 V).
L7	VDD	Power	Digital Core Supply Voltage (1.8 V).
L8	VDD	Power	Digital Core Supply Voltage (1.8 V).
L9	VDD	Power	Digital Core Supply Voltage (1.8 V).
L10	GND	Ground	Ground.
L11	GND	Ground	Ground.
L12	AVDD	Power	Analog Supply Voltage (1.8 V).
L13	AOUT	Analog monitor output	Analog Monitor Output.
L14	HS_IN1/TRI5	Miscellaneous analog	HS on Graphics Port 1 (HS_IN1). The HS input signal is used for 5-wire timing mode. Trilevel/Bilevel Input on the SCART or D-Terminal Connector (TRI5). (Selection available via the I^2C.)
L15	AIN1	Analog video input	Analog Video Input Channel.
L16	SYNC1	Miscellaneous analog	This is a synchronization on green or luma input (SOG/SOY) used in embedded synchronization mode. User configurable.
M1	GND	Ground	Ground.
M2	P23	Digital video output	Video Pixel Output Port.
M3	SDA	Miscellaneous digital	I^2C Port Serial Data Input/Output Pin. SDA is the data line for the control port.
M4	INT1	Miscellaneous digital	Interrupt. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control.
M5	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
M6	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
M7	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
M8	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
M9	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
M10	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
M11	GND	Ground	Ground.

Pin No.	Mnemonic	Type	Description
M12	GND	Ground	Ground.
M13	GND	Ground	Ground.
M14	GND	Ground	Ground.
M15	GND	Ground	Ground.
M16	GND	Ground	Ground.
N1	LLC	Digital video output	Line-Locked Output Clock for the Pixel Data.
N2	P24	Digital video output	Video Pixel Output Port.
N3	INT2	Miscellaneous digital	Interrupt. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control.
N4	TEST4	Test	Connect this pin to ground.
N5	$\overline{\text{RESET}}$	Miscellaneous digital	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7842 circuitry.
N6	TEST6	Test	Float this pin.
N7	SDRAM_A8	SDRAM interface	Address Output. Interface to external RAM address lines.
N8	SDRAM_A4	SDRAM interface	Address Output. Interface to external RAM address lines.
N9	SDRAM_A0	SDRAM interface	Address Output. Interface to external RAM address lines.
N10	$\overline{\text{SDRAM_CS}}$	SDRAM interface	Chip Select. SDRAM_CS enables and disables the command decoder on the RAM. One of four command signals to the external SDRAM.
N11	SDRAM_LDQS	SDRAM interface	Lower Data Strobe Pin. Data strobe pins are used for the RAM interface. This is an input when reading data from external memory and an output when writing data to external memory. It is edge aligned with data when reading from external memory and centered with data when writing to external memory. SDRAM_LDQS corresponds to the data on SDRAM_DQ7 to SDRAM_DQ0.
N12	SDRAM_DQ4	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
N13	SDRAM_DQ15	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
N14	SDRAM_DQ11	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
N15	SDRAM_CK	SDRAM interface	Differential Clock Output. All address and control output signals to the RAM should be sampled on the positive edge of SDRAM_CK and on the negative edge of $\overline{\text{SDRAM_CK}}$.
N16	SDRAM_CKE	SDRAM interface	Clock Enable. This pin acts as an enable to the clock signals of the external RAM.
P1	P25	Digital video output	Video Pixel Output Port.
P2	P26	Digital video output	Video Pixel Output Port.
P3	TEST5	Test	Connect this pin to ground.
P4	AVLINK	Digital input/output	Digital SCART Control Channel.
P5	TEST7	Test	Float this pin.
P6	SDRAM_A11	SDRAM interface	Address Output. Interface to external RAM address lines.
P7	SDRAM_A7	SDRAM interface	Address Output. Interface to external RAM address lines.
P8	SDRAM_A3	SDRAM interface	Address Output. Interface to external RAM address lines.
P9	SDRAM_A10	SDRAM interface	Address Output. Interface to external RAM address lines.
P10	$\overline{\text{SDRAM_RAS}}$	SDRAM interface	Row Address Select Command Signal. One of four command signals to the external SDRAM.
P11	SDRAM_DQ7	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
P12	SDRAM_DQ3	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
P13	SDRAM_VREF	SDRAM interface	1.25 V Reference for DDR SDRAM Interface or 1.65 V for SDR SDRAM Interface.
P14	SDRAM_DQ12	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
P15	SDRAM_UDQS	SDRAM interface	Upper Data Strobe Pin. Data strobe pins are used for the RAM interface. This is an input when reading data from external memory and an output when writing data to external memory. It is edge aligned with data when reading from external memory and centered with data when writing to external memory. SDRAM_UDQS corresponds to the data on SDRAM_DQ15 to SDRAM_DQ8.
P16	$\overline{\text{SDRAM_CK}}$	SDRAM interface	Differential Clock Output. All address and control output signals to the RAM should be sampled on the positive edge of SDRAM_CK and on the negative edge of $\overline{\text{SDRAM_CK}}$.
R1	P27	Digital video output	Video Pixel Output Port.
R2	P28	Digital video output	Video Pixel Output Port.
R3	P30	Digital video output	Video Pixel Output Port.
R4	P32	Digital video output	Video Pixel Output Port.

Pin No.	Mnemonic	Type	Description
R5	P34	Digital video output	Video Pixel Output Port.
R6	SDRAM_A9	SDRAM interface	Address Output. Interface to external RAM address lines.
R7	SDRAM_A6	SDRAM interface	Address Output. Interface to external RAM address lines.
R8	SDRAM_A2	SDRAM interface	Address Output. Interface to external RAM address lines.
R9	SDRAM_BA1	SDRAM interface	Bank Address Output. Interface to external RAM bank address lines.
R10	$\overline{\text{SDRAM_CAS}}$	SDRAM interface	Column Address Select Command Signal. One of four command signals to the external SDRAM.
R11	SDRAM_DQ6	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
R12	SDRAM_DQ2	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
R13	SDRAM_DQ0	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
R14	SDRAM_DQ13	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
R15	SDRAM_DQ9	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
R16	SDRAM_DQ8	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
T1	GND	Ground	Ground.
T2	P29	Digital video output	Video Pixel Output Port.
T3	P31	Digital video output	Video Pixel Output Port.
T4	P33	Digital video output	Video Pixel Output Port.
T5	P35	Digital video output	Video Pixel Output Port.
T6	GND	Ground	Ground.
T7	SDRAM_A5	SDRAM interface	Address Output. Interface to external RAM address lines.
T8	SDRAM_A1	SDRAM interface	Address Output. Interface to external RAM address lines.
T9	SDRAM_BA0	SDRAM interface	Bank Address Output. Interface to external RAM bank address lines.
T10	$\overline{\text{SDRAM_WE}}$	SDRAM interface	Write Enable Output Command Signal. One of four command signals to the external SDRAM.
T11	SDRAM_DQ5	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
T12	GND	Ground	Ground.
T13	SDRAM_DQ1	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
T14	SDRAM_DQ14	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
T15	SDRAM_DQ10	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
T16	GND	Ground	Ground.

FUNCTIONAL OVERVIEW

HDMI RECEIVER

The ADV7842 front end incorporates a 2:1 multiplexed HDMI 1.4 receiver with Xpressview fast switching technology and support for HDMI 1.4 features such as 3D TV. Building on the feature set of Analog Device existing HDMI devices, the ADV7842 also offers support for all HD TV formats up to 12-bit, 1080p Deep Color and all display resolutions up to UXGA (1600 × 1200 at 60 Hz). Xpressview fast switching technology, using Analog Devices hardware-based HDCP engine that minimizes software overhead, allows switching between the two input ports in less than 1 second.

With the inclusion of HDCP 1.4, the ADV7842 can receive encrypted video content. The HDMI interface of the ADV7842 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewal of that authentication during transmission, as specified by the HDCP 1.4 protocol. Repeater support is also offered by the ADV7842.

The HDMI receiver incorporates active equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. It is capable of equalizing for cable lengths up to 30 meters to achieve robust receiver performance at even the highest HDMI data rates.

The HDMI receiver offers advanced audio functionality. It supports multichannel I^2S audio for up to eight channels. It also supports a 6-DSD channel interface with each channel carrying an over-sampled 1-bit representation of the audio signal as delivered on SACD. The ADV7842 can also receive HBR audio packet streams and outputs them through the HBR interface in an SPDIF format conforming to the IEC60958 standard.

The receiver contains an audio mute controller that can detect a variety of conditions that may result in audible extraneous noise in the audio output. On detection of these conditions, the audio signal can be ramped to mute to prevent audio clicks or pops.

HDMI receiver features include:

- 2:1 multiplexed HDMI receiver
- HDMI 1.4, 3D format support, DVI 1.0
- 225 MHz HDMI receiver
- Integrated equalizer
- High-bandwidth Digital Content Protection (HDCP 1.4) also on background ports
- Internal HDCP keys
- 36-/30-bit Deep Color support
- PCM, HBR, DSD audio packet support
- Repeater support
- Internal E-EDID RAM
- Hot plug assert output pin for each HDMI port
- CEC controller

ANALOG FRONT END

The ADV7842 analog front end comprises four 170 MHz, 12-bit ADCs that digitize the analog video signal before applying it to the standard definition processor (SDP) or component processor (CP). The analog front end uses differential channels to each ADC to ensure high performance in a mixed-signal application. The front end also includes a 12-channel input mux that enables multiple video signals to be applied to the ADV7842 without the requirement of an external mux.

Current and voltage clamp control loops ensure that any DC offsets are removed from the video signal. The clamps are positioned in front of each ADC to ensure that the video signal remains within the range of the converter.

The ADCs are configured to run up to 8× oversampling mode when decoding composite or S-Video inputs. For component 525i, 625i, 525p, and 625p sources, 4× oversampling is performed. All other video standards are 1× oversampled. Oversampling the video signals reduces the cost and complexity of external antialiasing filters with the benefit of an increased signal-to-noise ratio (SNR).

Optional internal antialiasing filters with programmable bandwidth are positioned in front of each ADC. These filters can be used to band limit video signals, removing spurious, out-of-band noise.

The ADV7842 can support the simultaneous processing of CVBS and RGB standard definition signals to enable SCART compatibility and overlay functionality. A combination of CVBS and RGB inputs can be mixed with the output under the control of I^2C registers.

Analog front-end features include:

- Four 170 MHz, NSV, 12-bit ADCs that enable true 12-bit video decoding
- 12-channel analog input mux that enables multiple source connections without the requirement of an external mux
- Four current and voltage clamp control loops that ensure any dc offsets are removed from the video signal
- SCART functionality and SD RGB overlay on CVBS controlled by fast blank input
- SCART source switching detection through TRI1-TRI8 input
- Four programmable antialiasing filters

STANDARD DEFINITION PROCESSOR

The SDP is capable of decoding a large selection of baseband video signals in composite and S-Video formats. The video standards supported by the SDP include PAL, PAL 60, PAL M, PAL N, PAL NC, NTSC M/J, NTSC 4.43, and SECAM. The ADV7842 can automatically detect the video standard and process it accordingly.

The SDP has a 3D temporal comb filter and a five-line adaptive 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality with no user intervention required. The SDP has an IF filter block that compensates for attenuation in the high frequency chroma spectrum due to a tuner SAW filter. The SDP has specific luminance and chrominance parameter controls for brightness, contrast, saturation, and hue.

The ADV7842 implements a patented Adaptive Digital Line Length Tracking (ADLLT™) algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7842 to track and decode poor quality video sources (such as VCRs) and noisy sources (such as tuner outputs, VCR players, and camcorders). Frame TBC ensures stable clock synchronization between the decoder and the downstream devices.

The SDP also contains both a luma transient improvement (LTI) block and a chroma transient improvement (CTI) block. These increase the edge rate on the luma and chroma transitions, resulting in a sharper video image. The SDP has a Macrovision® detection circuit that allows Type I, Type II, and Type III Macrovision protection levels. The decoder is also fully robust to all Macrovision signal inputs.

SDP features include:

- Advanced adaptive 3D comb (using either external DDR or SDR SDRAM memory)
- Adaptive 2D five-line comb filters for NTSC and PAL that give superior chrominance and luminance separation for composite video
- Full automatic detection and autoswitching of all worldwide standards (PAL, NTSC, and SECAM)
- Automatic gain control with white peak mode that ensures the video is always processed without loss of the video processing range
- Proprietary architecture for locking to weak, noisy, and unstable sources from VCRs and tuners
- IF filter block that compensates for high frequency luma attenuation due to tuner SAW filter
- LTI and CTI
- Vertical and horizontal programmable luma peaking filters
- 8× oversampling (108 MHz) for CVBS, and S-Video modes
- Line-locked clock (LLC) output
- Free run output mode that provides stable timing when no video input is present or video lock is lost
- Internal color bar test pattern
- Advanced TBC with frame synchronization, which ensures nominal clock and data for nonstandard input
- Interlace-to-progressive conversion for 525i and 625i formats, enabling direct drive of HDMI Tx devices
- Color controls that include hue, brightness, saturation, and contrast

COMPONENT PROCESSOR

The CP section of the ADV7842 is capable of decoding and digitizing a wide range of component video formats in any color space. Component video standards supported by the CP are 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, 1250i, VGA up to UXGA at 60 Hz, and other standards.

The any-to-any, 3 × 3 CSC matrix is placed between the analog front end and the CP section. This enables YPbPr to RGB and RGB to YCbCr conversions. Many other standards of color space can be implemented using the color space converter.

The CP section contains circuitry to enable the detection of Macrovision encoded YPbPr signals for 525i, 625i, 525p, and 625p. It is designed to be fully robust when decoding these types of signals. VBI extraction of CGMS data is performed by the CP section of the ADV7842 for interlaced, progressive, and high definition scanning rates. The data extracted can be read back over the I^2C interface.

CP features include:

- 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, and many other HDTV formats are supported
- Supports 720p 24 Hz/25 Hz formats
- Manual adjustments, including gain (contrast), offset (brightness), hue, and saturation
- Support for analog component YPbPr and RGB video formats with embedded synchronization, composite synchronization or separate HS and VS
- Any-to-any, 3 × 3 CSC matrix that supports YCbCr-to-RGB and RGB-to-YCbCr, fully programmable or preprogrammable configurations
- Synchronization source polarity detector (SSPD) that determines the source and polarity of the synchronization signals that accompany the input video
- Macrovision copy protection detection on component formats (525i, 625i, 525p, and 625p)
- Free-run output mode that provides stable timing when no video input is present or video lock is lost
- Arbitrary pixel sampling support for nonstandard video sources
- 170 MHz conversion rate, which supports RGB input resolutions up to 1600 × 1200 at 60 Hz
- Standard identification enabled by STDI block
- RGB that can be color space converted to YCbCr and decimated to a 4:2:2 format for video-centric back-end IC interfacing

- Data enable (DE) output signal supplied for direct connection to HDMI/DVI Tx IC
- 32-phase DLL that allows optimum pixel clock sampling
- Automatic detection of synchronization source and polarity by SSPD block
- Contrast, brightness, hue, and saturation controls
- Automatic or manual clamp-and-gain controls for graphics modes

OTHER FEATURES

The ADV7842 has HS, VS, FIELD, and DE output signals with programmable position, polarity, and width, and two I^2C host port interfaces (control and VBI). The ADV7842 has two programmable interrupt request output pins, INT1 and INT2. It also features a number of low power modes and a full power-down mode. The ADV7842 is provided in a 17 mm × 17 mm, RoHS-compliant BGA package, and is specified over the −10°C to +70°C temperature range.

For more detailed product information about the ADV7842, contact your local Analog Devices sales office.

EXTERNAL MEMORY REQUIREMENTS

The ADV7842 uses external SDRAM for 3D comb and frame synchronizer. The ADV7842 supports either SDR or DDR SD RAM.

SINGLE DATA RATE (SDR)

The ADV7842 can use SDR external memory to provide 3D comb or frame synchronizer operation nonconcurrently.

There is a 64 Mb SDR SDRAM minimum memory requirement. The required memory architecture is four banks of 1 Mb × 16 (4M16) with a speed grade of 133 MHz at CAS latency (CL) 3. Using 22 Ω series termination resistors is recommended for this configuration.

Recommended SDR memory that is compatible with the ADV7842 includes Winbond W9864G6PH-7.

DOUBLE DATA RATE (DDR)

The ADV7842 can use DDR external memory to simultaneously provide 3D comb and frame synchronizer operation.

There is a 128 Mb DDR SDRAM minimum memory requirement. The required memory architecture is four banks of 2 Mb × 16 (8M16) with a speed grade of 133 MHz at CL 2.5. Using 22 Ω series termination resistors is recommended for this configuration

Recommended DDR memory that is compatible with the ADV7842 includes the K4H561638J-LCB3 from Samsung, the MT46V16M16P-6T from Micron Technology, Inc. and the H5DU1262GTR-E3C from Hynix Inc.

PIXEL INPUT/OUTPUT FORMATTING

The output section of the ADV7842 is highly flexible. The pixel output bus can support up to 36-bit 4:4:4. The pixel data supports both single and double data rates modes. In SDR mode, a 16-/20-/24-bit 4:2:2 or 24-/30-/36-bit 4:4:4 output is possible. In DDR mode, the pixel output port can be configured in 8-/10-/12-bit 4:2:2 modes or 24-/30-/36-bit 4:4:4 modes. Bus rotation and bus inversion are also supported. All output modes are controlled via I^2C controls.

PIXEL DATA OUTPUT MODES FEATURES

The output pixel port features include the following:

- 8-/10-/12-bit ITU-R BT.656 4:2:2 with embedded time codes and/or HS, VS, and FIELD output signals
- SDR 16-/20-/24-/30-/36 bit with embedded time codes and/or HS/CS and VS/FIELD pin timing
- DDR 8-/10-/12-bit 4:2:2 with embedded time codes and/or HS, VS, and FIELD output signals
- DDR 24-/30-/36 bit 4:4:4 with embedded time codes and/or HS, VS, and FIELD output signals

Note that DDR modes are supported up to 54 MHz by characterization.

REGISTER MAP ARCHITECTURE

The registers of the ADV7842 are controlled via a 2-wire serial (I^2C-compatible) interface. The ADV7842 has 12 maps. The IO map has a static I^2C address. All other map addresses must be programmed; this ensures no addressing clashes on the system. Figure 9 shows the register map architecture.

Table 8.

Register Map Name	Default Address	Programmable Address	Location at Which Address Can Be Programmed
IO Map	0x40	Not programmable	Not applicable
CP Map	0x00	Programmable	IO map, Register 0xFD
SDP Map	0x00	Programmable	IO map, Register 0xF1
SDP_IO Map	0x00	Programmable	IO map, Register 0xF2
VDP Map	0x00	Programmable	IO map, Register 0xFE
AVLINK Map	0x00	Programmable	IO map, Register 0xF3
CEC Map	0x00	Programmable	IO map, Register 0xF4
HDMI Map	0x00	Programmable	IO map, Register 0xFB
EDID Map	0x00	Programmable	IO map, Register 0xFA
Repeater Map	0x00	Programmable	IO map, Register 0xF9
AFE, DPLL Map	0x00	Programmable	IO map, Register 0xF8
InfoFrame Map	0x00	Programmable	IO map, Register 0xF5

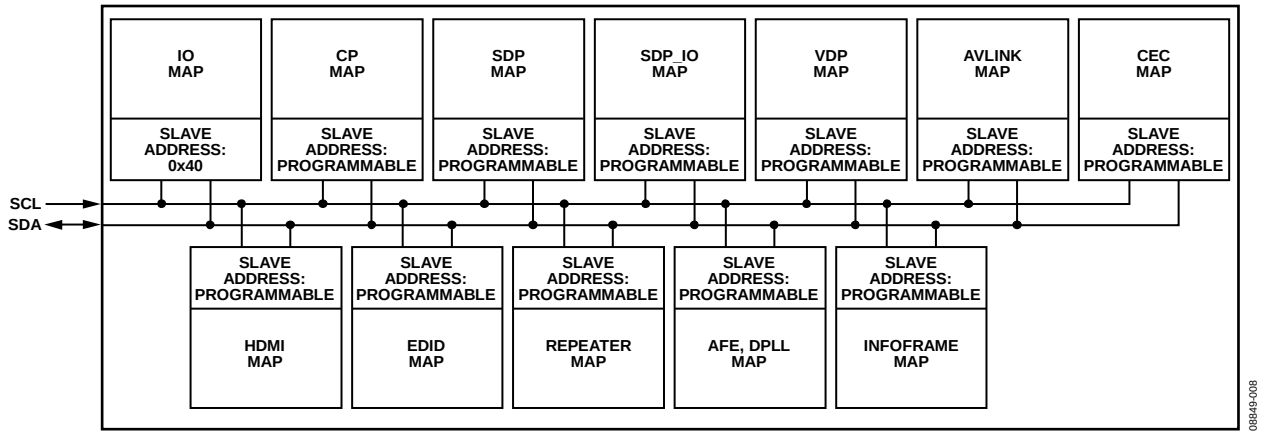


Figure 9. Register Map Architecture

OUTLINE DIMENSIONS

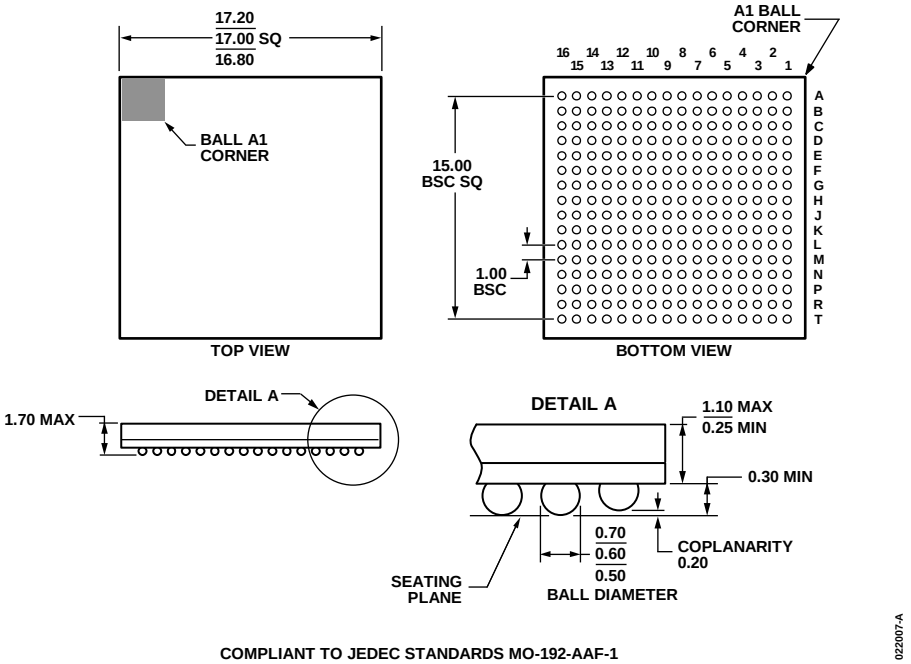


Figure 10. 256-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-256-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Notes	Temperature Range	Package Description	Package Option
ADV7842KBCZ-5	2, 3	−10°C to +70°C	256-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-256-3
ADV7842KBCZ-5P	2, 4, 5	−10°C to +70°C	256-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-256-3
EVAL-ADV7842EB1Z	3, 6, 7		Front-End Evaluation Board	
EVAL-ADV7842EB2Z	5, 6, 8		Front-End Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] Speed grade: 5 = 170 MHz.
[3] This part is programmed with internal HDCP keys. Customers must have HDCP adopter status (consult Digital Content Protection, LLC, for licensing requirements) to purchase any components with internal HDCP keys.
[4] HDCP functionality: P = no HDCP functionality (professional version).
[5] Professional version for non-HDCP encrypted applications. Purchaser is not required to be an HDCP adopter.
[6] An ATV motherboard is also required to process the ADV7842 digital outputs and achieve video output. An ATV video output board is optional to evaluate performance through an HDMI transmitter and video encoder.
[7] Front-end board for the ATV video evaluation platform, fitted with ADV7842KBCZ-5 decoder.
[8] Front-end board for the ATV video evaluation platform, fitted with ADV7842KBCZ-5P decoder.

NOTES

NOTES

I²C refers to a communications protocol originally developed by Phillips Semiconductors (now NXP Semiconductors).

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