

**Stereo 3.1W Class D Amplifier****MAX98303****General Description**

The MAX98303 stereo 3.1W Class D amplifier provides Class AB audio performance with Class D efficiency. This device offers five selectable gain settings (6dB, 9dB, 12dB, 15dB, and 18dB) set by a single gain-select input (GAIN).

Active emissions limiting, edge-rate, and overshoot control circuitry greatly reduces EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class D devices. These features reduce application component count.

The IC's 2.0mA at 3.7V, 2.7mA at 5V, quiescent current extends battery life in portable applications.

The IC is available in a 16-bump WLP (1.68mm x 1.68mm x 0.64mm) package specified over the extended -40°C to +85°C temperature range.

**Applications**

Notebook and Netbook  
Computers  
Tablets  
Cellular Phones

MP3 Players  
Portable Audio Players  
VoIP Phones

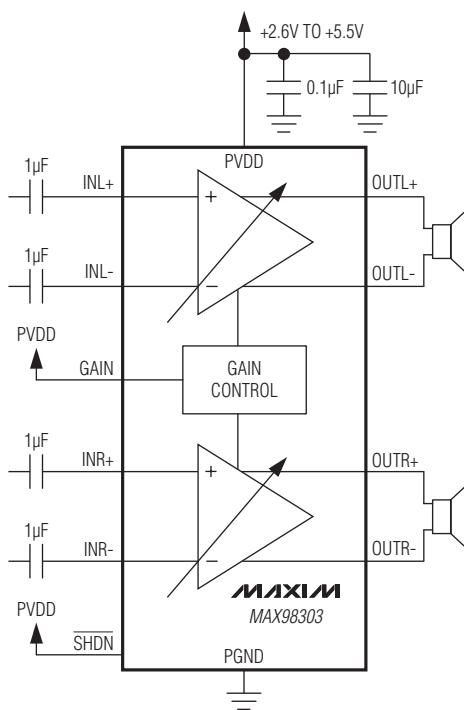
**Features**

- ◆ Low Quiescent Current: 2.0mA at 3.7V, 2.7mA at 5V
- ◆ Spread Spectrum and Active Emissions Limiting
- ◆ Five Pin-Selectable Gains
- ◆ Click-and-Pop Suppression
- ◆ Thermal and Overcurrent Protection
- ◆ Low-Current Shutdown Mode
- ◆ Space-Saving, 1.68mm x 1.68mm x 0.64mm, 16-Bump WLP (0.4mm Pitch)

**Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX98303EWE+	-40°C to +85°C	16 WLP	AAA

+Denotes a lead(Pb)-free/RoHS-compliant package.

**Typical Application Circuit**

# Stereo 3.1W Class D Amplifier

## ABSOLUTE MAXIMUM RATINGS

PVDD to PGND.....	-0.3V to +6V
OUT <sub>+</sub> , OUT <sub>-</sub> to PGND .....	-0.3V to (V <sub>PVDD</sub> + 0.3V)
All Other Pins to PGND .....	-0.3V to +6V
Continuous Current for PVDD, PGND, OUTL <sub>-,</sub> OUTR <sub>-</sub> .....	±1600mA
Continuous Input Current (all other pins).....	±20mA
Duration of Short Circuit Between OUTL <sub>-,</sub> OUTR <sub>-</sub> to PVDD or PGND .....	Continuous
OUTL <sub>+</sub> to OUTL <sub>-,</sub> OUTR <sub>+</sub> to OUTR <sub>-</sub> .....	Continuous

Continuous Power Dissipation for Multilayer Board (T <sub>A</sub> = +70°C) 16-Bump WLP (derate 17.2mW/°C above +70°C) .....	1.38W
θ <sub>JA</sub> (Note 1).....	58°C/W
θ <sub>JJC</sub> (Note 1) .....	15°C/W
Junction Temperature .....	+150°C
Operating Temperature Range.....	-40°C to +85°C
Storage Temperature Range.....	-65°C to +150°C
Soldering Temperature (reflow) .....	+260°C

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

(V<sub>PVDD</sub> = V<sub>SHDN</sub> = 3.7V, V<sub>PGND</sub> = 0V, A<sub>V</sub> = 12dB (GAIN = PVDD), R<sub>L</sub> = ∞, R<sub>L</sub> connected between OUT<sub>+</sub> to OUT<sub>-</sub>, 20Hz to 22kHz AC measurement bandwidth, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V <sub>PVDD</sub>	Inferred from PSRR test	2.6	5.5		V
Undervoltage Lockout	UVLO			2.3		V
Quiescent Supply Current	I <sub>DD</sub>			2.0	3.1	mA
		V <sub>PVDD</sub> = 5.0V		2.7		
Shutdown Supply Current	I <sub>SHDN</sub>	V <sub>SHDN</sub> = 0V, T <sub>A</sub> = +25°C	≤ 0.1	10		µA
Turn-On Time	t <sub>ON</sub>		3.4	10		ms
Bias Voltage	V <sub>BIAS</sub>			1.3		V
Voltage Gain	A <sub>V</sub>	Connect GAIN to PGND	17.5	18	18.5	dB
		Connect GAIN to PGND through 100kΩ ±5% resistor	14.5	15	15.5	
		Connect GAIN to PVDD	11.5	12	12.5	
		Connect GAIN to PVDD through 100kΩ ±5% resistor	8.5	9	9.5	
		GAIN unconnected	5.5	6	6.5	
Channel-to-Channel Gain Tracking				±0.1		%
Input Resistance	R <sub>IN</sub>	A <sub>V</sub> = 18dB	15	20	29	kΩ
		A <sub>V</sub> = 15dB	15	20	29	
		A <sub>V</sub> = 12dB	15	20	29	
		A <sub>V</sub> = 9dB	20	28	40	
		A <sub>V</sub> = 6dB	30	40	58	
Output Offset Voltage	V <sub>OS</sub>	T <sub>A</sub> = +25°C (Note 4)		±0.3	±3	mV

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{PVDD} = V_{SHDN} = 3.7V$ ,  $V_{PGND} = 0V$ ,  $AV = 12dB$  (GAIN =  $PVDD$ ),  $R_L = \infty$ ,  $R_L$  connected between  $OUT_+$  to  $OUT_-$ , 20Hz to 22kHz AC measurement bandwidth,  $TA = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $TA = +25^\circ C$ .) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Click and Pop	KCP	Peak voltage, A-weighted, 32 samples per second, $R_L = 8\Omega + 68\mu H$ (Notes 4, 5)	Into shutdown	-74		dBV
			Out of shutdown	-59		
Common-Mode Rejection Ratio	CMRR	$f_{IN} = 1kHz$ , input referred	$AV = 18dB$	67		dB
			$AV = 15dB$	72		
			$AV = 12dB$	67		
			$AV = 9dB$	65		
			$AV = 6dB$	62		
Crosstalk		$POUT = 300mW$ , $R_L = 8\Omega + 68\mu H$	$f = 1kHz$	100		dB
			$f = 10kHz$	95		
Power-Supply Rejection Ratio (Note 4)	PSRR	$V_{PVDD} = 2.6V$ to $5.5V$ , $TA = +25^\circ C$	51	78		dB
		$V_{RIPPLE} = 200mV_{P-P}$ , $R_L = 8\Omega + 68\mu H$	$f = 217Hz$	66		
			$f = 1kHz$	66		
			$f = 10kHz$	63		
Output Power	POUT	$THD+N = 10\%$ , $f = 1kHz$ , $R_L = 4\Omega + 33\mu H$	$V_{PVDD} = 5.0V$	3.1		W
			$V_{PVDD} = 4.2V$	2.2		
			$V_{PVDD} = 3.7V$	1.7		
			$V_{PVDD} = 5.0V$	2.5		
		$THD+N = 1\%$ , $f = 1kHz$ , $R_L = 4\Omega + 33\mu H$	$V_{PVDD} = 4.2V$	1.7		
			$V_{PVDD} = 3.7V$	1.3		
			$V_{PVDD} = 5.0V$	1.8		
			$V_{PVDD} = 4.2V$	1.2		
		$THD+N = 10\%$ , $f = 1kHz$ , $R_L = 8\Omega + 68\mu H$	$V_{PVDD} = 3.7V$	1.0		
			$V_{PVDD} = 5.0V$	1.4		
			$V_{PVDD} = 4.2V$	1.0		
			$V_{PVDD} = 3.7V$	0.7		
Total Harmonic Distortion Plus Noise	THD+N	$f_{IN} = 1kHz$	$R_L = 4\Omega + 33\mu H$ , $POUT = 1W$	0.047		%
			$R_L = 8\Omega + 68\mu H$ , $POUT = 0.5W$	0.04		
Oscillator Frequency	fosc			300		kHz
Spread-Spectrum Bandwidth				$\pm 15$		kHz
Efficiency	$\eta$	$THD+N = 10\%$ , $f = 1kHz$ , $R_L = 8\Omega + 68\mu H$		93		%
Output Noise	$V_N$	$AV = 6dB$ , A weighted (Note 4)		37		$\mu V_{RMS}$
Signal-to-Noise Ratio	SNR	$POUT = 3.1W$ , $V_{PVDD} = 5.0V$ , $AV = 6dB$		99.6		dB

# Stereo 3.1W Class D Amplifier

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{PVDD} = V_{SHDN} = 3.7V$ ,  $V_{PGND} = 0V$ ,  $AV = 12dB$  ( $GAIN = PVDD$ ),  $R_L = \infty$ ,  $R_L$  connected between  $OUT_+$  to  $OUT_-$ , 20Hz to 22kHz AC measurement bandwidth,  $TA = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $TA = +25^\circ C$ .) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Limit	$I_{LIM}$			2		A
Thermal Shutdown Level				145		°C
Thermal Shutdown Hysteresis				15		°C
<b>DIGITAL INPUT (SHDN)</b>						
Input Voltage High	$V_{IH}$	$V_{PVDD} = 2.5V$ to $5.5V$		1.4		V
Input Voltage Low	$V_{IL}$	$V_{PVDD} = 2.5V$ to $5.5V$			0.4	V
Input Leakage Current		$TA = +25^\circ C$			$\pm 1$	$\mu A$

**Note 2:** This device is 100% production tested at  $TA = +25^\circ C$ . All temperature limits are guaranteed by design.

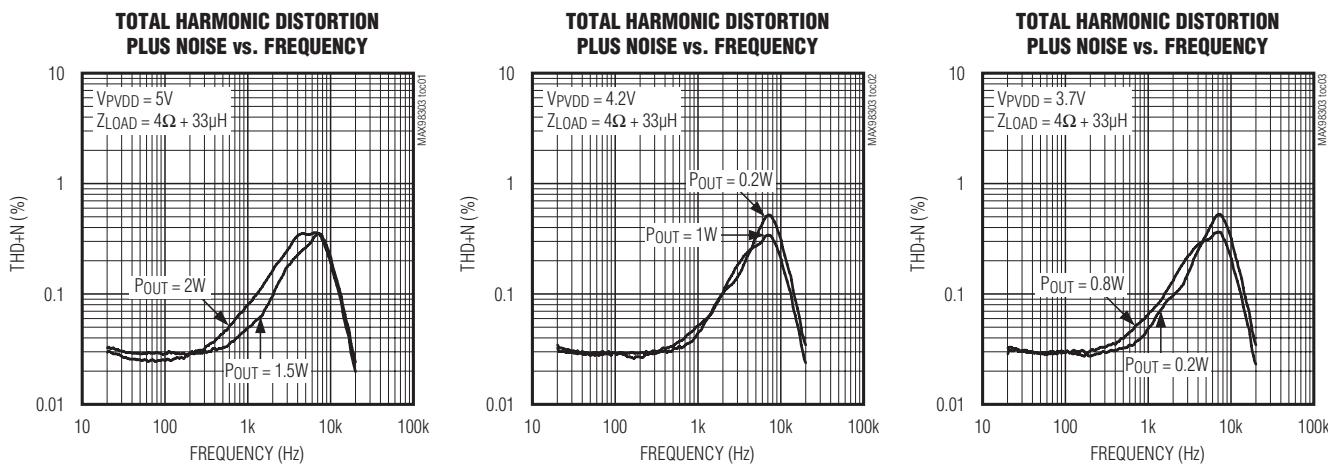
**Note 3:** Testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For  $R_L = 4\Omega$ ,  $L = 33\mu H$ . For  $R_L = 8\Omega$ ,  $L = 68\mu H$ .

**Note 4:** Amplifier inputs AC-coupled to ground.

**Note 5:** Mode transitions controlled by SHDN.

## Typical Operating Characteristics

( $V_{PVDD} = V_{SHDN} = 5.0V$ ,  $V_{PGND} = 0V$ ,  $AV = 12dB$ ,  $R_L = \infty$ ,  $R_L$  connected between  $OUT_+$  to  $OUT_-$ , 20Hz to 22kHz AC measurement bandwidth,  $TA = +25^\circ C$ , unless otherwise noted.)

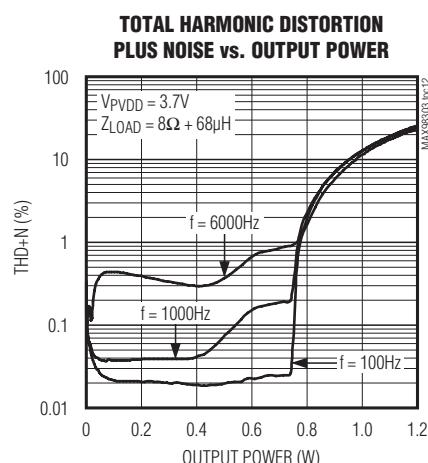
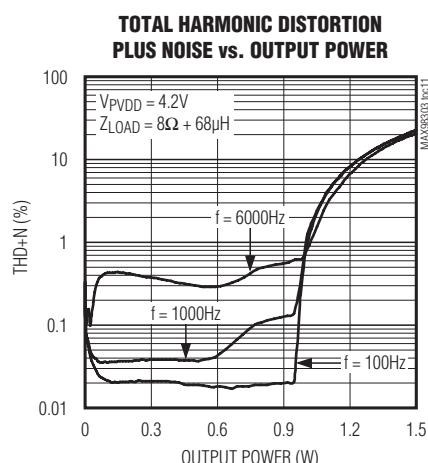
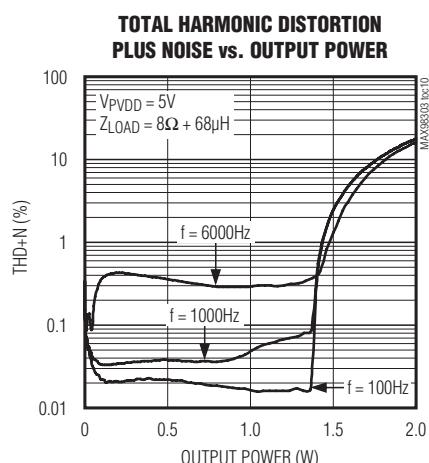
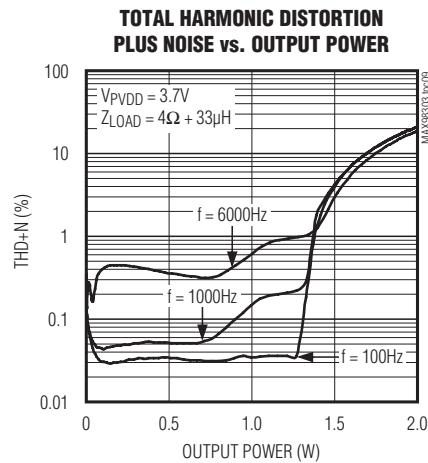
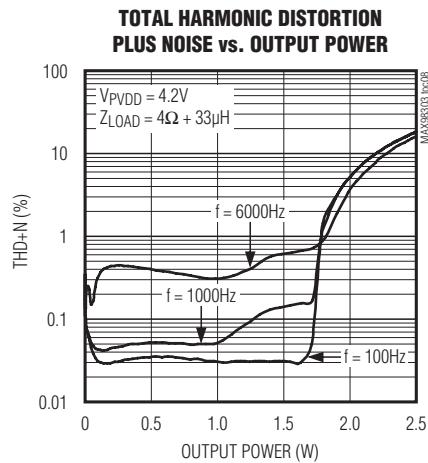
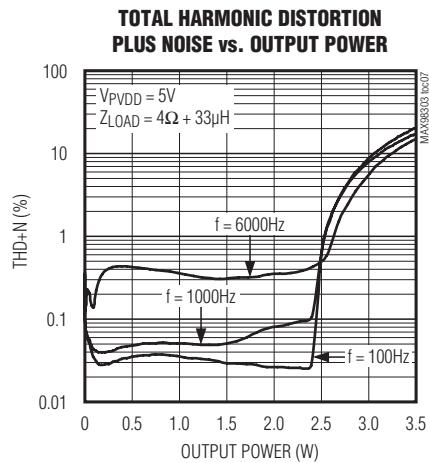
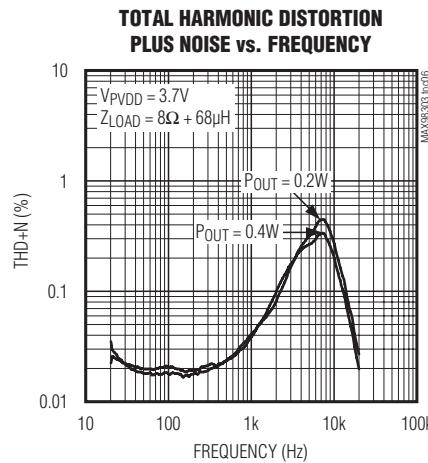
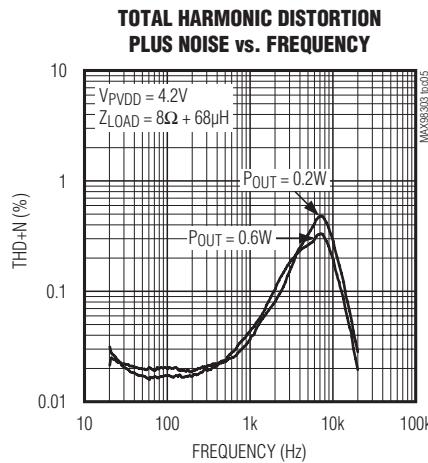
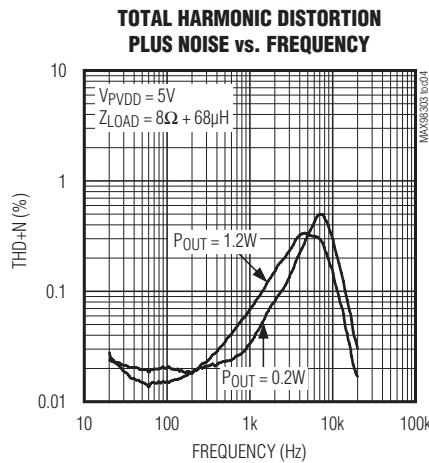


# Stereo 3.1W Class D Amplifier

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## Typical Operating Characteristics (continued)

( $V_{PVDD} = V_{SHDN} = 5.0V$ ,  $V_{PGND} = 0V$ ,  $AV = 12dB$ ,  $R_L = \infty$ ,  $R_L$  connected between  $OUT_+$  to  $OUT_-$ , 20Hz to 22kHz AC measurement bandwidth,  $T_A = +25^\circ C$ , unless otherwise noted.)

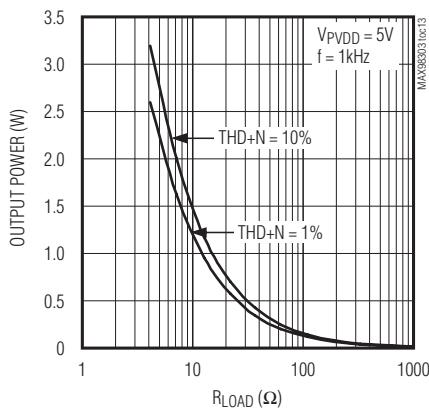


# Stereo 3.1W Class D Amplifier

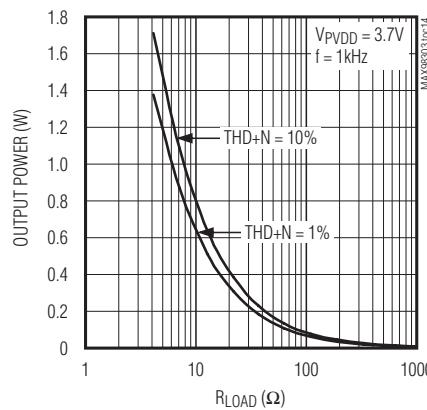
## Typical Operating Characteristics (continued)

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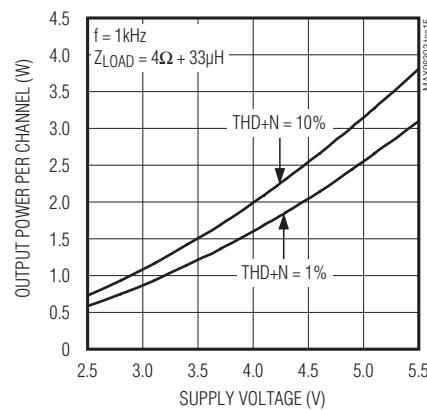
### OUTPUT POWER vs. LOAD RESISTANCE



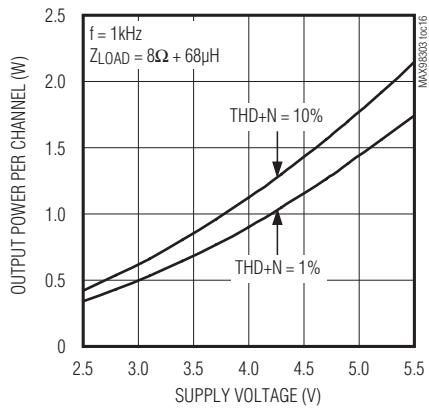
### OUTPUT POWER vs. LOAD RESISTANCE



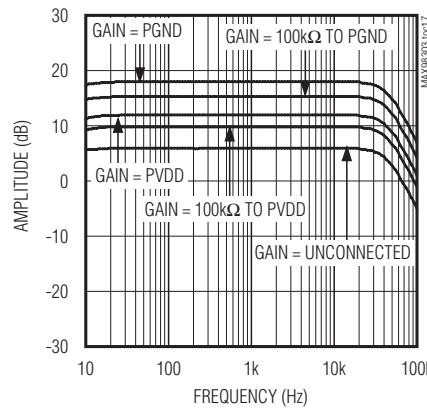
### OUTPUT POWER vs. SUPPLY VOLTAGE



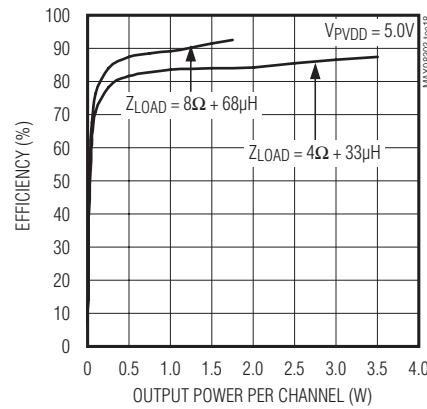
### OUTPUT POWER vs. SUPPLY VOLTAGE



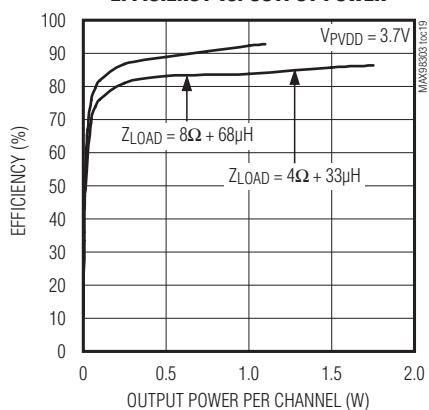
### GAIN vs. FREQUENCY



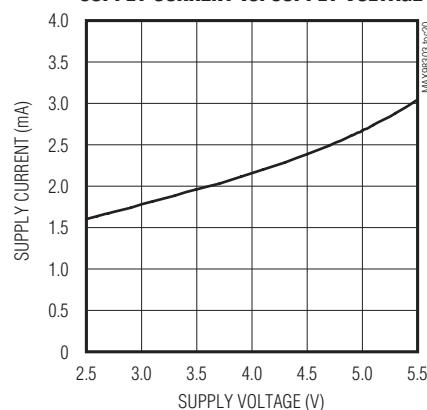
### EFFICIENCY vs. OUTPUT POWER



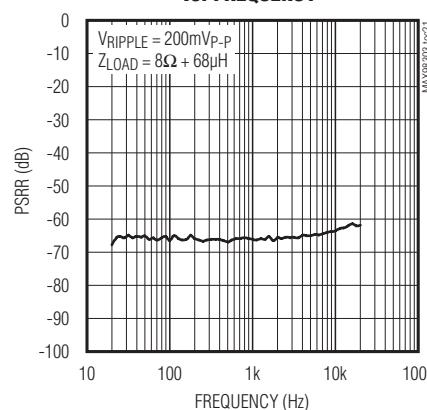
### EFFICIENCY vs. OUTPUT POWER



### SUPPLY CURRENT vs. SUPPLY VOLTAGE



### POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



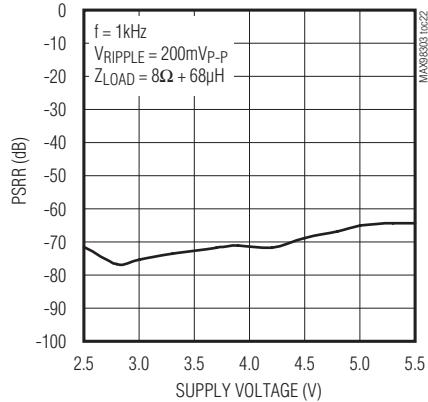
# Stereo 3.1W Class D Amplifier

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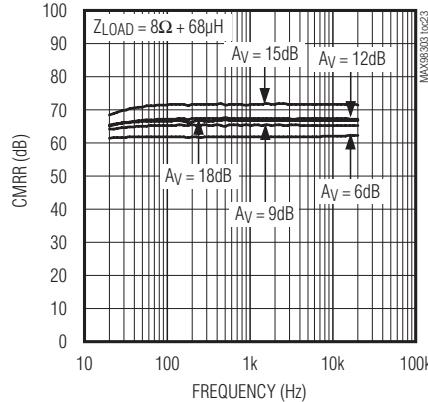
## Typical Operating Characteristics (continued)

( $V_{PVDD} = V_{SHDN} = 5.0V$ ,  $V_{PGND} = 0V$ ,  $A_V = 12dB$ ,  $R_L = \infty$ ,  $R_L$  connected between  $OUT_{+}$  to  $OUT_{-}$ , 20Hz to 22kHz AC measurement bandwidth,  $T_A = +25^\circ C$ , unless otherwise noted.)

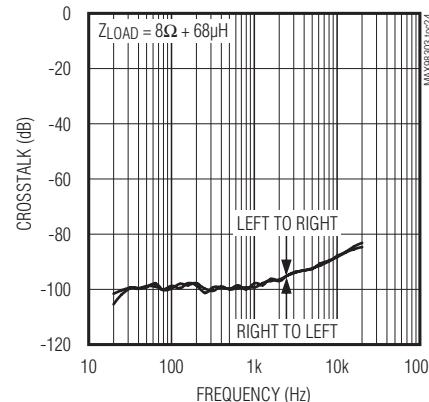
### POWER-SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE



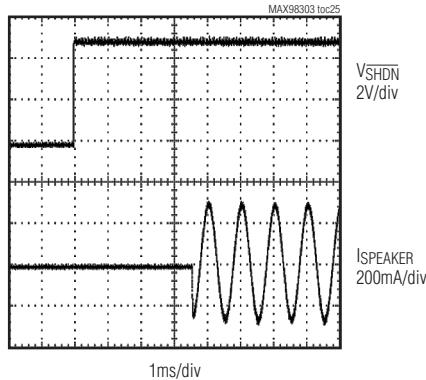
### COMMON-MODE REJECTION RATIO vs. FREQUENCY



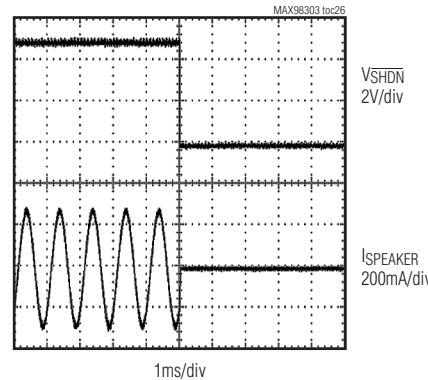
### CROSSTALK vs. FREQUENCY



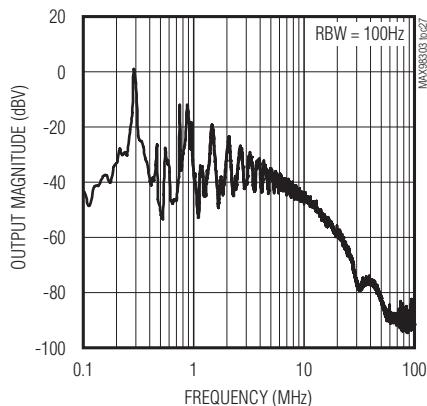
### STARTUP RESPONSE



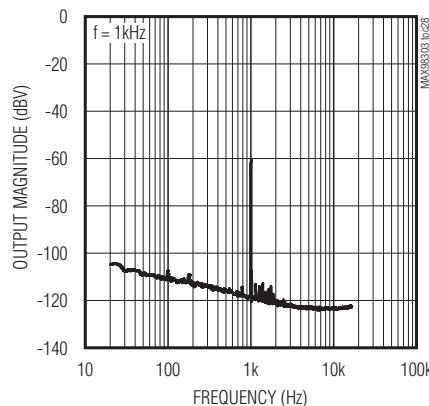
### SHUTDOWN RESPONSE



### WIDEBAND vs. FREQUENCY

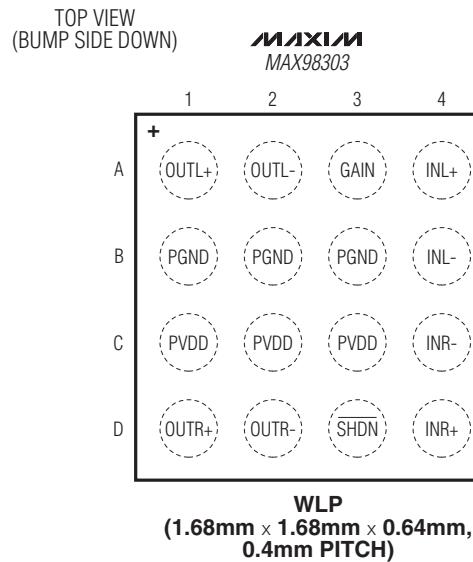


### IN-BAND vs. FREQUENCY



# Stereo 3.1W Class D Amplifier

## Bump Configuration



## Bump Description

BUMP	NAME	FUNCTION
A1	OUTL+	Positive Left Speaker Output
A2	OUTL-	Negative Left Speaker Output
A3	GAIN	Gain Select. See Table 1 for Gain Settings.
A4	INL+	Noninverting Audio Left Input
B1, B2, B3	PGND	Ground
B4	INL-	Inverting Audio Left Input
C1, C2, C3	PVDD	Power Supply. Bypass PVDD to PGND with 0.1µF and 10µF capacitors.
C4	INR-	Inverting Audio Right Input
D1	OUTR+	Positive Right Speaker Output
D2	OUTR-	Negative Right Speaker Output
D3	SHDN	Active-Low Shutdown Input. Drive SHDN low to place the device in shutdown.
D4	INR+	Noninverting Audio Right Input

# Stereo 3.1W Class D Amplifier

MAX98303

## Detailed Description

The MAX98303 features low quiescent current, a low-power shutdown mode, comprehensive click-and-pop suppression, and excellent RF immunity.

The IC offers Class AB audio performance with Class D efficiency in a minimal board-space solution.

The Class D amplifier features spread-spectrum modulation, edge-rate, and overshoot control circuitry that offers significant improvements to switch-mode amplifier radiated emissions.

The amplifier features click-and-pop suppression that reduces audible transients on startup and shutdown. The amplifier includes thermal-overload and short-circuit protection.

## Class D Speaker Amplifier

The filterless Class D amplifier offers much higher efficiency than Class AB amplifiers. The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. Any power loss associated with the Class D output stage is mostly due to the  $I^2R$  loss of the MOSFET on-resistance and quiescent current overhead.

## Ultra-Low-EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. Maxim's active emissions limiting edge-rate control circuitry and spread-spectrum modulation reduce EMI emissions, while maintaining up to 93% efficiency.

Maxim's spread-spectrum modulation mode flattens wideband spectral components, while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The IC's spread-spectrum modulator randomly varies the switching frequency by  $\pm 15\text{kHz}$  around the center frequency (300kHz). Above 10MHz, the wideband spectrum looks like noise for EMI purposes (Figure 1).

## Speaker Current Limit

If the output current of the speaker amplifier exceeds the current limit (2A typ), the IC disables the outputs for approximately 100 $\mu\text{s}$ . At the end of 100 $\mu\text{s}$ , the outputs are reenabled. If the fault condition still exists, the IC continues to disable and reenable the outputs until the fault condition is removed.

## Selectable Gain

The IC offers five programmable gains selected using the GAIN input.

## Table 1. Gain Control Configuration

GAIN PIN	MAXIMUM GAIN (dB)
Connect to PGND	18
Connect to PGND through 100k $\Omega$ $\pm 5\%$ resistor	15
Connect to PVDD	12
Connect to PVDD through 100k $\Omega$ $\pm 5\%$ resistor	9
Unconnected	6

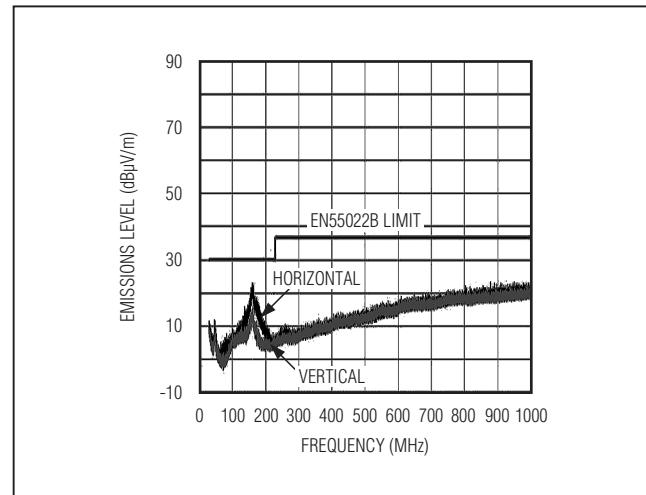


Figure 1. EMI with 30cm of Speaker Cable and No Output Filter

## Shutdown

The IC features a low-power shutdown mode, drawing  $\leq 0.1\mu\text{A}$  (typ) of supply current. Drive SHDN low to place the MAX98303 into shutdown.

## Click-and-Pop Suppression

The IC speaker amplifier features Maxim's comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transient sources internal to the device. When entering shutdown, the differential speaker outputs ramp down to PGND quickly and simultaneously.

# Stereo 3.1W Class D Amplifier

## Applications Information

### Filterless Class D Operation

Traditional Class D amplifiers require an output filter. The filter adds cost and size and decreases THD performance. The IC's filterless modulation scheme does not require an output filter.

Because the switching frequency of the IC is well beyond the bandwidth of most speakers, voice coil movement due to the switching frequency is very small. Use a speaker with a series inductance  $> 10\mu\text{H}$ . Typical  $8\Omega$  speakers exhibit series inductances in the  $20\mu\text{H}$  to  $100\mu\text{H}$  range.

### Component Selection

#### Power-Supply Input (PVDD)

PVDD powers the speaker amplifier. PVDD ranges from 2.6V to 5.5V. Bypass PVDD with  $0.1\mu\text{F}$  and  $10\mu\text{F}$  capacitors to PGND. Apply additional bulk capacitance at the device if long input traces between PVDD and the power source are used.

#### Input Filtering

The input-coupling capacitor ( $C_{IN}$ ), in conjunction with the amplifier's internal input resistance ( $R_{IN}$ ), forms a highpass filter that removes the DC bias from the incoming signal. These capacitors allow the amplifier to bias the signal to an optimum DC level.

Assuming zero source impedance with a gain setting of 12dB, 15dB, or 18dB,  $C_{IN}$  is:

$$C_{IN} = \frac{8}{f_{-3\text{dB}}} [\mu\text{F}]$$

with a gain setting of 9dB,  $C_{IN}$  is:

$$C_{IN} = \frac{5.7}{f_{-3\text{dB}}} [\mu\text{F}]$$

with a gain setting of 6dB,  $C_{IN}$  is:

$$C_{IN} = \frac{4}{f_{-3\text{dB}}} [\mu\text{F}]$$

where  $f_{-3\text{dB}}$  is the -3dB corner frequency. Use capacitors with adequately low-voltage coefficients for best low-frequency THD performance.

### Layout and Grounding

Proper layout and grounding are essential for optimum performance. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal.

Use wide, low-resistance output traces. As the load impedance decreases, the current drawn from the device increases. At higher current, the resistance of the output traces decrease the power delivered to the load. For example, if 2W is delivered from the device output to a  $4\Omega$  load through  $100\text{m}\Omega$  of total speaker trace, 1.904W is delivered to the speaker. If power is delivered through  $10\text{m}\Omega$  of total speaker trace, 1.99W is delivered to the speaker. Wide output, supply, and ground traces also improve the power dissipation of the device.

The IC is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes.

### WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to Application Note 1891: *Wafer level packaging (WLP) and its applications*. Figure 2 shows the dimensions of the WLP balls used on the IC.

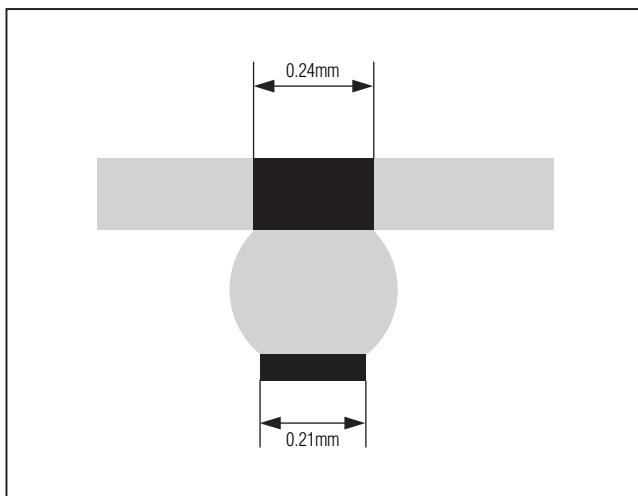
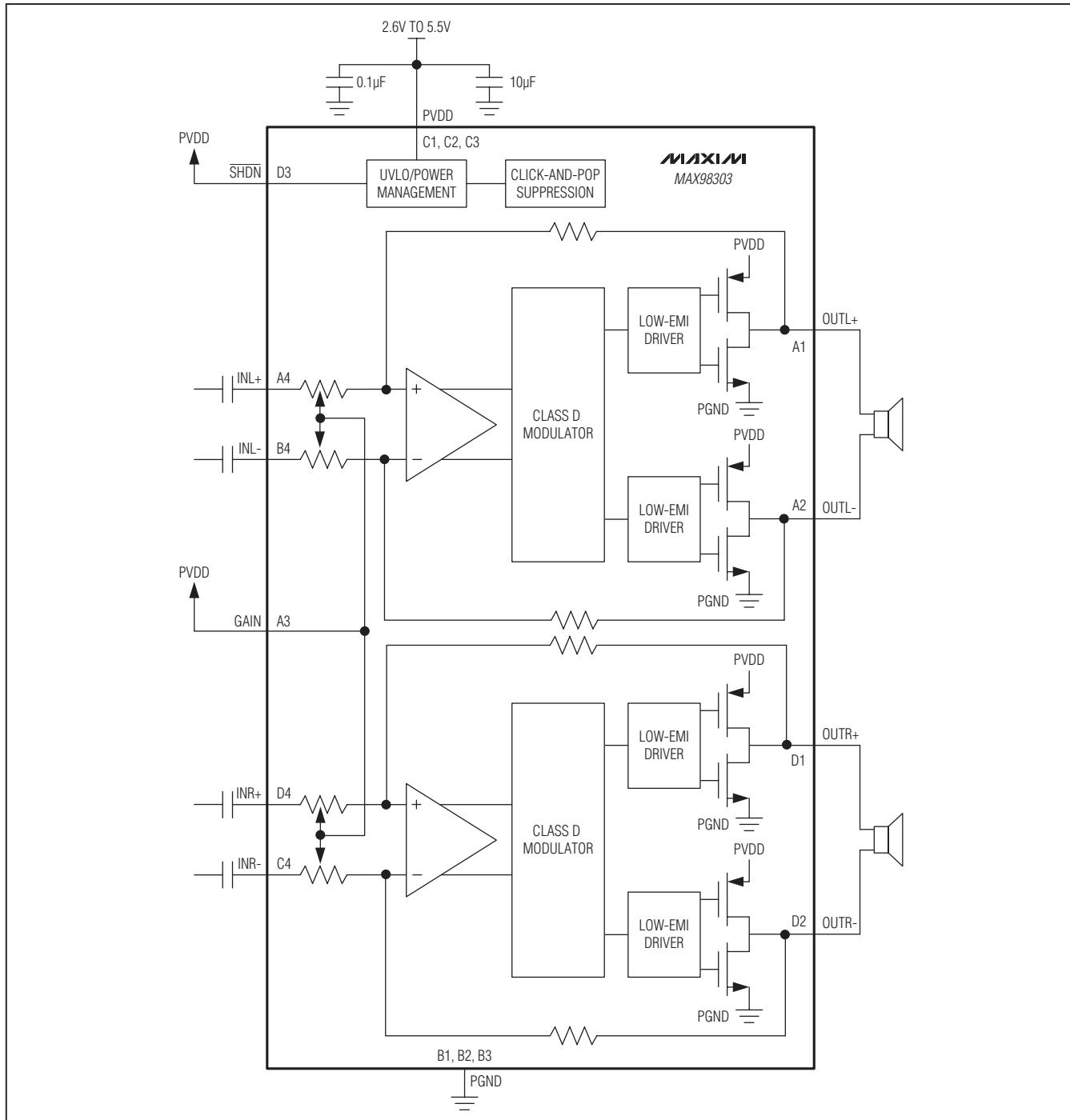


Figure 2. MAX98303 WLP Ball Dimensions

# Stereo 3.1W Class D Amplifier

MAX98303

## Block Diagram



## Chip Information

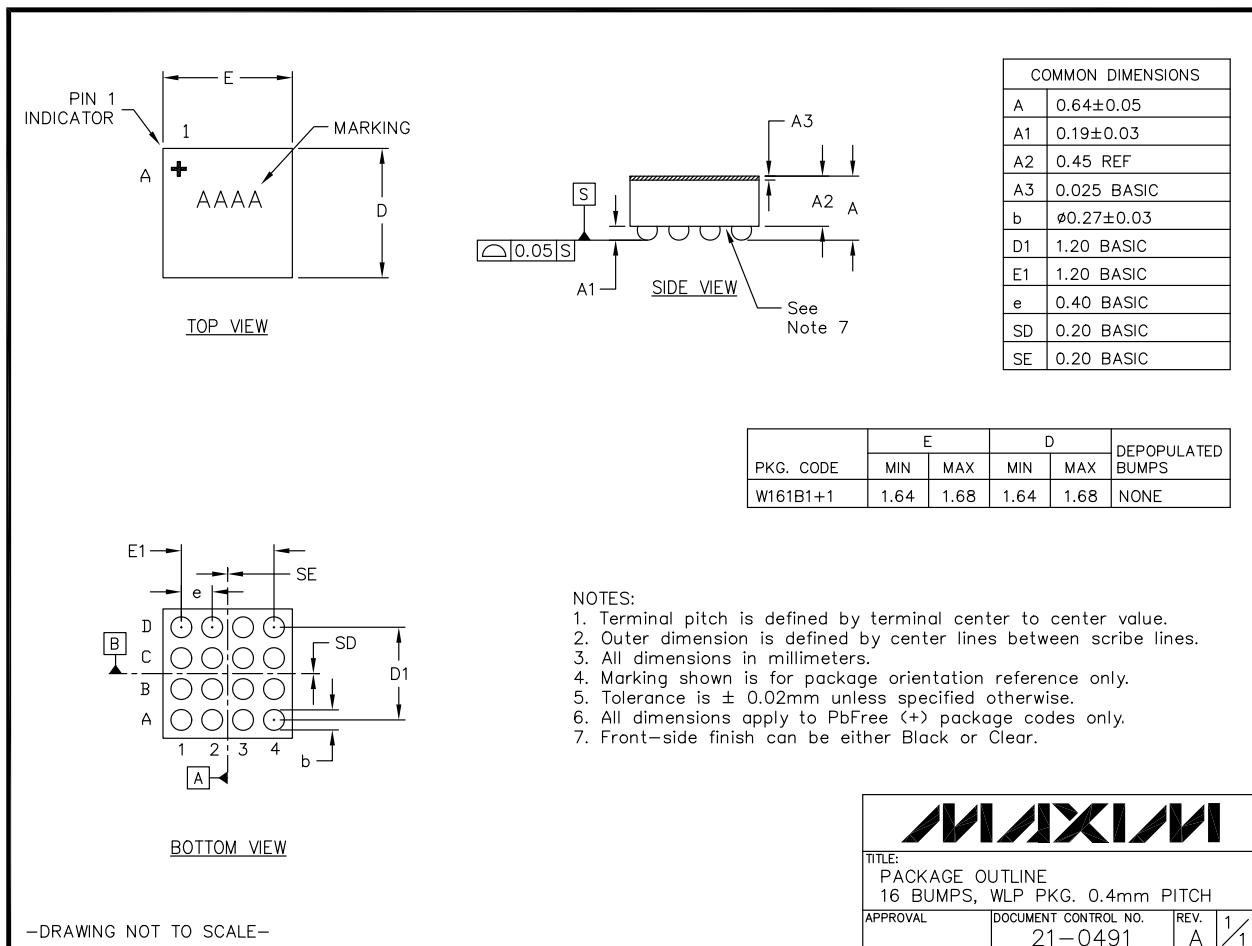
PROCESS: CMOS

# Stereo 3.1W Class D Amplifier

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 WLP	W161B1+1	<a href="#">21-0491</a>	—



# **Stereo 3.1W Class D Amplifier**

## **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—

**MAX98303**

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