M95M02-DR M95M02-DF

Datasheet

2-Mbit serial SPI bus EEPROM

SO8N

(150 mil width)

WLCSP8

(3.556 × 2.011 mm)

Product status link
M95M02-DR
M95M02-DF

Features

Compatible with the serial peripheral interface (SPI) bus

Memory array

- 2 Mbits (256 Kbytes) of EEPROM
- Page size: 256 bytes
- Write protection by block: ¼, ½, or whole memory
- Additional write lockable page (identification page)

Write

- Byte write within 10 ms
- Page write within 10 ms

Clock frequency: 5 MHz

Single supply voltage

- 1.7 to 5.5 V over -20 °C to +85 °C
- 1.8 to 5.5 V over -40 °C to +85 °C

Operating temperature range

- From -40 °C up to +85 °C

Enhanced ESD protection

More than 4 million write cycles

More than 200-year data retention

Packages

- ECOPACK2 (RoHS compliant and halogen-free) packages:
  - SO8N
  - WLCSP8

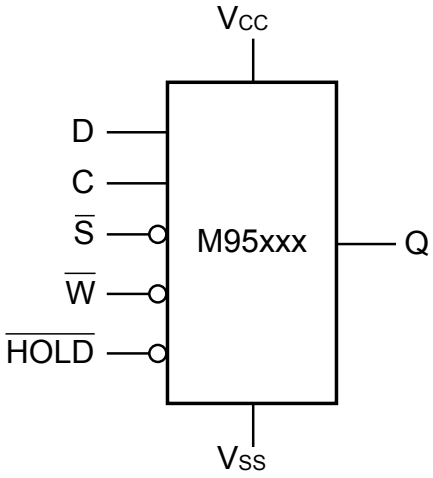
1 Description

The M95M02 devices are electrically erasable programmable memory (EEPROM) organized as 262144 x 8 bits, accessed through the SPI bus.

Over an ambient temperature range of -40 °C / +85 °C the M95M02-DR can operate with a supply voltage from 1.8 to 5.5 V. Over an ambient temperature range of -20 °C / +85 °C the M95M02-DF can operate with a supply voltage from 1.7 to 5.5 V.

The M95M02 devices offer an additional page, named the Identification page (256 bytes). The Identification page can be used to store sensitive application parameters that can be (later) permanently locked in read-only mode.

Figure 1. Logic diagram

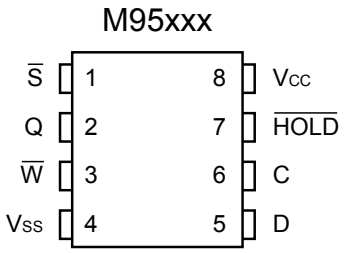


The SPI bus signals are C, D and Q, as shown in Figure 1 and Table 1. The device is selected when chip select ($\overline{S}$) is driven low. Communications with the device can be interrupted when the $\overline{HOLD}$ is driven low.

Table 1. Signal names

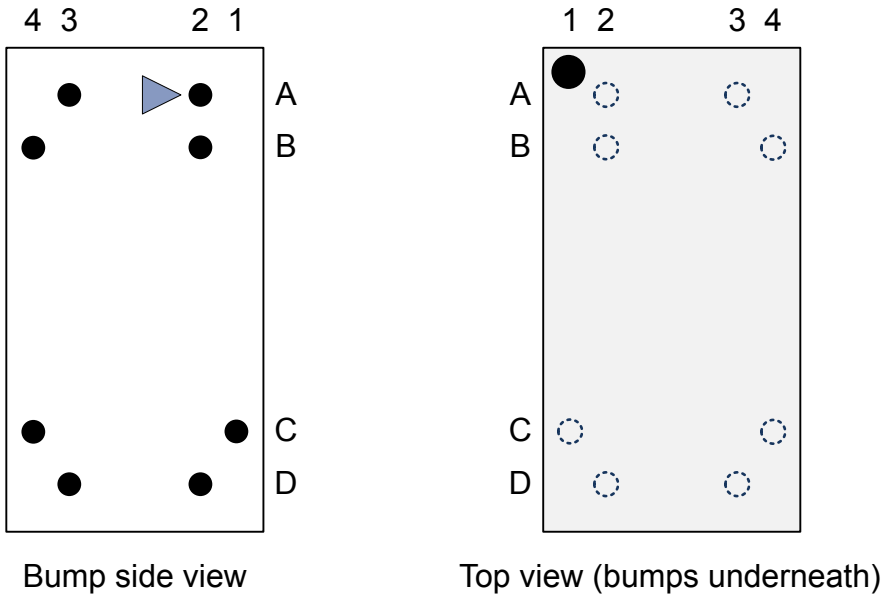
Signal name	Function	Direction
C	Serial clock	Input
D	Serial data input	Input
Q	Serial data output	Output
$\overline{S}$	Chip select	Input
$\overline{W}$	Write protect	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

Figure 2. 8-pin package connections (top view)



1. See Section 10 Package information for package dimensions, and how to identify pin 1.

Figure 3. WLCSP connections



1. See Section 10 Package information for package dimensions, and how to identify pin 1.

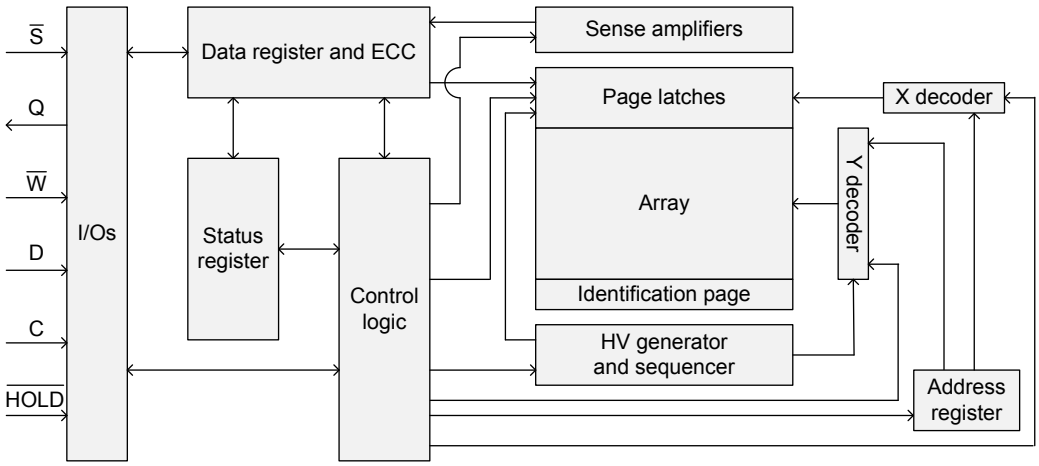
Table 2. Signals vs. bump position

Position	A	B	C	D
1	-	-	C	-
2	V_{CC}	$\overline{HOLD}$	-	D
3	$\overline{S}$	-	-	V_{SS}
4	-	Q	$\overline{W}$	-

2 Block diagram

The block diagram is organized as shown in the following figure.

Figure 4. Block diagram



3 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals must be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in Section 9 DC and AC parameters). These signals are described next.

3.1 Serial data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of serial clock (C).

3.2 Serial data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of serial clock (C).

3.3 Serial clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at serial data input (D) are latched on the rising edge of serial clock (C). Data on serial data output (Q) change from the falling edge of serial clock (C).

3.4 Chip select ($\overline{S}$)

When this input signal is high, the device is deselected and serial data output (Q) is at high impedance. The device is in the standby power mode, unless an internal write cycle is in progress. Driving chip select ($\overline{S}$) low selects the device, placing it in the active power mode.

After power-up, a falling edge on chip select ($\overline{S}$) is required prior to the start of any instruction.

3.5 Hold ($\overline{HOLD}$)

The hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the hold condition, the serial data output (Q) is high impedance, and serial data input (D) and serial clock (C) are "Don't care".

To start the hold condition, the device must be selected, with chip select ($\overline{S}$) driven low.

3.6 Write protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status register).

This pin must be driven either high or low, and must be stable during all Write instructions.

3.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

3.8 V_{SS} ground

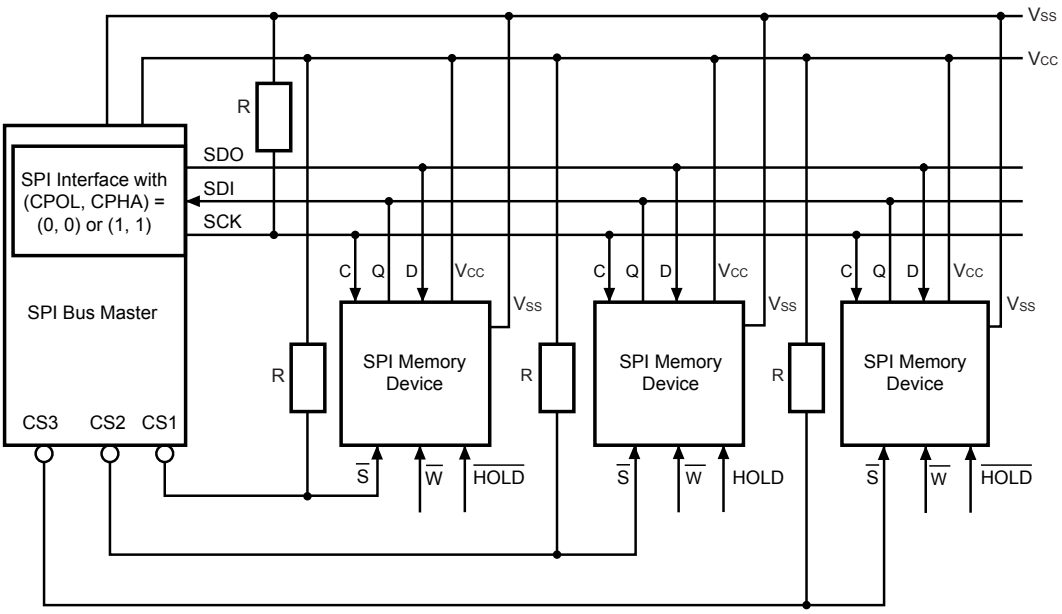
V_{SS} is the reference for all signals, including the V_{CC} supply voltage.

4 Connecting to the SPI bus

All instructions, addresses, and input data bytes are shifted in to the device, the most significant bit first. The serial data input (D) is sampled on the first rising edge of the serial clock (C) after chip select ($\overline{S}$) goes low.

All output data bytes are shifted out of the device, the most significant bit first. The serial data output (Q) is latched on the first falling edge of the serial clock (C) after the instruction (such as the read from memory array and read status register instructions) have been clocked into the device.

Figure 5. Bus master and memory devices on the SPI bus



1. The write protect ($\overline{W}$) and hold ($\overline{HOLD}$) signals should be driven, high, or low as appropriate.

Figure 5 shows an example of three memory devices connected to an SPI bus master. Only one memory device is selected at a given time, so only one memory device drives the serial data output (Q) line at that time. The other memory devices are in high impedance state.

The pull-up resistor R (represented in Figure 5) ensures that a device is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state.

In applications where the bus master may leave all SPI bus lines in high impedance at the same time (for example, if the bus master is reset during the transmission of an instruction), it is recommended to connect the clock line (C) to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the S line is pulled high): this ensures that S and C do not become high at the same time, and so, that the t_{SHCH} requirement is met. The typical value of R is 100 kΩ.

4.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

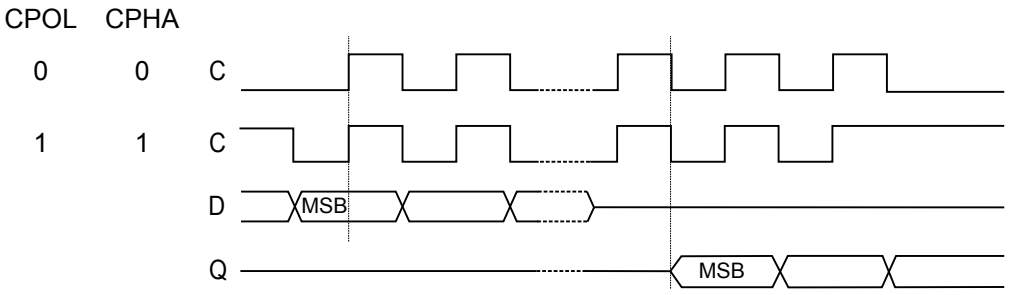
- CPOL = 0, CPHA = 0
- CPOL = 1, CPHA = 1

For these two modes, input data is latched in on the rising edge of serial clock (C), and output data is available from the falling edge of serial clock (C).

The difference between the two modes, as shown in Figure 6, is the clock polarity when the bus master is in stand-by mode and not transferring data:

- C remains at 0 for (CPOL = 0, CPHA = 0)
- C remains at 1 for (CPOL = 1, CPHA = 1)

Figure 6. SPI modes supported



5 Operating features

5.1 Supply voltage (V_{CC})

5.1.1 Operating supply voltage (V_{CC})

Before selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see operating conditions in Section 9 DC and AC parameters). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually in the range between 10 and 100 nF) close to the V_{CC} / V_{SS} device pins.

5.1.2 Device reset

In order to prevent erroneous instruction decoding and inadvertent write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until VCC reaches the POR threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see operating conditions in Section 9 DC and AC parameters).

At power-up, when V_{CC} passes over the POR threshold, the device is reset and is in the following state:

- in standby power mode,
- deselected,
- Status register values:
  - the write enable latch (WEL) bit is reset to 0
  - the write in progress (WIP) bit is reset to 0
  - the SRWD, BP1 and BP0 bits remain unchanged (nonvolatile bits).

It is important to note that the device must not be accessed until V_{CC} reaches a valid and stable level within the specified [V_{CC}(min), V_{CC}(max)] range, as defined under operating conditions in Section 9 DC and AC parameters.

5.1.3 Power-up conditions

When the power supply is turned on, V_{CC} rises continuously from V_{SS} to V_{CC}. During this time, the chip select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage. It is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see Figure 5. Bus master and memory devices on the SPI bus).

In addition, the chip select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge-sensitive as well as level-sensitive: after power-up, the device does not become selected until a falling edge has first been detected on chip select ($\overline{S}$). This ensures that chip select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined under operating conditions in Section 9 DC and AC parameters.

5.1.4 Power-down

During power-down (continuous decrease of the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined in Section 9 DC and AC parameters), the device must be:

- deselected (chip select $\overline{S}$ must be allowed to follow the voltage applied on V_{CC})
- in standby power mode (there must not be any internal write cycle in progress).

5.2 Active power and standby power modes

When chip select ($\overline{S}$) is low, the device is selected, and in the active power mode. The device consumes I_{CC}.

When chip select ($\overline{S}$) is high, the device is deselected. If a write cycle is not currently in progress, the device then goes into the standby power mode, and the device consumption drops to I_{CC1}, as specified in DC characteristics (see Section 9 DC and AC parameters).

5.3 Hold condition

The hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

To enter the hold condition, the device must be selected, with chip select ($\overline{S}$) low.

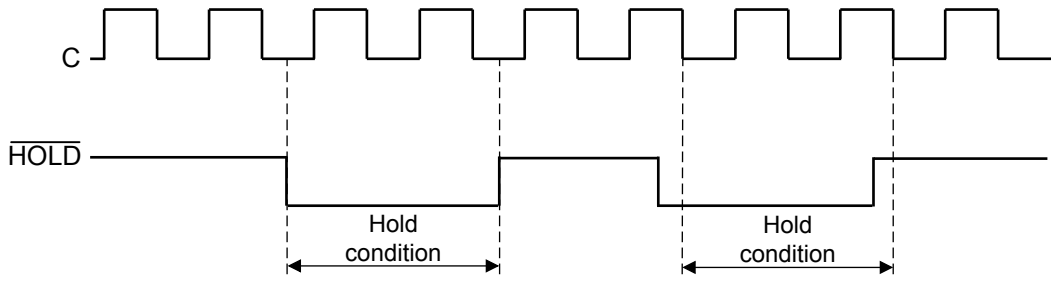
During the hold condition, the serial data output (Q) is high impedance, and the serial data input (D) and the serial clock (C) are "Don't care".

Normally, the device is kept selected for the whole duration of the Hold condition. Deselecting the device while it is in the hold condition has the effect of resetting the state of the device: this mechanism can be used, if required, to reset the ongoing processes.

Note: This resets the internal logic, except the WEL and WIP bits of the status register.

Note: In the specific case where the device has moved in a write command (Inst + Address + data bytes, each data byte being exactly 8 bits), deselecting the device also triggers the write cycle of this decoded command.

Figure 7. Hold condition activation



The hold condition starts when the hold ($\overline{HOLD}$) signal is driven low when serial clock (C) is already low (as shown in Figure 7).

Figure 7 also shows what happens if the rising and falling edges are not timed to coincide with serial clock (C) being low.

5.4 Status register

The status register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See Section 6.3 Read status register (RDSR) for a detailed description of the status register bits.

5.5 Data protection and protocol control

The device features the following data protection mechanisms:

- Before accepting the execution of the write and write status register instructions, the device checks whether the number of clock pulses comprised in the instructions is a multiple of eight.
- All instructions that modify data must be preceded by a write enable (WREN) instruction to set the write enable latch (WEL) bit.
- The block protect (BP1, BP0) bits in the status register are used to configure part of the memory as read-only.
- The write protect ($\overline{W}$) signal is used to protect the block protect (BP1, BP0) bits in the status register.

For any instruction to be accepted, and executed, chip select ($\overline{S}$) must be driven high after the rising edge of serial clock (C) for the last bit of the instruction, and before the next rising edge of serial clock (C).

Two points to note in the previous sentence:

- The “last bit of the instruction” can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for read status register (RDSR) and read (READ) instructions).
- The “next rising edge of serial clock (C)” might (or might not) be the next bus transaction for some other device on the SPI bus.

Table 3. Write-protected block size

Status register bits		Protected block	Protected array addresses
BP1	BP0		
0	0	None	None
0	1	Upper quarter	30000h - 3FFFFh
1	0	Upper half	20000h - 3FFFFh
1	1	Whole memory	00000h - 3FFFFh

6 Instructions

Each command is composed of bytes (MSB bit transmitted first), initiated with the instruction byte, as summarized in Table 4.

If an invalid instruction is sent (one not contained in Table 4), the device automatically enters in a wait state until deselected.

Table 4. Instruction set

Instruction	Description	Instruction format
WREN	Write enable	0000 0110
WRDI	Write disable	0000 0100
RDSR	Read status register	0000 0101
WRSR	Write status register	0000 0001
READ	Read from memory array	0000 0011
WRITE	Write to memory array	0000 0010
RDID	Read identification page	1000 0011
WRID	Write identification page	1000 0010
RDLS	Read identification page lock status	1000 0011
LID	Lock identification page in read-only mode	1000 0010

For read and write commands to the memory array and identification page the address is defined by three bytes as explained in Table 5.

Table 5. Significant bits within the address bytes

Instruction(1)(2)	Upper address byte								Middle address byte								Lower address byte							
	b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
READ or WRITE	X	X	X	X	X	X	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RDID or WRID	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	A7	A6	A5	A4	A3	A2	A1	A0
RDLS or LID	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X

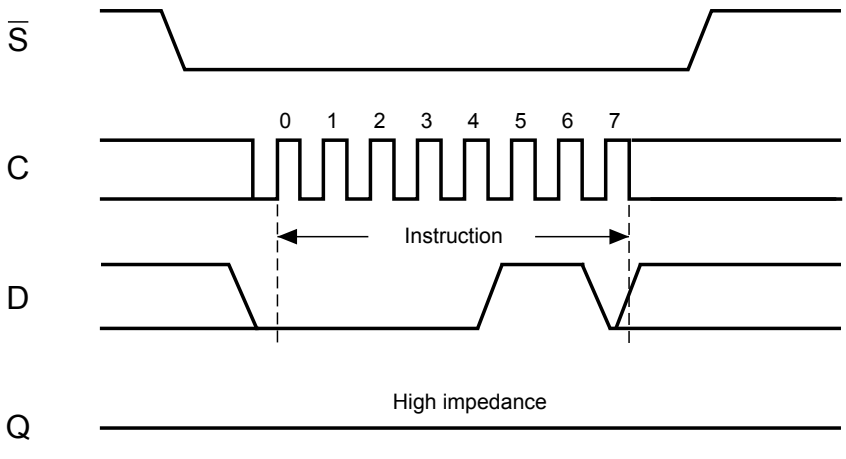
1. *A: Significant address bit*
2. *X: Don't Care bit*

6.1 Write enable (WREN)

The write enable latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a write enable instruction to the device.

As shown in Figure 8, to send this instruction to the device, chip select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on serial data input (D). The device then enters a wait state. It waits for the device to be deselected by chip select ($\overline{S}$) being driven high.

Figure 8. Write enable (WREN) sequence



6.2 Write disable (WRDI)

One way of resetting the WEL bit is to send a write disable instruction to the device.

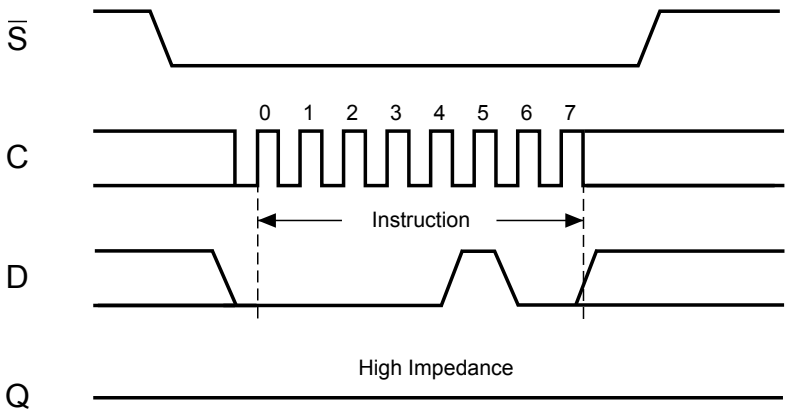
As shown in Figure 9, to send this instruction to the device, chip select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on serial data input (D).

The device then enters a wait state. It waits for the device to be deselected, by chip select ($\overline{S}$) being driven high.

The write enable latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

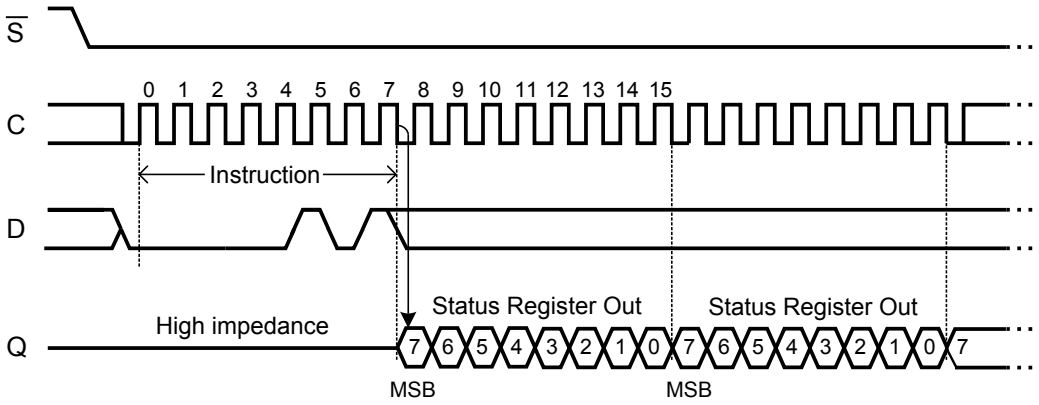
Figure 9. Write disable (WRDI) sequence



6.3 Read status register (RDSR)

The read status register (RDSR) instruction is used to read the status register. The status register may be read at any time, even while a write or write status register cycle is in progress. When one of these cycles is in progress, it is recommended to check the write in progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status register continuously, as shown in Figure 10.

Figure 10. Read Status register (RDSR) sequence



The status and control bits of the status register are detailed in the following subsections.

6.3.1 WIP bit

The write in progress (WIP) bit indicates whether the memory is busy with a write or write status register cycle. When set to 1, such a cycle is in progress, when reset to 0, no such cycle is in progress.

6.3.2 WEL bit

The WEL bit (write enable latch) bit is a flag that indicates the status of the internal write enable latch.

When WEL is set to 1, the internal write latch is set; when WEL is set to 0, the internal write enable latch is reset, and no write or write status register instruction is accepted.

The WEL bit is returned to its reset state by the following events:

- Power-up
- Write disable (WRDI) instruction completion
- Write status register (WRSR) instruction completion
- Write (WRITE) instruction completion

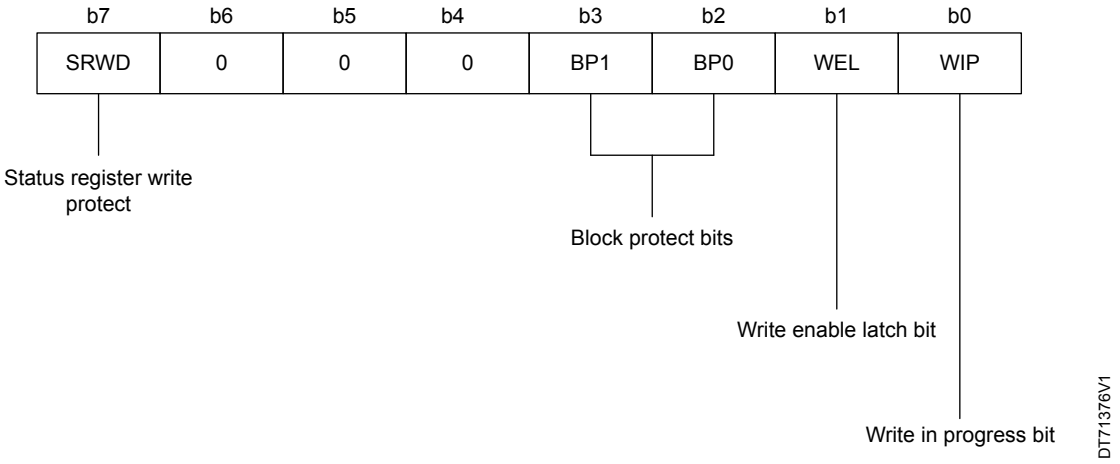
6.3.3 BP1, BP0 bits

The block protect (BP1, BP0) bits are nonvolatile. They define the size of the area to be software-protected against write instructions. These bits are written with the write status register (WRSR) instruction. When one or both of the block protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 3. Write-protected block size) becomes protected against write (WRITE) instructions. The block protect (BP1, BP0) bits can be written provided that the hardware protected mode has not been set.

6.3.4 SRWD bit

The status register write disable (SRWD) bit is operated in conjunction with the write protect ($\overline{W}$) signal. The status register write disable (SRWD) bit and write protect ($\overline{W}$) signal enable the device to be put in the hardware protected mode (when the status register write disable (SRWD) bit is set to 1, and write protect ($\overline{W}$) is driven low). In this mode, the non-volatile bits of the status register (SRWD, BP1, BP0) become read-only bits and the write status register (WRSR) instruction is no longer accepted for execution.

Figure 11. Status register format



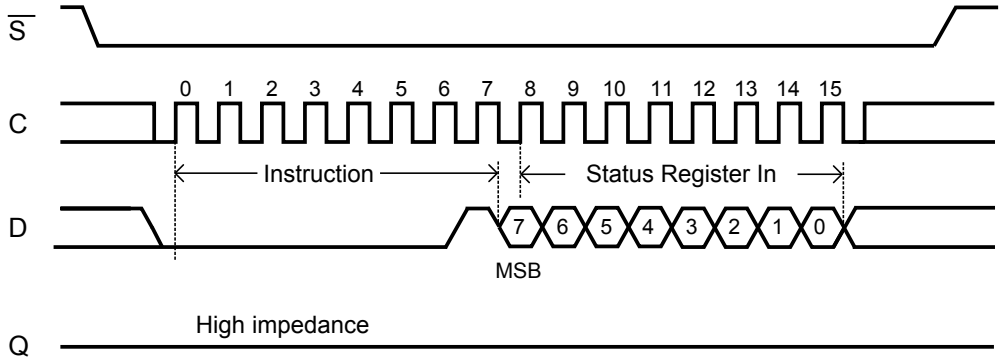
6.4 Write status register (WRSR)

The write dtatus register (WRSR) instruction is used to write new values to the status register. Before it can be accepted, a write enable (WREN) instruction must have been previously executed.

The write Status register (WRSR) instruction is entered by driving chip select ($\overline{S}$) low, followed by the instruction code, the data byte on serial data input (D) and chip select ($\overline{S}$) driven high. Chip select ($\overline{S}$) must be driven high after the rising edge of serial clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of serial clock (C). Otherwise, the write status register (WRSR) instruction is not executed.

The instruction sequence is shown in Figure 12.

Figure 12. Write status register (WRSR) sequence



Driving the chip select ($\overline{S}$) signal high at a byte boundary of the input data triggers the self-timed write cycle that takes t_W to complete (as specified in AC tables in Section 9 DC and AC parameters).

While the write status register cycle is in progress, the status register may still be read to check the value of the write in progress (WIP) bit: the WIP bit is 1 during the self-timed write cycle t_W, and 0 when the write cycle is complete. The WEL bit (Write enable latch) is also reset at the end of the write cycle t_W.

The write status register (WRSR) instruction enables the user to change the values of the BP1, BP0 and SRWD bits:

- The block protect (BP1, BP0) bits define the size of the area that is to be treated as read-only, as defined in Table 3. Write-protected block size.
- The SRWD (status register write disable) bit, in accordance with the signal read on the write protect pin ($\overline{W}$), enables the user to set or reset the write protection mode of the status register itself, as defined in Table 6. When in write-protected mode, the write status register (WRSR) instruction is not executed.

The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the t_W write cycle.

The write status register (WRSR) instruction has no effect on the b6, b5, b4, b1, b0 bits in the status register. Bits b6, b5, b4 are always read as 0.

Table 6. Protection modes

W signal	SRWD bit	Mode	Write protection of the Status register	Memory content	
				Protected area(1)	Unprotected area(1)
1	0	Software-protected (SPM)	Status register is writable (if the WREN instruction has set the WEL bit). The values in the BP1 and BP0 bits can be changed.	Write-protected	Ready to accept write instructions
0	0				
1	1				
0	1	Hardware-protected (HPM)	Status register is hardware write-protected. The values in the BP1 and BP0 bits cannot be changed.	Write-protected	Ready to accept write instructions

1. *As defined by the values in the Block protect (BP1, BP0) bits of the Status register. See Table 3. Write-protected block size.*

The protection features of the device are summarized in Table 6.

When the status register write disable (SRWD) bit in the status register is 0 (its initial delivery state), it is possible to write to the status register (provided that the WEL bit has previously been set by a WREN instruction), regardless of the logic level applied on the write protect ($\overline{W}$) input pin.

When the status register write disable (SRWD) bit in the Status register is set to 1, two cases should be considered, depending on the state of the write protect ($\overline{W}$) input pin:

- If write protect ($\overline{W}$) is driven high, it is possible to write to the status register (provided that the WEL bit has previously been set by a WREN instruction).
- If write protect ($\overline{W}$) is driven low, it is not possible to write to the status register even if the WEL bit has previously been set by a WREN instruction. (attempts to write to the status register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area, which are software-protected (SPM) by the block protect (BP1, BP0) bits in the status register, are also hardware-protected against data modification.

Regardless of the order of the two events, the hardware-protected mode (HPM) can be entered by:

- either setting the SRWD bit after driving the write protect ($\overline{W}$) input pin low,
- or driving the write protect ($\overline{W}$) input pin low after setting the SRWD bit.

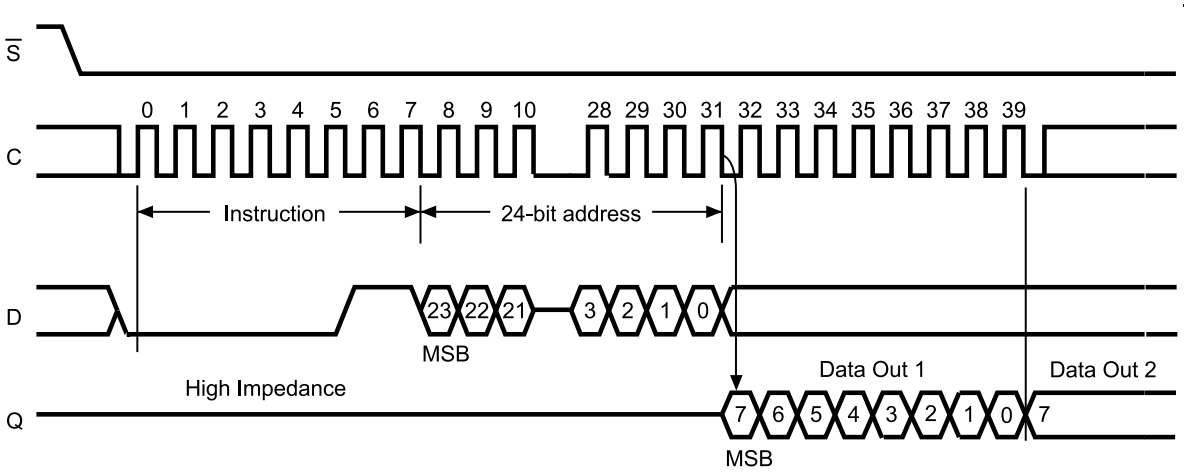
Once the hardware-protected mode (HPM) has been entered, the only way of exiting it is to pull high the write protect ($\overline{W}$) input pin.

If the write protect ($\overline{W}$) input pin is permanently tied high, the hardware-protected mode (HPM) can never be activated, and only the software-protected mode (SPM), using the block protect (BP1, BP0) bits in the status register, can be used.

6.5 Read from memory array (READ)

As shown in Figure 13, to send this instruction to the device, chip select ($\overline{S}$) is first driven low. The bits of the instruction byte and address bytes are then shifted in, on serial data input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on serial data output (Q).

Figure 13. Read from memory array (READ) sequence



If chip select ($\overline{S}$) continues to be driven low, the internal address register is incremented automatically, and the byte of data at the new address is shifted out.

When the highest address is reached, the address counter rolls over to zero, allowing the read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The read cycle is terminated by driving chip select ($\overline{S}$) high. The rising edge of the chip select ($\overline{S}$) signal can occur at any time during the cycle.

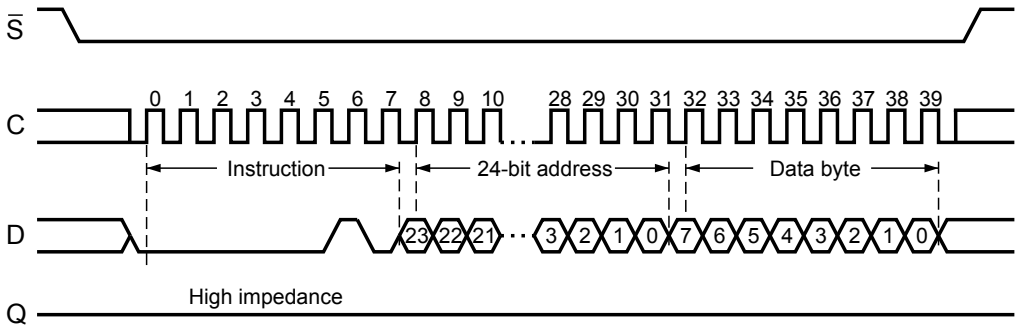
The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

6.6 Write to memory array (WRITE)

As shown in Figure 14, to send this instruction to the device, chip select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on serial data input (D).

The instruction is terminated by driving chip select ($\overline{S}$) high at a byte boundary of the input data. The self-timed write cycle, triggered by the chip select ($\overline{S}$) rising edge, continues for a period t_W (as specified in AC characteristics in Section 9 DC and AC parameters), at the end of which the write in progress (WIP) bit is reset to 0.

Figure 14. Byte write (WRITE) sequence



In the case of Figure 14, chip select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. However, if chip select ($\overline{S}$) continues to be driven low (as shown in Figure 15), the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal write cycle.

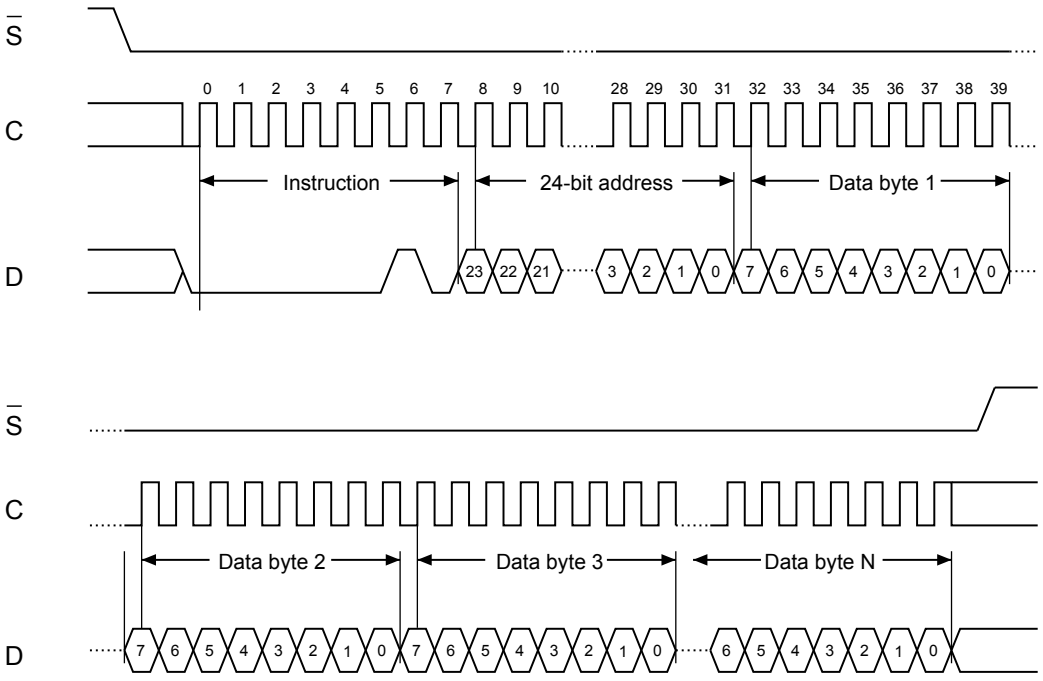
Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If more bytes are sent than will fit up to the end of the page, a condition known as “roll-over” occurs. In case of roll-over, the bytes exceeding the page size are overwritten from location 0 of the same page.

The instruction is not accepted, and is not executed, under the following conditions:

- if the write enable latch (WEL) bit has not been set to 1 (by executing a write enable instruction just before),
- if a write cycle is already in progress,
- if the device has not been deselected, by driving high chip select ($\overline{S}$), at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in),
- if the addressed page is in the region protected by the block protect (BP1 and BP0) bits.

Note: The self-timed write cycle t_W is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as “0” and a programmed bit is read as “1”.

Figure 15. **Page write (WRITE) sequence**



6.6.1 Cycling with error correction code (ECC x4)

M95M02-D devices offer an error correction code (ECC), an internal logic function transparent for the SPI communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes. (A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer). Inside a group, if a single bit out of the four bytes happens to be erroneous during a read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the four bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined in Table 11. Cycling performance by groups of four bytes.

6.7 Read identification page

The identification page (256 bytes) is an additional page that can be written and (later) permanently locked in read-only mode.

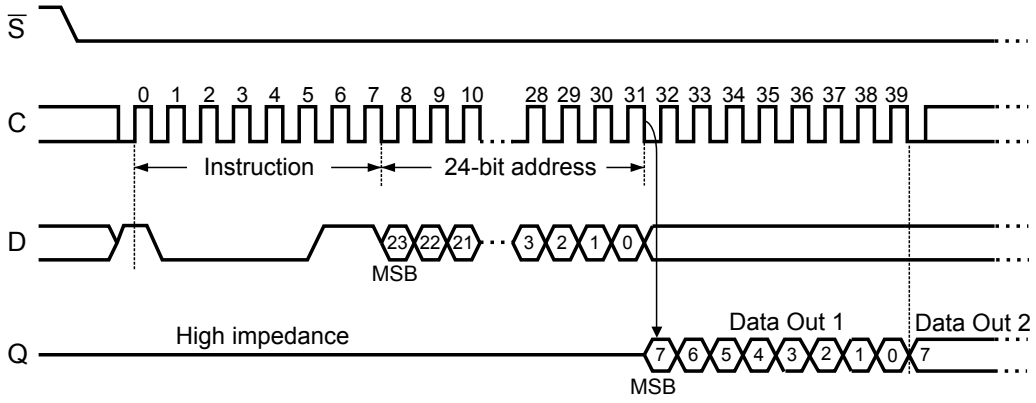
This page is read with the read identification page instruction (see Table 4. Instruction set). The chip select signal ($\overline{S}$) is first driven low, the bits of the instruction byte and address bytes are then shifted in, on serial data input (D). Address bit A10 must be 0, upper address bits are "don't care", and the data byte pointed to by the lower address bits [A7:A0] is shifted out on serial data output (Q). If chip select ($\overline{S}$) continues to be low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

The number of bytes to read in the ID page must not exceed the page boundary, otherwise unexpected data is read (for example, when reading the ID page from location 90d, the number of bytes should be lower than or equal to 166d, as the ID page boundary is 256 bytes).

The read cycle is terminated by driving chip select ($\overline{S}$) high. The rising edge of the chip select ($\overline{S}$) signal can occur at any time during the cycle. The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 16. Read identification page sequence

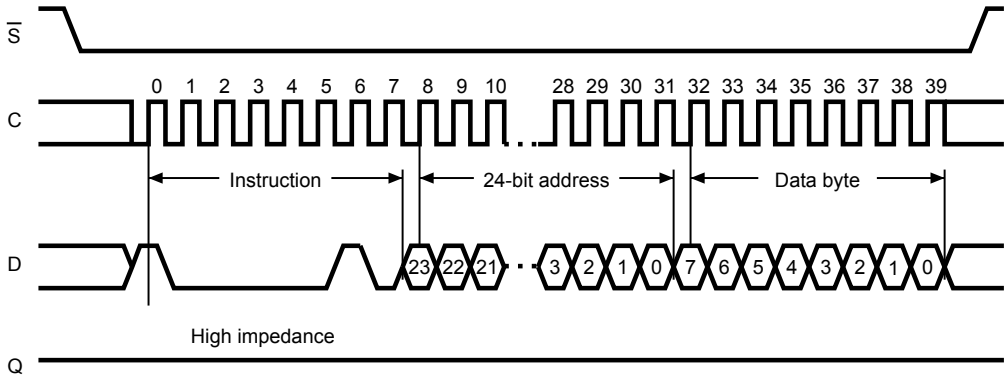


6.8 Write identification page

The identification page (256 bytes) is an additional page that can be written and (later) permanently locked in read-only mode.

Writing this page is achieved with the write identification page instruction (see Table 4. Instruction set). The chip select signal ($\overline{S}$) is first driven low. The bits of the instruction byte, address bytes, and at least one data byte are then shifted in on serial data input (D). Address bit A10 must be 0, the upper address bits are "don't care", and the lower address bits [A7:A0] define the byte address within the identification page. The instruction sequence is shown in Figure 17.

Figure 17. Write identification page sequence

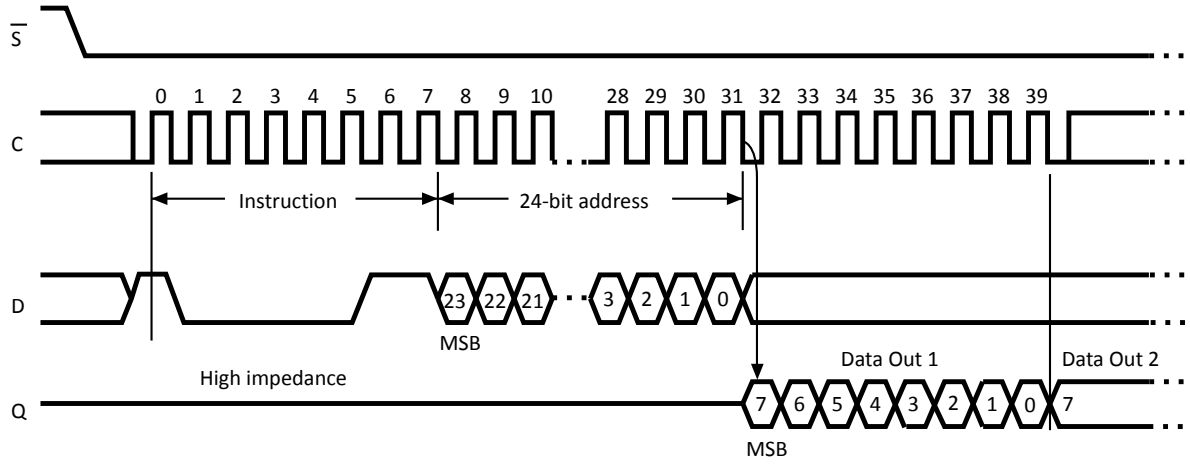


6.9 Read lock status (available only in M95M02-D device)

The read lock status instruction (see Table 4. Instruction set) is used to check whether the identification page is locked or not in Read-only mode. The read lock status sequence is defined with the chip select ($\overline{S}$) first driven low. The bits of the instruction byte and address bytes are then shifted in on serial data input (D). Address bit A10 must be 1, all other address bits are "Don't Care". The lock bit is the LSB (least significant bit) of the byte read on serial data output (Q). It is at “1” when the lock is active and at “0” when the lock is not active. If chip select ($\overline{S}$) continues to be driven low, the same data byte is shifted out. The read cycle is terminated by driving chip select ($\overline{S}$) high.

The instruction sequence is shown in Figure 18.

Figure 18. Read lock status sequence



6.10 Lock ID

The lock ID instruction permanently locks the identification page in read-only mode. Before this instruction can be accepted, a write enable (WREN) instruction must have been executed.

The lock ID instruction is issued by driving chip select ($\overline{S}$) low, sending the instruction code, the address and a data byte on serial data input (D), and driving chip select ($\overline{S}$) high. In the address sent, A10 must be equal to 1, all other address bits are "Don't Care". The data byte sent must be equal to the binary value xxxx xx1x, where x = Don't Care.

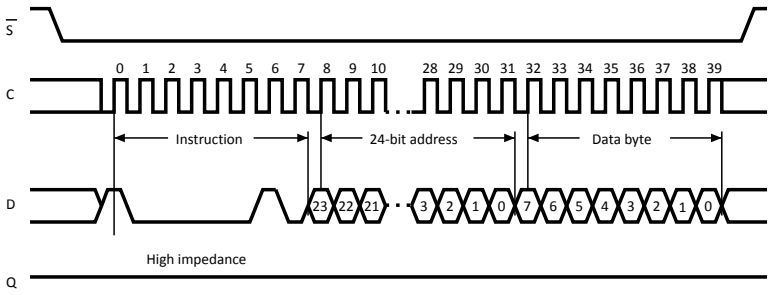
Chip select ($\overline{S}$) must be driven high after the rising edge of serial clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of serial clock (C). Otherwise, the lock ID instruction is not executed.

Driving chip select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed write cycle whose duration is t_W (as specified in AC characteristics in Section 9 DC and AC parameters). The instruction sequence is shown in Figure 19.

The instruction is discarded, and is not executed, under the following conditions:

- If a write cycle is already in progress
- If block protect bits (BP1, BP0) = (1, 1)
- If a rising edge on chip select ($\overline{S}$) happens outside of a byte boundary

Figure 19. Lock ID sequence



7 Power-up and delivery state

7.1 Power-up state

After power-up, the device is in the following state:

- standby power mode
- deselected (after power-up, a falling edge is required on chip select ($\overline{S}$) before any instructions can be started)
- not in the hold condition
- the write enable latch (WEL) is reset to 0
- write in progress (WIP) is reset to 0.

The SRWD, BP1 and BP0 bits of the status register are unchanged from the previous power-down (they are non-volatile bits).

7.2 Initial delivery state

The device is delivered with the memory array and identification page bits set to all 1s (each byte = FFh). The status register write disable (SRWD) and block protect (BP1 and BP0) bits are initialized to 0.

8 Maximum ratings

Stressing the device outside the ratings listed in Table 7 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{AMB}	Ambient operating temperature	-40	130	°C
T_{STG}	Storage temperature	-65	150	
T_{LEAD}	Lead temperature during soldering	See note (1)		
V_O	Output voltage	-0.50	V_{CC} + 0.6	V
V_I	Input voltage	-0.50	6.5	
V_{CC}	Supply voltage	-0.50	6.5	
I_{OL}	DC output current (Q = 0)	-	5	mA
I_{OH}	DC output current (Q = 1)	-	5	
V_{ESD}	Electrostatic discharge voltage (human body model)(2)	-	3000	V

1. *Compliant with JEDEC standard J-STD-020 (for small-body, Sn-Pb or Pb free assembly), the ST ECOPACK 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses applied on different combinations of pin connections, according to ANSI/ESDA/JEDEC JS-001 (C1=100 pF, R1=1500 Ω, and R2=500 Ω).*

9 DC and AC parameters

This section summarizes the operating conditions and the DC/AC characteristics.

Table 8. Operating conditions (M95M02-DR, device grade 6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	-40	85	°C

Table 9. Operating conditions (M95M02-DF, device grade 5)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	-20	85	°C

Table 10. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	-	30	pF
-	Input rise and fall times	-	25	ns
-	Input pulse voltages	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input and output timing reference voltages	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 20. AC measurement I/O waveform

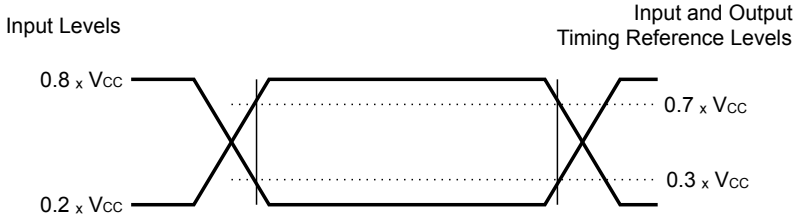


Table 11. Cycling performance by groups of four bytes

Symbol	Parameter	Test condition	Min.	Max.	Unit
Ncycle	Write cycle endurance(1)	$T_A \leq$ 25 °C, V_{CC}(min) < V_{CC} < V_{CC}(max)	-	4,000,000	Write cycle (2)
		T_A = 85 °C, V_{CC}(min) < V_{CC} < V_{CC}(max)	-	1,200,000	

1. *The write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer. The write cycle endurance is defined by characterization and qualification.*
2. *A write cycle is executed when either a page write, a byte write, a WRSR, a WRID or an LID instruction is decoded. When using the byte write, the page write or the WRID instruction, refer also to Section 6.6.1 Cycling with error correction code (ECC x4).*

Table 12. Memory cell data retention

Parameter	Test conditions	Min.	Unit
Data retention(1)	T_A = 55 °C	200	Year

1. *The data retention behaviour is checked in production, while the 200-year limit is defined from characterization and qualification results.*

Table 13. Capacitance

Symbol	Parameter	Test conditions(1)	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V	-	8	pF
C_{IN}	Input capacitance (D)	V_{IN} = 0 V	-	8	pF
	Input capacitance (other pins)	V_{IN} = 0 V	-	6	pF

1. *Evaluated by characterization – not tested in production.*

Table 14. DC characteristics

Symbol	Parameter	Test conditions	Min	Max	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}	-	±2	µA
I_{LO}	Output leakage current	$\overline{S}= V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}	-	±2	
I_{CC}	Supply current (Read)	C = 0.1 V_{CC} / 0.9 V_{CC} at 5 MHz, 1.8 V(1) ≤ V_{CC} ≤ 5.5 V, Q = open	-	3	mA
I_{CC0}(2)	Supply current (Write)	During t_W, $\overline{S}$ = V_{CC},	-	3	mA
I_{CC1}	Supply current (Standby power mode)	$\overline{S}= V_{CC}$, $V_{IN}= V_{SS}$ or V_{CC}, V_{CC} = 1.8 V(1)	-	3	µA
		$\overline{S}= V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}, 1.8 V(1) ≤ V_{CC} < 2.5 V	-	5	
		$\overline{S}= V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}, 2.5 V ≤ V_{CC} ≤ 5.5 V	-	5	
V_{IL}	Input low voltage	1.8 V(1) ≤ V_{CC} < 2.5 V	-0.45	0.25 V_{CC}	V
		2.5 V ≤ V_{CC} ≤ 5.5 V	-0.45	0.30 V_{CC}	
V_{IH}	Input high voltage	1.8 V(1) ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC} + 1	
		2.5 V ≤ V_{CC} ≤ 5.5 V	0.70 V_{CC}	V_{CC} + 1	
V_{OL}	Output low voltage	I_{OL} = 0.15 mA, V_{CC} = 1.8 V(1)	-	0.3	
		V_{CC} = 2.5 V, I_{OL} = 1.5 mA, or V_{CC} = 5.0 V, I_{OL} = 2.0 mA	-	0.4	
V_{OH}	Output high voltage	I_{OH} = -0.1 mA, V_{CC} = 1.8 V(1)	0.80 V_{CC}	-	
		V_{CC} = 2.5 V, I_{OH} = -0.4 mA, or V_{CC} = 5 V, I_{OH} = -2.0 mA			

1. *V_{CC} = 1.7 V for M95M02-DF.*
2. *Evaluated by characterization - not tested in production.*

Table 15. AC characteristics

Test conditions specified in Table 8, Table 9 and Table 10					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	DC	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	60	-	ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	60	-	ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	90	-	ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	60	-	ns
t_{CHSL}	-	$\overline{S}$ not active hold time	60	-	ns
t_{CH}(1)	t_{CLH}	Clock high time	90	-	ns
t_{CL}(1)	t_{CLL}	Clock low time	90	-	ns
t_{CLCH}(2)	t_{RC}	Clock rise time	-	2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time	-	2	µs
t_{DVCH}	t_{DSU}	Data in setup time	20	-	ns
t_{CHDX}	t_{DH}	Data in hold time	20	-	ns
t_{HHCH}	-	Clock low hold time after $\overline{HOLD}$ not active	60	-	ns
t_{HLCH}	-	Clock low hold time after $\overline{HOLD}$ active	60	-	ns
t_{CLHL}	-	Clock low set-up time before $\overline{HOLD}$ active	0	-	ns
t_{CLHH}	-	Clock low set-up time before $\overline{HOLD}$ not active	0	-	ns
t_{SHQZ}(2)	t_{DIS}	Output disable time	-	80	ns
t_{CLQV}	t_V	Clock low to output valid	-	80	ns
t_{CLQX}	t_{HO}	Output hold time	0	-	ns
t_{QLQH}(2)	t_{RO}	Output rise time	-	80	ns
t_{QHQL}(2)	t_{FO}	Output fall time	-	80	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid	-	80	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z	-	80	ns
t_W	t_{WC}	Write time	-	10	ms

1. *t_{CH} + t_{CL} must never be less than the shortest possible clock period, 1 / f_C(max)*
2. *Evaluated by characterization - not tested in production.*

Figure 21. **Serial input timing**

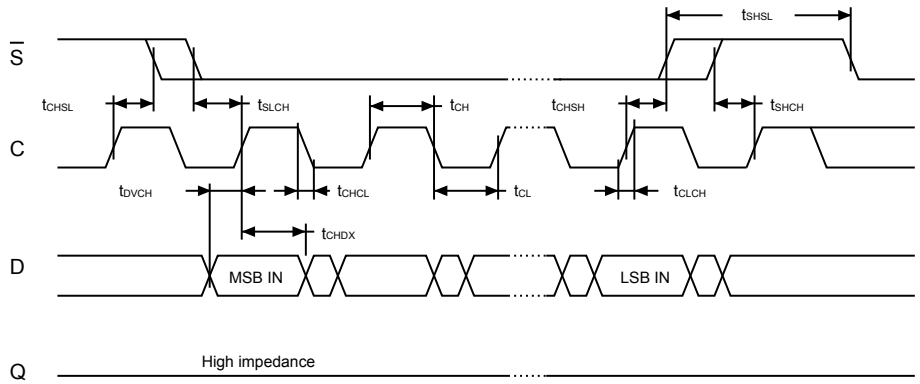


Figure 22. **Hold timing**

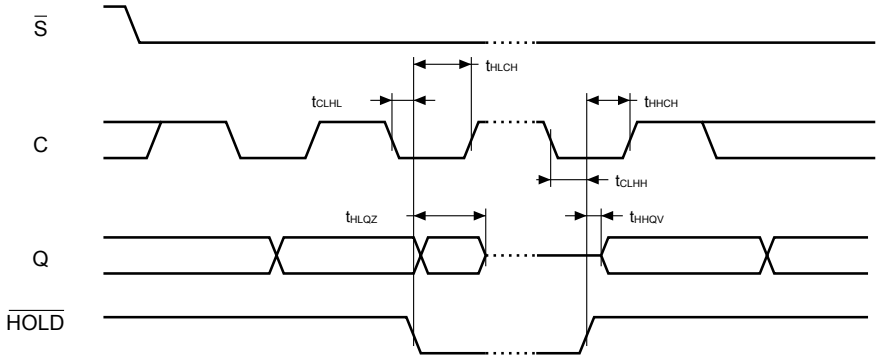
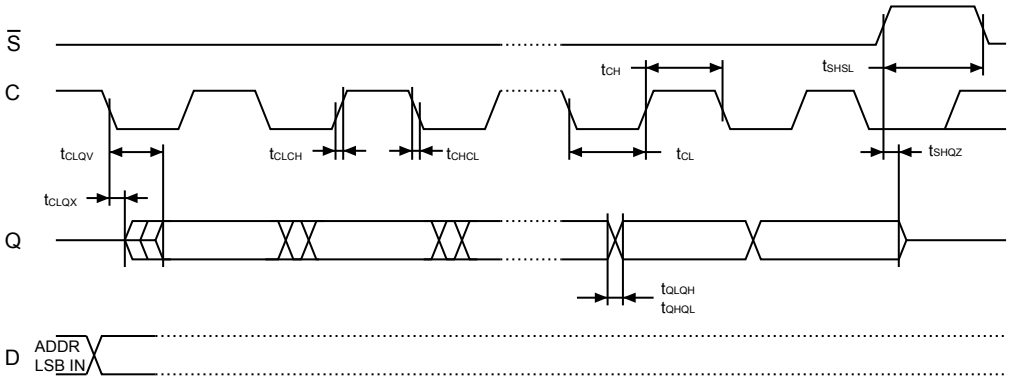


Figure 23. **Serial output timing**



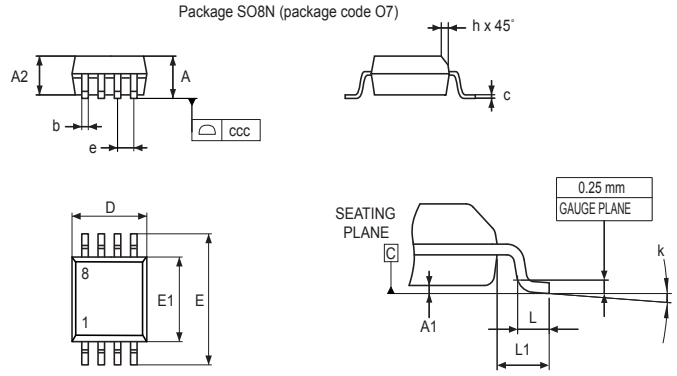
10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 SO8N package information

This SO8N is an 8-lead, 4.9 x 6 mm, plastic small outline, 150 mils body width, package.

Figure 24. SO8N – Outline



1. Drawing is not to scale.

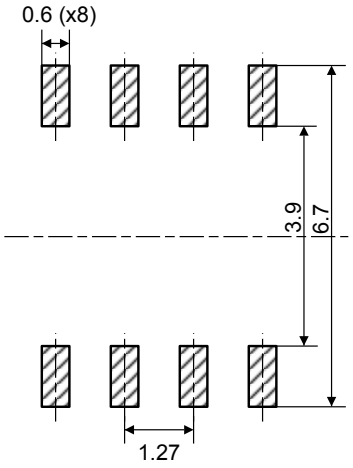
Table 16. SO8N – Mechanical data

Symbol	millimeters			inches (1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.100	-	0.230	0.0039	-	0.0091
D(2)	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1(3)	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side*
3. *Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Note: The package top may be smaller than the package bottom. Dimensions D and E1 are determinated at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interleads flash, but including any mismatch between the top and bottom of plastic body. Measurement side for mold flash, protusions or gate burrs is bottom side.

Figure 25. SO8N - Recommended footprint

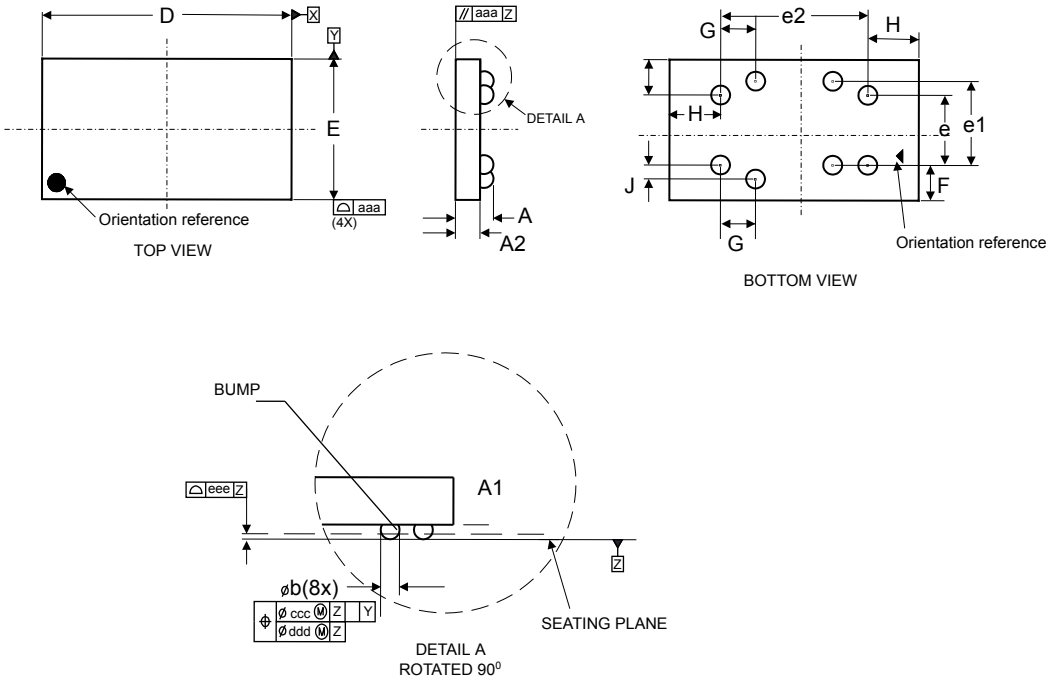


1. Dimensions are expressed in millimeters.

10.2 WLCSP8 without BSC package information

This WLCSP is a 8-ball, 3.556 x 2.011 mm, without BSC, wafer level chip scale package.

Figure 26. WLCSP8 without BSC - Outline



E1a_WLCSP8_noBSC_ME_V1

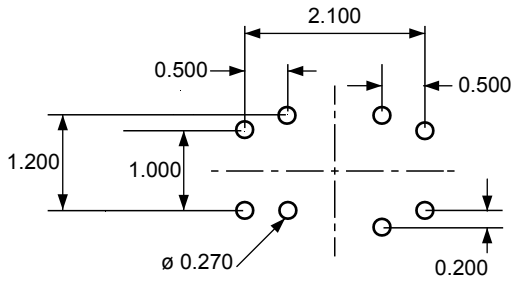
1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

Table 17. WLCSP8 without BSC - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.540	0.580	0.0197	0.0213	0.0228
A1	-	0.190	-	-	0.0075	-
A2	-	0.350	-	-	0.0138	-
b[2]	-	0.270	-	-	0.0106	-
D	-	3.556	3.576	-	0.1400	0.1408
E	-	2.011	2.031	-	0.0792	0.0800
e	-	1.000	-	-	0.0394	-
e1	-	1.200	-	-	0.0472	-
e2	-	2.100	-	-	0.0827	-
F	-	0.505	-	-	0.0199	-
G	-	0.500	-	-	0.0197	-
H	-	0.728	-	-	0.0287	-
J	-	0.200	-	-	0.0079	-
aaa	-	0.110	-	-	0.0043	-
bbb	-	0.110	-	-	0.0043	-
ccc	-	0.110	-	-	0.0043	-
ddd	-	0.060	-	-	0.0024	-
eee	-	0.060	-	-	0.0024	-

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *Dimension is measured at the maximum bump diameter parallel to primary datum Z.*

Figure 27. WLCSP8 without BSC - Recommended footprint



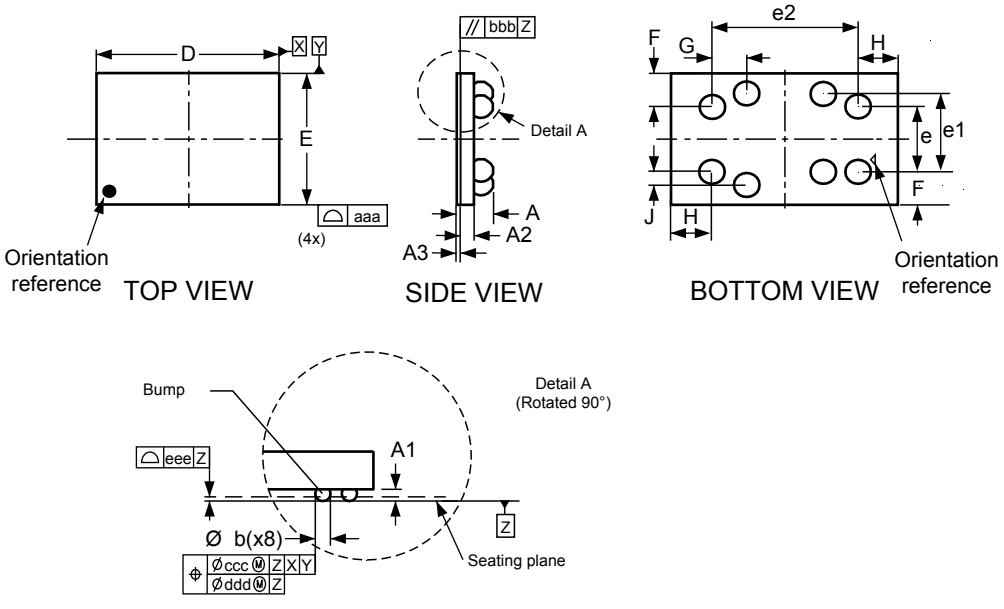
E1_WLCSP8_FP_V1

1. Dimensions are expressed in millimeters.

10.3 WLCSP8 with BSC package information

This WLCSP is a 8-ball, 3.556 x 2.011 mm, with BSC, wafer level chip scale package.

Figure 28. WLCSP8 with BSC - Outline



E1a_WLCSP8_withBSC_ME_V1

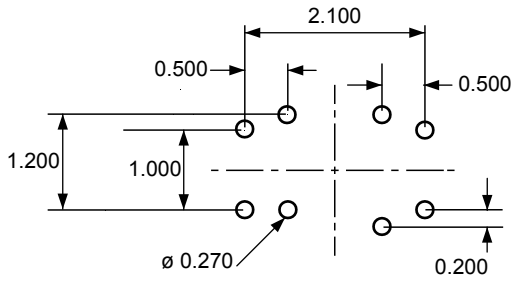
1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

Table 18. WLCSP8 with BSC - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.565	0.605	0.0207	0.0222	0.0238
A1	-	0.190	-	-	0.0075	-
A2	-	0.350	-	-	0.0138	-
A3	-	0.025	-	-	0.0010	-
b[2]	-	0.270	-	-	0.0106	-
D	-	3.556	3.576	-	0.1400	0.1408
E	-	2.011	2.031	-	0.0792	0.0800
e	-	1.000	-	-	0.0394	-
e1	-	1.200	-	-	0.0472	-
e2	-	2.100	-	-	0.0827	-
F	-	0.505	-	-	0.0199	-
G	-	0.500	-	-	0.0197	-
H	-	0.728	-	-	0.0287	-
J	-	0.200	-	-	0.0079	-
aaa	-	0.110	-	-	0.0043	-
bbb	-	0.110	-	-	0.0043	-
ccc	-	0.110	-	-	0.0043	-
ddd	-	0.060	-	-	0.0024	-
eee	-	0.060	-	-	0.0024	-

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *Dimension is measured at the maximum bump diameter parallel to primary datum Z.*

Figure 29. WLCSP8 with BSC - Recommended footprint



E1_WLCSP8_FP_V1

1. Dimensions are expressed in millimeters.

11 Ordering information

Table 19. Ordering information scheme

Example: M95 M02 -D R MN 6 T P /K

Device type

M95 = SPI serial access EEPROM

Device function

M02 = 2048 Kbit

Device family

-D = with additional identification page

Operating voltage

R = V_{CC} = 1.8 V to 5.5 V

F = V_{CC} = 1.7 V to 5.5 V

Package(1)

MN = SO8N (150 mil width)

CS = WLCSP8

Device grade

6 = Industrial temperature range: -40 to 85 °C(2)

5 = Industrial temperature range: -20 to 85 °C(2)

Option

T = Tape and reel packing

blank = tube packing

Plating technology

P or G = RoHS compliant and halogen-free (ECOPACK2)

Process (3) **and option**

/K = Manufacturing technology code, without back side coating

/KF = Manufacturing technology code, with back side coating

1. *All packages are ECOPACK2 (RoHS-compliant and free of brominated, chlorinated and antimony-oxide flame retardants).*
2. *Device tested with standard test flow.*
3. *These process letters appear on the device package (marking) and on the shipment box. Please contact your nearest ST Sales Office for further information.*

Note: For a list of available options (speed, package, etc.) or for further information on any aspect of this device, contact your nearest ST sales office.

Note: Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Revision history

Table 20. **Document revision history**

Date	Revision	Changes
15-Nov-2010	1	Initial release.
10-Dec-2010	2	Updated DC and AC characteristics according to characterization test results.
10-Jan-2011	3	Updated ordering information.
10-May-2011	4	Updated Table 13: AC characteristics and related text, and Table 12: DC characteristics.
19-Oct-2011	5	Changed datasheet status to full datasheet. Modified Section 1: Description. Added Figure 3: WLSCP connections (bump side view). Updated Figure 4: Bus master and memory devices on the SPI bus and Figure 7: Block diagram. Modified Section 7: ECC (error correction code) and write cycling. Updated Note 2 in Table 7: Absolute maximum ratings. Added Table 8: Memory cell characteristics. Updated Figure 24: M95M02-DR WLCSP package outline and Table 15: M95M02-DR WLCSP package mechanical data. Updated disclaimer on last page.
04-Oct-2012	6	Text and structure of document modified as per new M95xxx standard EEPROM datasheet template. Updated: • Cycling: 4 million cycles • Data retention: 200 years Added: • Standard WLCSP (CS)
19-Dec-2012	7	Updated Section 7.2: Initial delivery state. Restored Figure 23, Figure 24 and Figure 25.
13-Mar-2013	8	Document reformatted. Replaced “ball” by “bump” in the entire document. Deleted Figure 3: Thin WLCSP connections (bump side view), Figure 24: M95M02-DR thin WLCSP package (CT) outline, bump side view and Table 15: M95M02-DR thin WLCSP package mechanical data. Renamed Figure 39: M95M02-DRCS6TP/K, WLCSP standard package outline, bump side view and Table 55: M95M02-DRCS6TP/K, WLCSP package mechanical data. Updated package information in Table 20: Ordering information scheme.
15-Sep-2014	9	Updated WLCSP (CS) package figure on cover page. Removed “Preliminary data” footnote from Figure 3, Figure 24 and Table 16. Removed note about exposure to UV light in Section 10: Package information. Updated Table 4: Instruction set, and removed footnotes from it. Added Table 5: Significant bits within the address bytes and Figure 27: WLCSP 8-bump wafer length chip-scale recommended land pattern. Updated Note 1 in Table 12: Absolute maximum ratings. Updated Table 16: AC characteristics and Table 20: Ordering information scheme.
22-Jun-2015	10	Updated Features and WLCSP figure on cover page. Updated Figure 3: WLCSP connections, Figure 4: Block diagram and Figure 14: Page Write (WRITE) sequence.

Date	Revision	Changes
		Updated Section 5.1.3: Power-up conditions and Section 6: Instructions. Added Table 2: Signals vs. bump position and updated Table 3: Write-protected block size and footnotes of Table 8: Absolute maximum ratings. Updated Section 10: Package information, Section 10.1: SO8N package information and Section 10.2: WLCSP package information. Updated footnote 1 of Table 20: Ordering information scheme and added Note: on Engineering samples.
28-Sep-2018	11	Updated Figure 1: Logic diagram, Figure 7: Hold condition activation, Figure 8: Write enable (WREN) sequence, Figure 9: Write disable (WRDI) sequence, Figure 10: Read Status register (RDSR) sequence, Figure 11: Write Status register (WRSR) sequence, Figure 13: Byte Write (WRITE) sequence and Figure 15: Read Identification page sequence. Updated title of Section 6.6.1: Cycling with error correction code (ECC x4) and of Section 11: Ordering information, and Note: in it. Updated Section 10.1: SO8N package information and Section 10.2: WLCSP8 package information. Updated Table 11: AC measurement conditions and Table 20: Ordering information scheme. Minor text edits across the whole document.
28-Aug-2019	12	Added M95M02-DF. Updated Features, Section 1: Description and Section 11: Ordering information. Updated Figure 1: Logic diagram. Updated Table 15: DC characteristics. Added Table 10: Operating conditions (M95M02-DF, device grade 5). Minor text edits across the whole document.
24-Oct-2022	13	Updated: • Features • Section 2 Block diagram • Section 4 Connecting to the SPI bus • Table 16. SO8N – Mechanical data • Section 11 Ordering information Minor text edits across the whole document.

Contents

List of figures

List of tables