MINI-ANALOG SERIES
CMOS SINGLE MIDDLE-BAND OPERATIONAL AMPLIFIER S-89410A

The mini analog series is a group of ICs that incorporate a general-purpose analog circuit in a small package.
The S-89410A is a CMOS type middle-band operational amplifier that includes a phase compensation circuit and that can be driven at a lower voltage with lower current consumption than existing bipolar operational amplifiers. These features make this product ideal for use in small battery-powered portable equipments.

■ Features

- Bandwidth : 550 kHz (typ.) @Gain = 1
- Can be driven at lower voltage than existing general-purpose operational amplifiers : V_{DD} = 1.2 to 5.5 V
- Low current consumption Operating mode : I_{DD} = 135 μA (typ.) @1.2 V
  Shutdown mode : I_{DD} = 0.1 μA (typ.)
- Wide I/O voltage range : V_{CMR} = V_{SS} to V_{DD}
- Large output current
- External elements not required due to internal phase compensation
- Small package : SOT-23-6

■ Applications

- Cellular phones
- PDAs
- Notebook PCs
- Digital cameras
- Digital video cameras

■ Package

- SOT-23-6 (Package drawing code : MP006-A)

■ Product Code

- Product code S-89410ALMD-HNO-TF
- Delivery form: Taping only

■ Pin Configurations

SOT-23-6
Top view

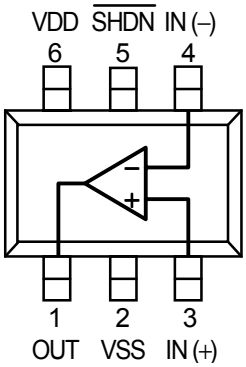


Figure 1

Table 1

Pin No.	Symbol	Description	Internal equivalent circuit
1	OUT	Output pin	**Figure 2**
2	VSS	GND pin	—
3	IN (+)	Non-inverted input pin	**Figure 3**
4	IN (–)	Inverted input pin	**Figure 3**
5	$\overline{\text{SHDN}}$	Shutdown pin	**Figure 5**
6	VDD	Positive power supply pin	**Figure 4**

■ Internal Equivalent Circuits

(1) Output pin

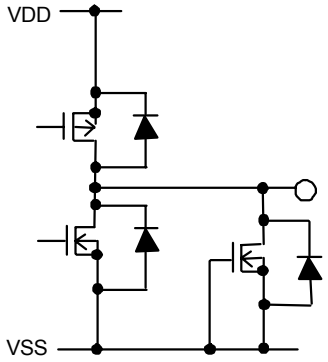


Figure 2

(2) Input pin

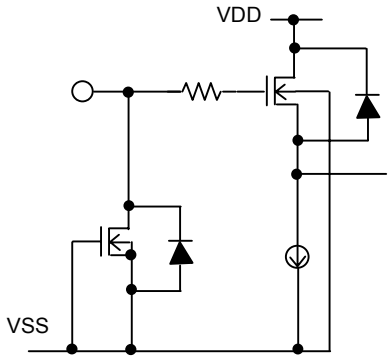


Figure 3

(3) VDD pin

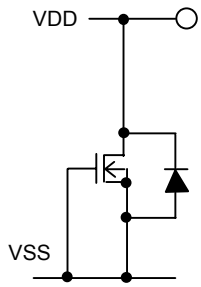


Figure 4

(4) $\overline{\text{SHDN}}$ pin

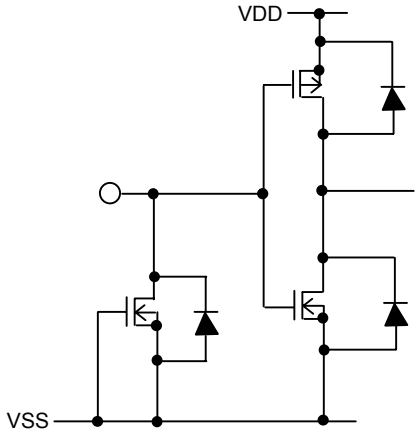


Figure 5

■ Absolute Maximum Ratings

Table 2

Item	Symbol	Absolute maximum ratings	Unit
Power supply voltage	V_{DD} to V_{SS}	7.0	V
Input voltage	V_{IN}	V_{SS} to V_{DD}	V
Output voltage	V_{OUT}	V_{SS} to V_{DD}	V
Differential input voltage	V_{IND}	±5.5	V
Output pin current	I_{SOURCE}	30	mA
	I_{SINK}		
Power dissipation	P_D	250	mW
Operating temperature	Topr	−40 to +85	°C
Storage temperature	Tstg	−55 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Power Supply Voltage Range

Table 3

Item	Symbol	Range	Unit
Operating power supply voltage range	V_{DD}	1.2 to 5.5	V

■ Electrical Characteristics

1. V_{DD}=3.0 V

Table 4

DC characteristics (V_{DD}=3.0 V) ($V_{\overline{SHDN}}$=V_{DD}, Ta=25°C unless overwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
Power supply current	I_{DD}	V_{CMR}=V_{OUT}=1.5 V	—	170	235	μA	**Figure 11**
Power supply current in shutdown mode	I_{DDSHDN}	$V_{\overline{SHDN}}$=0 V	—	0.1	1	μA	**Figure 12**
Input offset voltage	V_{IO}	V_{CMR}=1.5 V	−10	±5	+10	mV	**Figure 7**
Input offset current	I_{IO}	—	—	1	—	pA	—
Input bias current	I_{BIAS}	—	—	1	—	pA	—
Common-mode input voltage	V_{CMR}	—	0	—	3	V	—
Voltage gain(open loop)	A_{VOL}	V_{SS}+0.1 V ≤V_{OUT} ≤V_{DD}−0.1 V V_{CMR}=1.5 V, R_L=1 MΩ	80	90	—	dB	**Figure 16**
Maximum output swing voltage	V_{OH}	R_L=100 kΩ	2.99	—	—	V	**Figure 9**
	V_{OL}	R_L=100 kΩ	—	—	0.01		**Figure 10**
Output voltage in shutdown mode	V_{OSHDN}	$V_{\overline{SHDN}}$=0 V, R_L=100 kΩ	—	—	0.01	V	—
Common-mode input signal rejection ratio	CMRR	V_{SS} ≤ V_{CMR} ≤ V_{DD}	45	55	—	dB	**Figure 8**
Power supply voltage rejection ratio	PSRR	V_{DD}=1.2 to 5.5 V	50	66	—	dB	**Figure 6**
Source current	I_{SOURCE}	V_{OUT}=V_{DD}−0.1 V	4.9	5.4	—	mA	**Figure 13**
Sink current	I_{SINK}	V_{OUT}=V_{SS}+0.1 V	1.6	1.7	—	mA	**Figure 14**
		V_{OUT}=V_{DD}	14.5	18	—		
Shutdown pin input voltage	$V_{\overline{SHDN}}$	During operation	1.8	—	3	V	—
		During shutdown	0	—	0.55		

Table 5

AC characteristics (V_{DD}=3.0 V) ($V_{\overline{SHDN}}$=V_{DD}, Ta=25°C unless overwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Slew rate	SR	R_L=1.0 MΩ, C_L=15 pF (Refer to **Figure 15**)	—	1	—	V/μs
Gain-bandwidth product	GBP	Gain=1, C_L=0 pF	—	550	—	kHz
Maximum load capacitance	C_L	Gain=1	—	25	—	pF

2. V_{DD}=1.8 V

Table 6

DC characteristics (V_{DD}=1.8 V) ($V_{\overline{SHDN}}$=V_{DD}, Ta=25°C unless overwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
Power supply current	I_{DD}	V_{CMR}=V_{OUT}=0.9 V	—	150	200	μA	**Figure 11**
Power supply current in shutdown mode	I_{DDSHDN}	$V_{\overline{SHDN}}$=0 V	—	0.1	1	μA	**Figure 12**
Input offset voltage	V_{IO}	V_{CMR}=0.9 V	−10	±5	+10	mV	**Figure 7**
Input offset current	I_{IO}	—	—	1	—	pA	—
Input bias current	I_{BIAS}	—	—	1	—	pA	—
Common-mode input voltage	V_{CMR}	—	0	—	1.8	V	—
Voltage gain(open loop)	A_{VOL}	V_{SS}+0.1 V ≤V_{OUT} ≤V_{DD}−0.1 V V_{CMR}=0.9 V, R_L=1 MΩ	80	90	—	dB	**Figure 16**
Maximum output swing voltage	V_{OH}	R_L=100 kΩ	1.79	—	—	V	**Figure 9**
	V_{OL}	R_L=100 kΩ	—	—	0.01		**Figure 10**
Output voltage in shutdown mode	V_{OSHDN}	$V_{\overline{SHDN}}$=0 V, R_L=100 kΩ	—	—	0.01	V	—
Common-mode input signal rejection ratio	CMRR	V_{SS} ≤ V_{CMR} ≤ V_{DD}	35	45	—	dB	**Figure 8**
Power supply voltage rejection ratio	PSRR	V_{DD}=1.2 to 5.5 V	50	66	—	dB	**Figure 6**
Source current	I_{SOURCE}	V_{OUT}=V_{DD}−0.1 V	2.6	3	—	mA	**Figure 13**
		V_{OUT}=V_{SS}	12	16	—		
Sink current	I_{SINK}	V_{OUT}=V_{SS}+0.1 V	0.85	1	—	mA	**Figure 14**
		V_{OUT}=V_{DD}	4.2	6	—		
Shutdown pin input voltage	$V_{\overline{SHDN}}$	During operation	1.5	—	1.8	V	—
		During shutdown	0	—	0.55		

Table 7

AC characteristics (V_{DD}=1.8 V) ($V_{\overline{SHDN}}$=V_{DD}, Ta=25°C unless overwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Slew rate	SR	R_L=1.0 MΩ, C_L=15 pF (Refer to **Figure 15**)	—	7	—	V/μs
Gain-bandwidth product	GBP	Gain=1, C_L=0 pF	—	550	—	kHz
Maximum load capacitance	C_L	Gain=1	—	25	—	pF

3. V_{DD}=1.2 V

Table 8

DC characteristics (V_{DD}=1.2 V) ($V_{\overline{SHDN}}$=V_{DD}, Ta=25°C unless overwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
Power supply current	I_{DD}	V_{CMR}=V_{OUT}=0.6 V	—	135	185	μA	**Figure 11**
Power supply current in shutdown mode	I_{DDSHDN}	$V_{\overline{SHDN}}$=0 V	—	0.1	1	μA	**Figure 12**
Input offset voltage	V_{IO}	V_{CMR}=0.6 V	−10	±5	+10	mV	**Figure 7**
Input offset current	I_{IO}	—	—	1	—	pA	—
Input bias current	I_{BIAS}	—	—	1	—	pA	—
Common-mode input voltage	V_{CMR}	—	0	—	1.2	V	—
Voltage gain(open loop)	A_{VOL}	V_{SS}+0.1 V ≤V_{OUT} ≤V_{DD}−0.1 V V_{CMR}=0.6 V, R_L=1 MΩ	70	80	—	dB	**Figure 16**
Maximum output swing voltage	V_{OH}	R_L=100 kΩ	1.19	—	—	V	**Figure 9**
	V_{OL}	R_L=100 kΩ	—	—	0.01		**Figure 10**
Output voltage in shutdown mode	V_{OSHDN}	$V_{\overline{SHDN}}$=0 V, R_L=100 kΩ	—	—	0.01	V	—
Common-mode input signal rejection ratio	CMRR	V_{SS} ≤ V_{CMR} ≤ V_{DD}	25	35	—	dB	**Figure 8**
		V_{SS} ≤ V_{CMR} ≤ V_{DD}−0.3 V	40	50	—		
Power supply voltage rejection ratio	PSRR	V_{DD}=1.2 ~ 5.5 V	50	66	—	dB	**Figure 6**
Source current	I_{SOURCE}	V_{OUT}=V_{DD}−0.1 V	1	1.5	—	mA	**Figure 13**
		V_{OUT}=V_{SS}	2.1	4.5	—		
Sink current	I_{SINK}	V_{OUT}=V_{SS}+0.1 V	0.4	0.55	—	mA	**Figure 14**
		V_{OUT}=V_{DD}	1	1.8	—		
Shutdown pin input voltage	$V_{\overline{SHDN}}$	During operation	1.14	—	1.2	V	—
		During shutdown	0	—	0.3		

Table 9

AC characteristics (V_{DD}=1.2 V) ($V_{\overline{SHDN}}$=V_{DD}, Ta=25°C unless overwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Slew rate (Rise)	SR	R_L=1.0 MΩ, C_L=15 pF (Refer to **Figure 15**)	—	1	—	V/μs
Gain-bandwidth product	GBP	Gain=1, C_L=0 pF	—	550	—	kHz
Maximum load capacitance	C_L	Gain=1	—	25	—	pF

■ Measurement Circuits

1. Power supply voltage rejection ratio

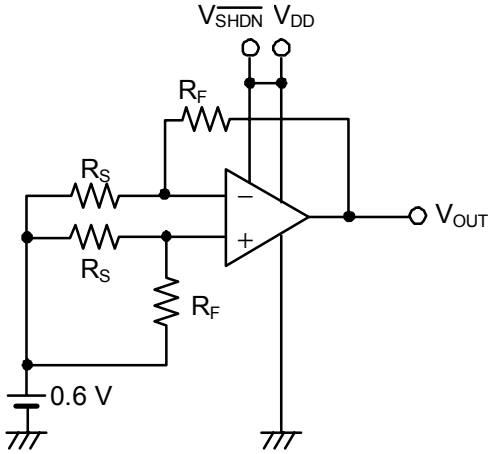


Figure 6

- **Power supply voltage rejection ratio (PSRR)**
  The power supply voltage rejection ratio (PSRR) can be calculated by the following formula, with the value of V_{OUT} measured at each V_{DD}.

  Measurement conditions :
  When V_{DD} = 1.2 V: $V_{DD} = V_{DD1}$, $V_{OUT} = V_{OUT1}$
  When V_{DD} = 5.5 V: $V_{DD} = V_{DD2}$, $V_{OUT} = V_{OUT2}$

$$PSRR = 20\log\left(\left|\frac{V_{DD1} - V_{DD2}}{V_{OUT1} - V_{OUT2}}\right| \times \frac{R_F + R_S}{R_S}\right)$$

2. Input offset voltage

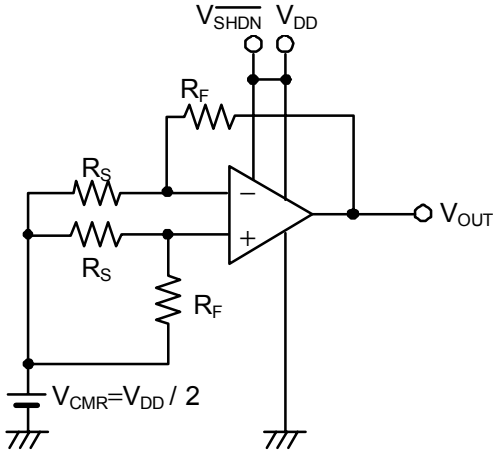


Figure 7

- **Input Offset voltage (V_{IO})**

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

3. Common-mode input signal rejection ratio, common-mode input voltage

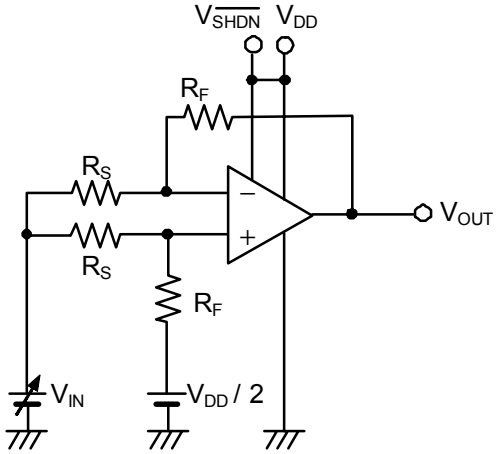


Figure 8

- **Common-mode input signal rejection ratio (CMRR)**
  The common-mode input signal rejection ratio (CMRR) can be calculated by the following formula, with the value of V_{OUT} measured at each V_{IN}.

  Measurement conditions :
  When $V_{IN} = V_{CMR}$ (max.): $V_{IN} = V_{IN1}$, $V_{OUT} = V_{OUT1}$
  When $V_{IN} = V_{CMR}$ (min.): $V_{IN} = V_{IN2}$, $V_{OUT} = V_{OUT2}$

$$CMRR = 20\log\left(\left|\frac{V_{IN1} - V_{IN2}}{V_{OUT1} - V_{OUT2}}\right| \times \frac{(R_F + R_S)}{R_S}\right)$$

- **Common-mode input voltage (V_{CMR})**
  The common-mode input voltage is the range of input voltage within which V_{OUT} satisfies the common-mode input signal rejection ratio specification when V_{IN} is varied.

4. Maximum output swing voltage

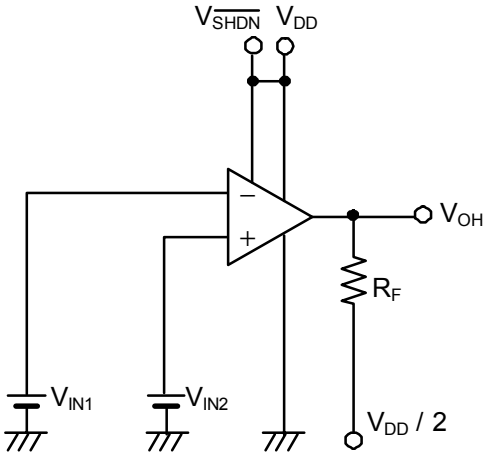


Figure 9

- **Maximum output swing voltage (V_{OH})**

Measurement conditions :

$$V_{IN1} = \frac{V_{DD}}{2} - 0.1V$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.1V$$

R_L=100 kΩ

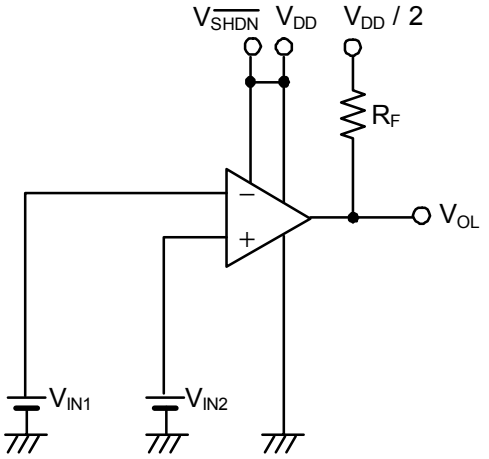


Figure 10

- **Maximum output swing voltage (V_{OL})**

Measurement conditions :

$$V_{IN1} = \frac{V_{DD}}{2} + 0.1V$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.1V$$

R_L=100 kΩ

5. Power supply current

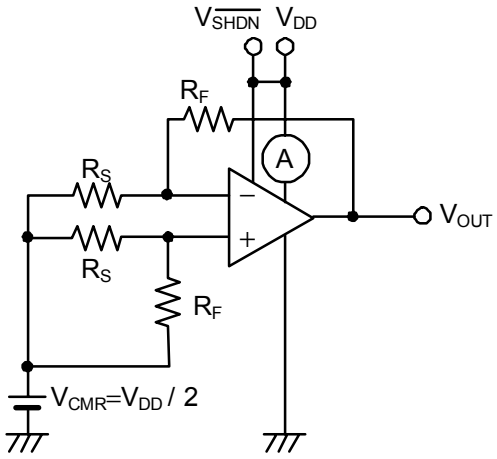


Figure 11

- **Power supply current (I_{DD})**

6. Power supply current in shutdown mode

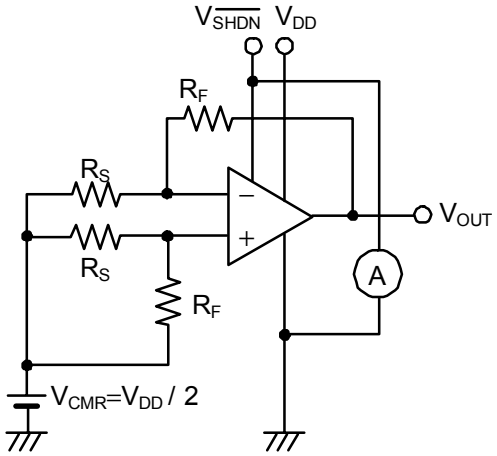


Figure 12

- **Power supply current** in shutdown mode **(I_{DDSHDN})**

7. Source current

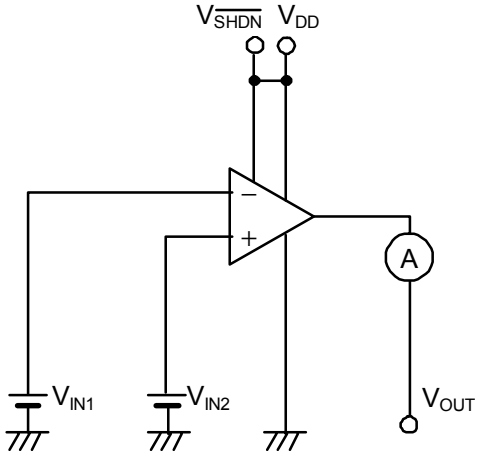


Figure 13

- **Source current (I_{SOURCE})**

  Measurement conditions :
  $V_{OUT}=V_{DD}-0.1$ V or $V_{OUT}=0$ V

$$V_{IN1}=\frac{V_{DD}}{2}-0.1V$$

$$V_{IN2}=\frac{V_{DD}}{2}+0.1V$$

8. Sink current

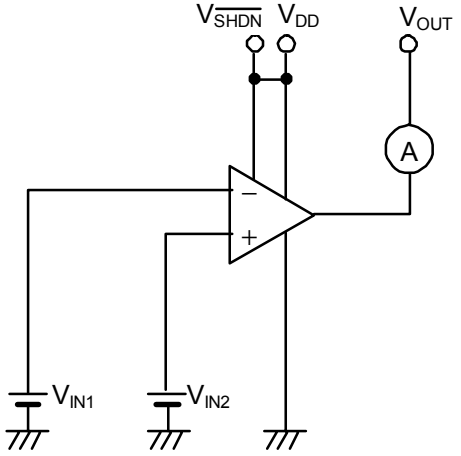


Figure 14

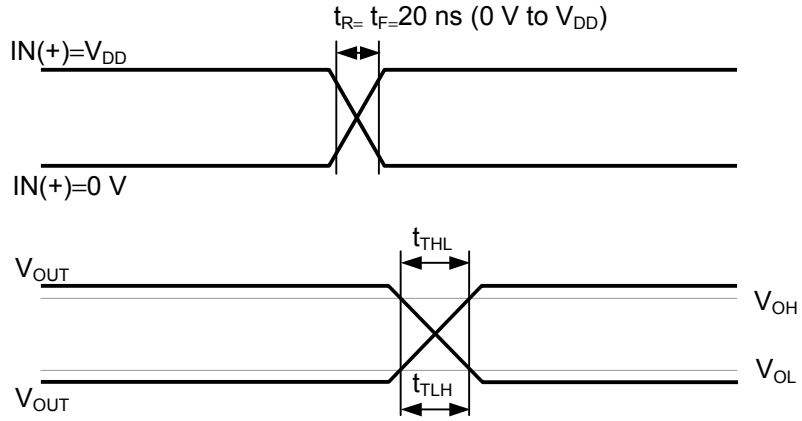
- **Sink current (I_{SINK})**

  Measurement conditions :
  $V_{OUT}=V_{DD}-0.1$ V or $V_{OUT}=0$ V

$$V_{IN1}=\frac{V_{DD}}{2}+0.1V$$

$$V_{IN2}=\frac{V_{DD}}{2}-0.1V$$

9. Slew rate (SR)



When falling

$$SR = \frac{V_{OH} - V_{OL}}{t_{THL}}$$

When rising

$$SR = \frac{V_{OH} - V_{OL}}{t_{TLH}}$$

Figure 15

	When V_{DD}=3.0 V	When V_{DD}=1.8 V	When V_{DD}=1.2 V
V_{OH}	2.7 V	1.62 V	1.08 V
V_{OL}	0.3 V	0.18 V	0.12 V

10. Voltage gain (open loop)

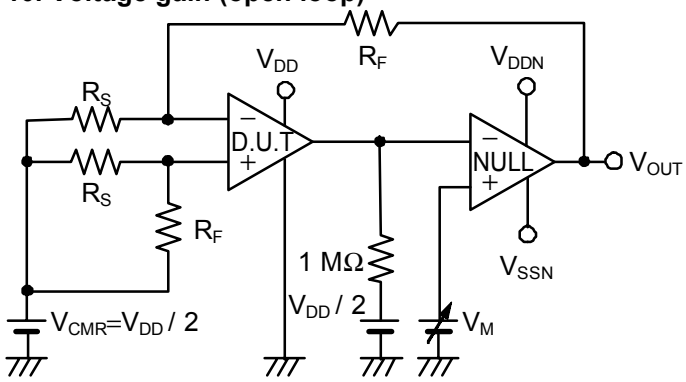


Figure 16

- **Voltage gain (open loop) (A_{VOL})**

  The voltage gain (open loop) (A_{VOL}) can be calculated by the following formula, with the value of V_{OUT} measured at each V_M.

  Measurement conditions :
  When $V_M = V_{DD} - 0.1$ V: $V_M = V_{M1}$, $V_{OUT} = V_{OUT1}$
  When $V_M = 0.1$ V: $V_M = V_{M2}$, $V_{OUT} = V_{OUT2}$

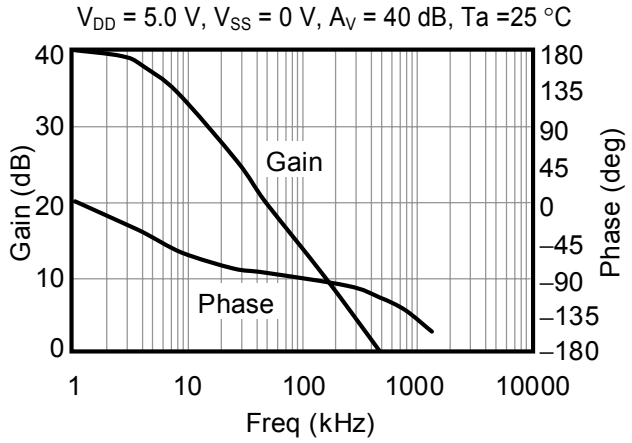
$$A_{VOL} = 20\log\left(\left|\frac{V_{M1} - V_{M2}}{V_{OUT1} - V_{OUT2}}\right| \times \frac{(R_F + R_S)}{R_S}\right)$$

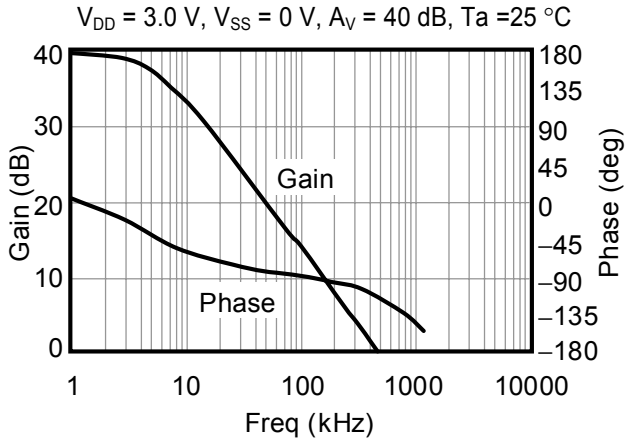
■ Precaution

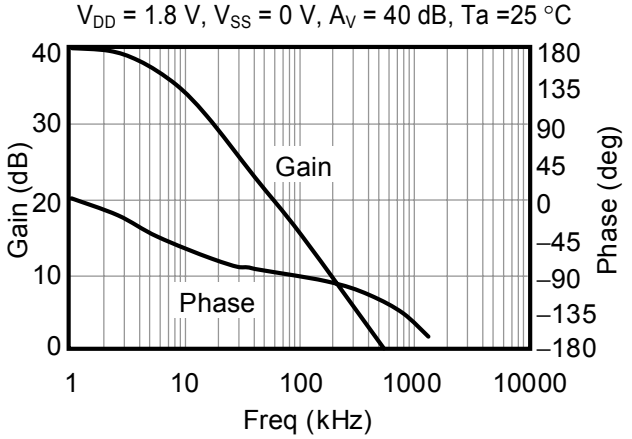
- Be aware that, as in the majority of other operational amplifiers, the capacitative load reduces the phase margin, which may cause ringing, overshoot, or inadvertent oscillation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Be sure to use the product with an output current of no more than 30 mA.
- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

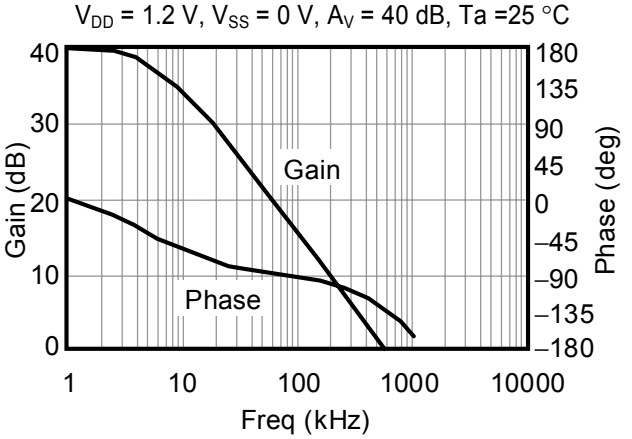
■ Operational Amplifier Characteristics (All Data Indicates Typical Values One Circuit, $V_{\overline{SHDN}}=V_{DD}$)

(1) Voltage gain vs. Frequency

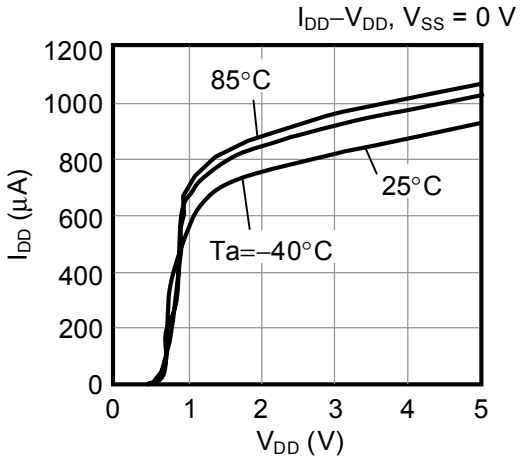








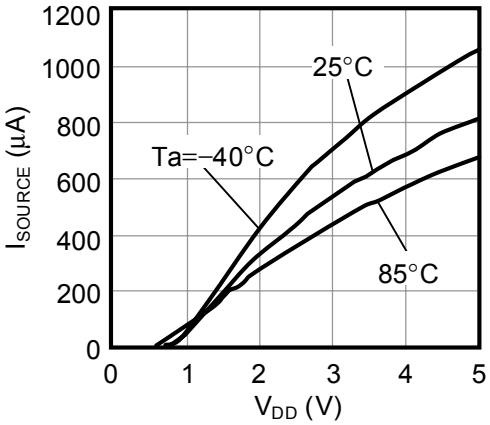
(2) Power supply current vs. Power supply voltage



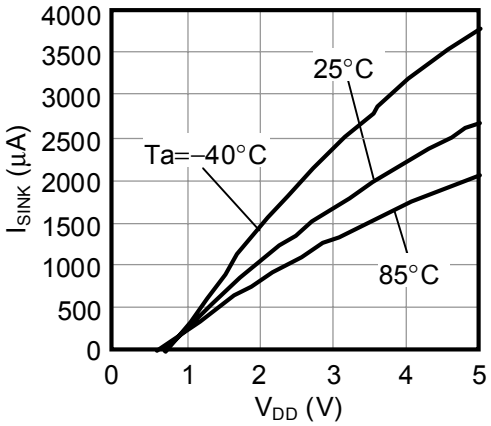
(3) Output current characteristics

1. Power supply voltage

I_{SOURCE} vs. Power supply voltage
$V_{OH} = V_{DD}–0.1$ V, $V_{SS} = 0$ V

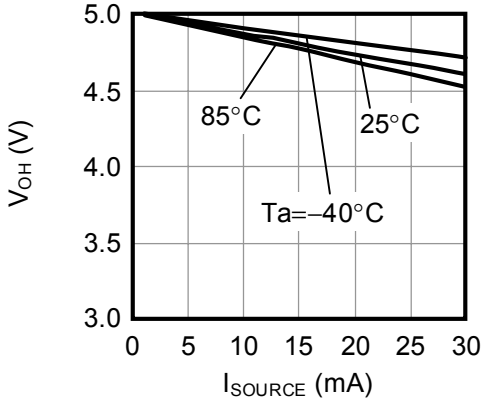


I_{SINK} vs. Power supply voltage
$V_{OL} = 0.1$ V, $V_{SS} = 0$ V

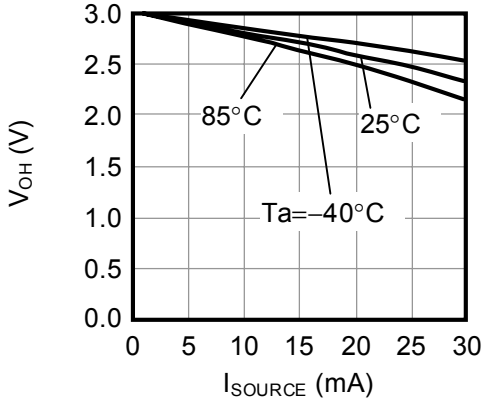


2. Output voltage (V_{OH}) vs. I_{SOURCE}

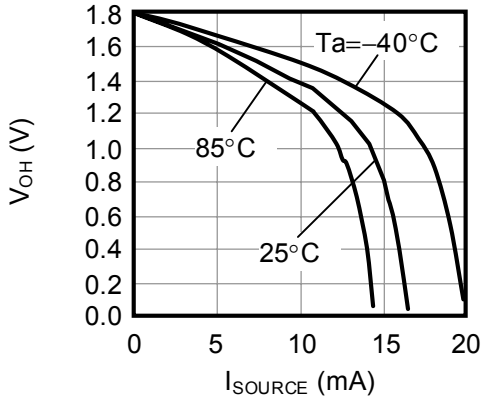
$V_{DD} = 5$ V, $V_{SS} = 0$ V



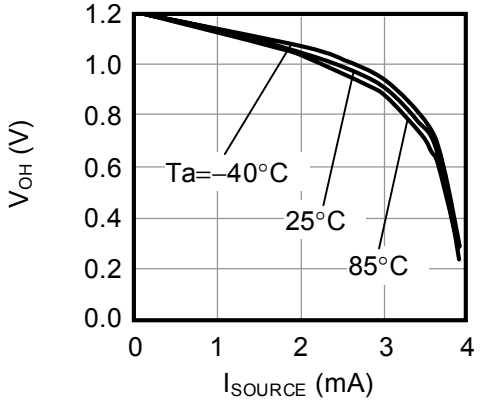
$V_{DD} = 3$ V, $V_{SS} = 0$ V



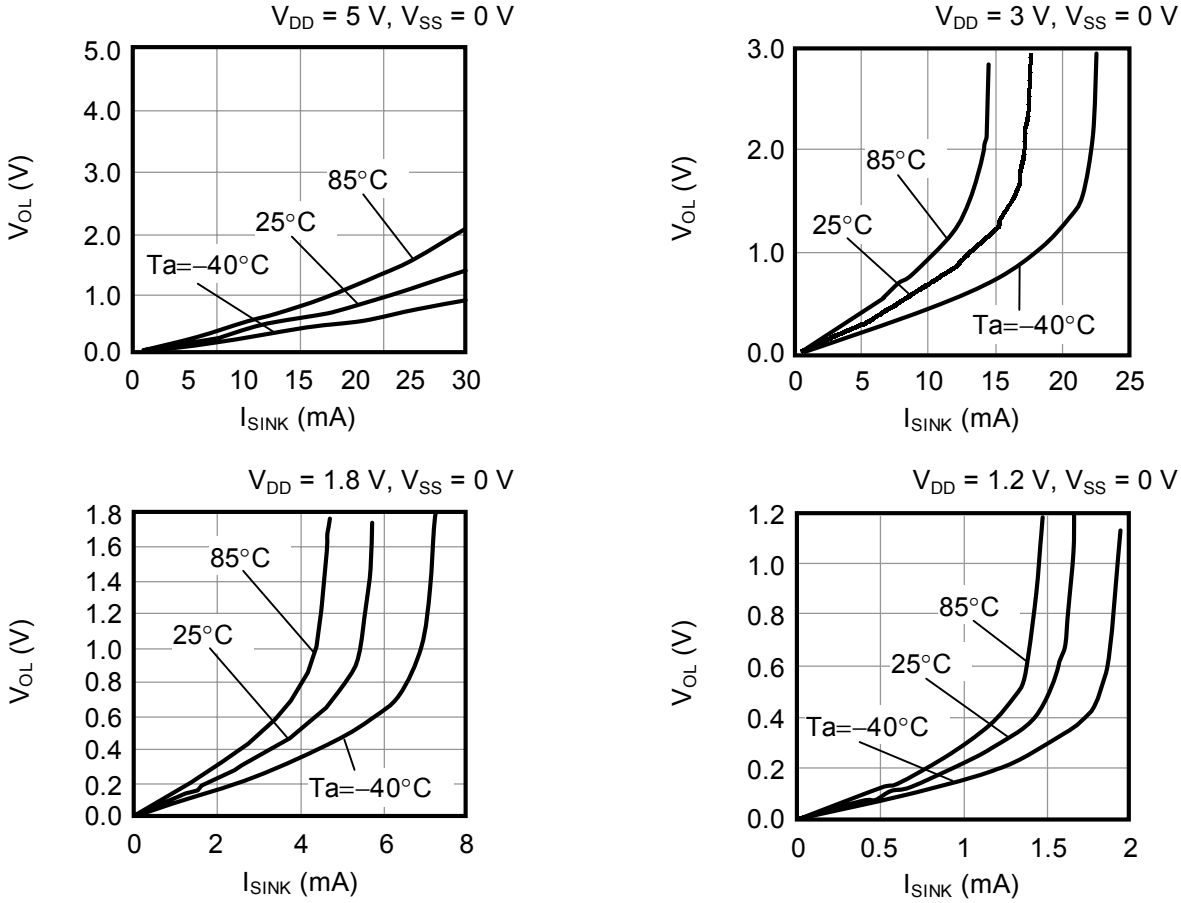
$V_{DD} = 1.8$ V, $V_{SS} = 0$ V

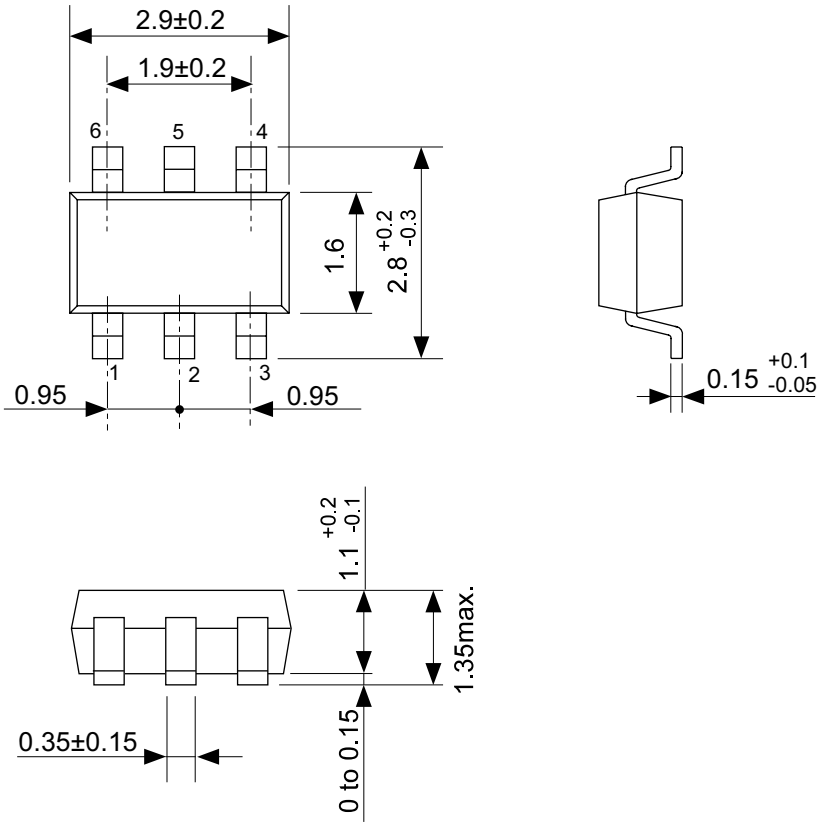


$V_{DD} = 1.2$ V, $V_{SS} = 0$ V



3. Output voltage (V_{OL}) vs. I_{SINK}

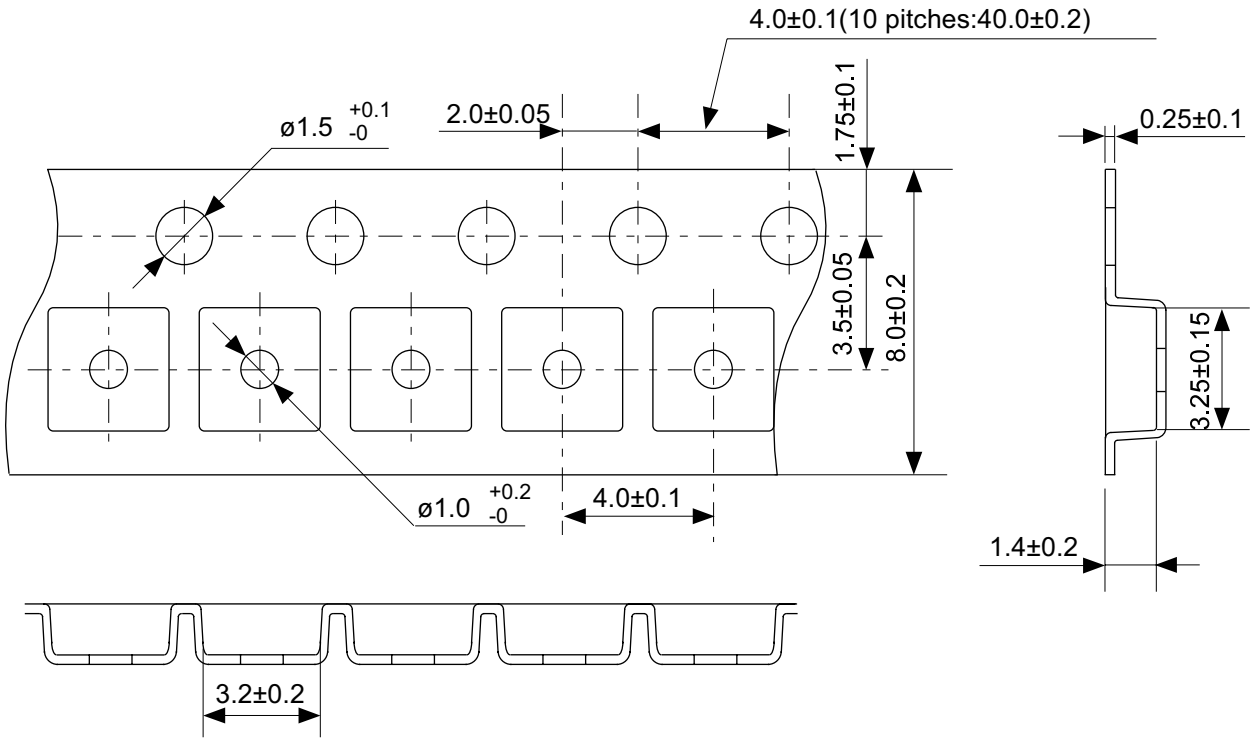


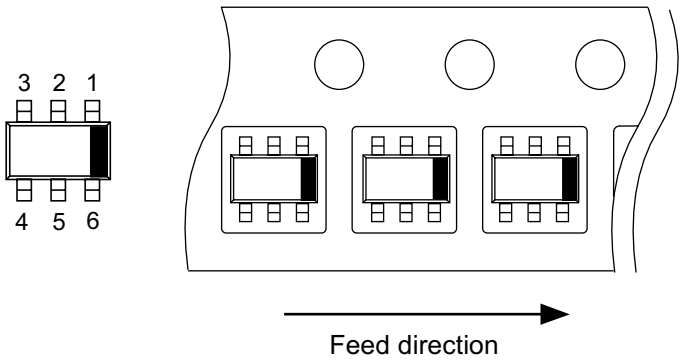


No. MP006-A-P-SD-1.1

TITLE	SOT236-A-PKG Dimensions
No.	MP006-A-P-SD-1.1
SCALE	
UNIT	mm

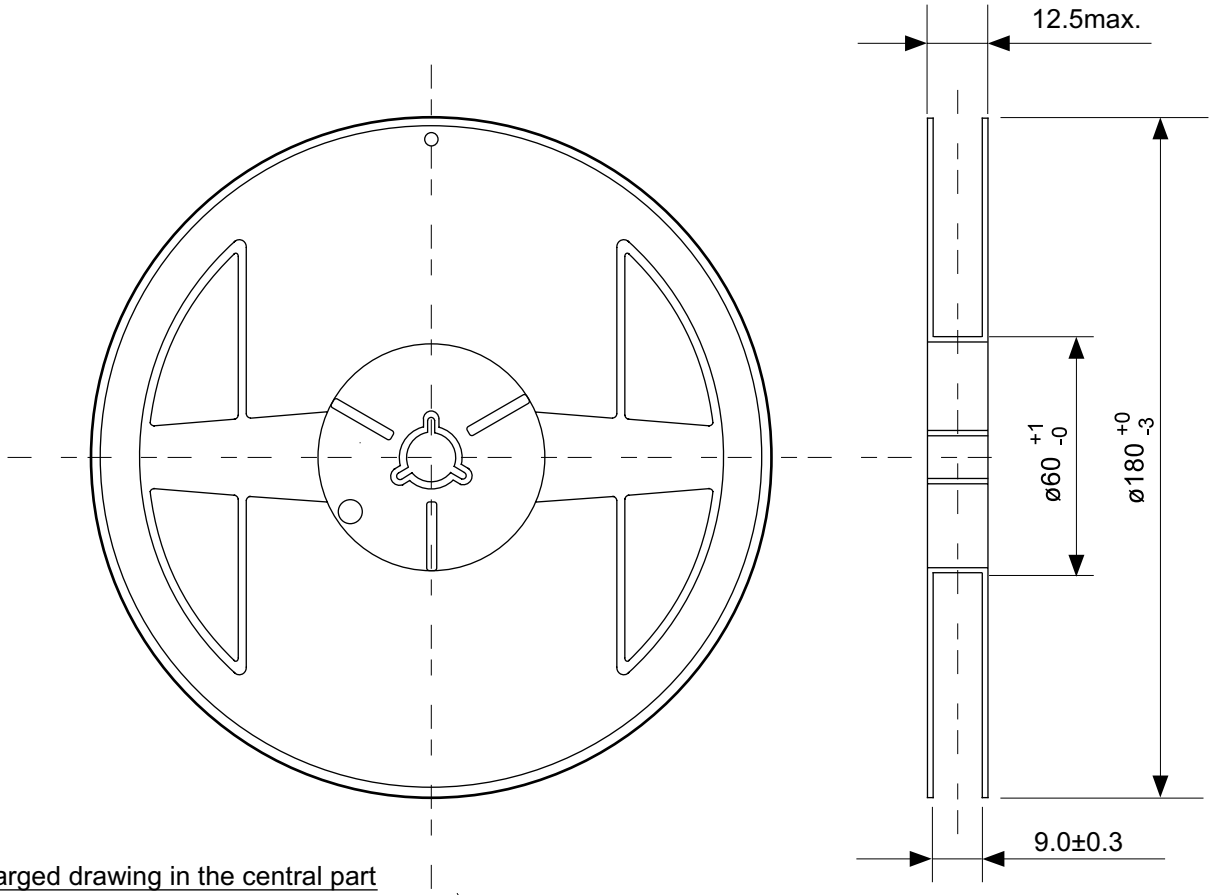
Seiko Instruments Inc.



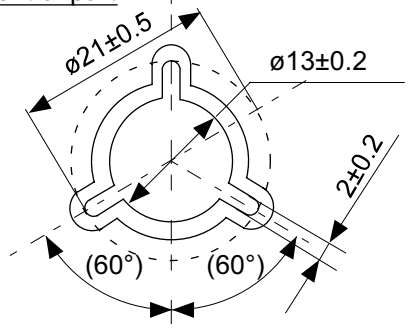


No. MP006-A-C-SD-3.1

TITLE	SOT236-A-Carrier Tape
No.	MP006-A-C-SD-3.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. MP006-A-R-SD-2.1

TITLE	SOT236-A-Reel		
No.	MP006-A-R-SD-2.1		
SCALE		QTY	3,000
UNIT	mm		
Seiko Instruments Inc.			

- The information described herein is subject to change without notice.
- Seiko Instruments Inc. is not responsible for any problems caused by circuits or diagrams described herein whose related industrial properties, patents, or other rights belong to third parties. The application circuit examples explain typical applications of the products, and do not guarantee the success of any specific mass-production design.
- When the products described herein are regulated products subject to the Wassenaar Arrangement or other agreements, they may not be exported without authorization from the appropriate governmental authority.
- Use of the information described herein for other purposes and/or reproduction or copying without the express permission of Seiko Instruments Inc. is strictly prohibited.
- The products described herein cannot be used as part of any device or equipment affecting the human body, such as exercise equipment, medical equipment, security systems, gas equipment, or any apparatus installed in airplanes and other vehicles, without prior written permission of Seiko Instruments Inc.
- Although Seiko Instruments Inc. exerts the greatest possible effort to ensure high quality and reliability, the failure or malfunction of semiconductor products may occur. The user of these products should therefore give thorough consideration to safety design, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue.