Multi-Output, Individual On/Off Control Power-Supply Controller

FEATURES

- Five Output 50-W, Triple Output DC-DC-Controller
- Up to 95% Efficiency
- ±3% Total Regulation (Line, Load and Temperature)
- 4.5-V to 30-V Input Voltage Range
- Two Fixed 1.5-V, 1.8-V, 2.0-V, 2.2-V, 2.5-V, 2.8-V, 3.3-V Outputs
- One Adjustable 1.24-V to 20-V Output
- 3.3-V Reference Output
- 5-V/30-mA Linear Regulator Output
- Individual ON/OFF Control for A and B Outputs
- 300-kHz Low-Noise Fixed Frequency Operation
- High Efficiency Pulse Skipping Mode Operation at Light Load
- Only Three Inductors Required—No Transformer
- LITTLE FOOT® Optimized Output Drivers
- Internal Under Voltage Lockout and Soft-Start
- Minimum Number of External Control Components
- 28-Pin SSOP Package
- Output Overvoltage Protection
- Output Undervoltage Shutdown
- Power-Good Output ($\overline{\text{RESET}}$)

APPLICATIONS

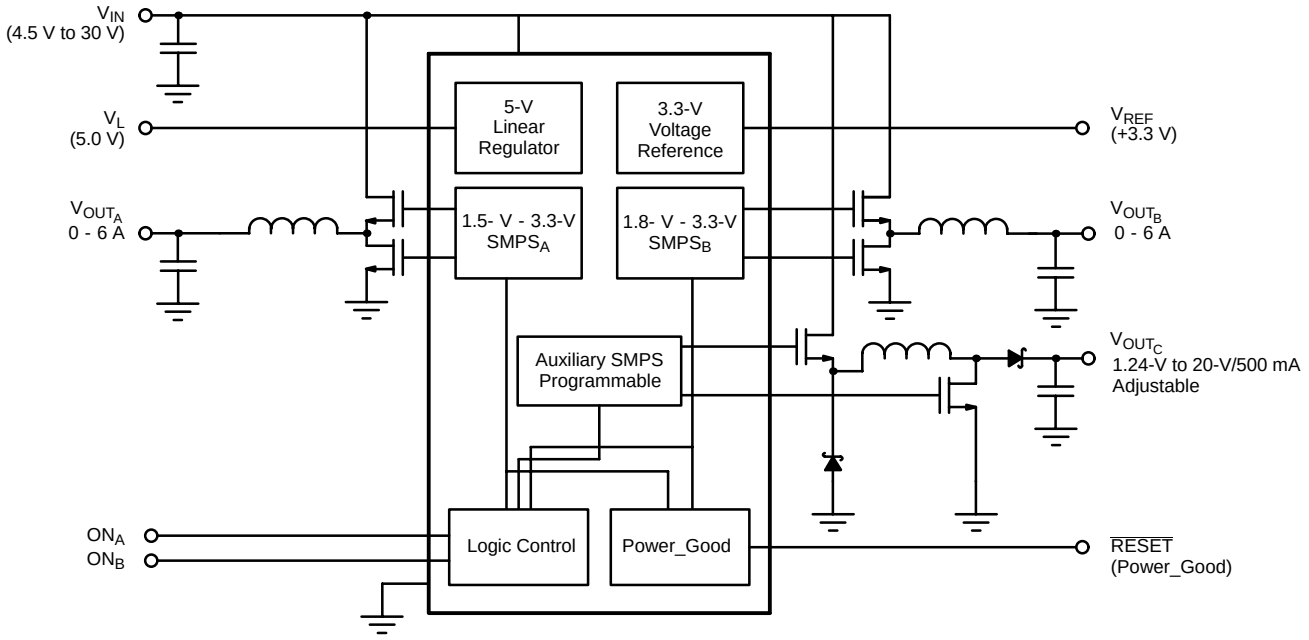
- Notebook and Subnotebook Computers
- PDAs and Mobile Communicators
- Portable Display
- Multimedia Set-Top Box
- Telecommunications Infrastructure
- Network Equipment
- Distributed Power Conversion

DESCRIPTION

The Si9139 is current-mode PWM and PSM converter controller, with two high current, high efficiency synchronous buck controllers and an adjustable buck-boost controller whose output can be set between 1.24 V and 20 V with an external resistor divider. Designed for fixed and portable devices, it offers a total of five power outputs (three tightly regulated dc/dc converter outputs, a precision 3.3-V reference and a 5-V LDO output. Individually controlled power-up sequencing, power-good signal with delay, internal frequency compensation networks and automatic boot-strapping simplify the system by minimizing the number of external components while achieving conversion efficiencies approaching 95%.

The Si9139 is available in a 28-pin SSOP package and specified to operate over the extended commercial (-40°C to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{IN} to GND . . . . . -0.3 to +36 V
P_{GND} to GND . . . . . ±2 V
V_L to GND . . . . . -0.3 to +6.5 V
BST_A, BST_B, BST_C to GND . . . . . -0.3 V to +36 V
V_L Short to GND . . . . . Continuous
LX_A to BST_A; LX_B to BST_B; LX_C to BST_C . . . . . -6.5 V to 0.3 V
Inputs/Outputs to GND
(CS_A, CS_B, CSP, CSN) . . . . . -0.3 V to (V_L +0.3 V)
$\overline{RESET}$, ON_A, ON_B . . . . . -0.3 V to +5.5 V
DL_A, DL_B, DL_C to PGND . . . . . -0.3 V to (V_L +0.3 V)
DH_A to LX_A, DH_B to LX_B,
DH_C to LX_C . . . . . -0.3 V to (BST_x +0.3 V)
Continuous Power Dissipation (T_A = 70°C)[a]
28-Pin SSOP[b] . . . . . 762 mW
Operating Temperature Range . . . . . -40 °C to 85°C
Storage Temperature Range . . . . . -40 °C to 125°C
Lead Temperature (Soldering, 10 Sec.) . . . . . 300°C

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 9.52 mW/°C above 70°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS

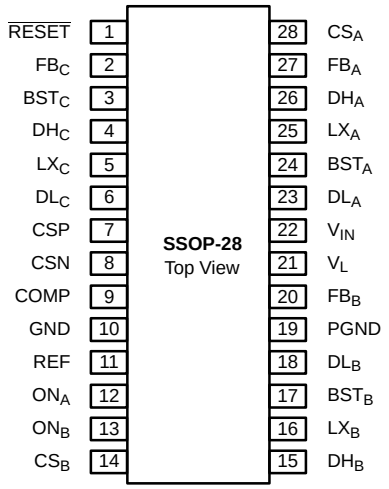
Parameter	Test Conditions V_{IN} = 15 V , I_{VL} = I_{REF} = 0 mA T_A = -40°C to 85°C, All Controllers ON		Limits Min[a]	Typ[b]	Max[a]	Unit
Buck Controller A						
Total Regulation (Line, Load, and Temperature)	V_{IN} = 4.5 V to 30 V, 0 < V_{CS3} - V_{FB3} < 90 mV		-3	0	3	%
Line Regulation	V_{IN} = 6.0 V to 30 V				±0.5	%
	V_{IN} = 4.5 V to 30 V				±1.0	%
Load Regulation	0 < V_{CS3} - V_{FB3} < 90 mV				±0.5	%
Current Limit	V_{CSA} - V_{FBA}	V_{OUT} > 2.5 V	90	125	160	mV
		V_{OUT} < 2.5 V	100		180	mV
Bandwidth	L = 10 µH, C = 330 µF			50		kHz
Phase Margin	R_{SENSE} = 20 mΩ			65		°
Minimum Duty Cycle				7		%
Buck Controller B						
Total Regulation (Line, Load, and Temperature)	V_{IN} = 4.5 V to 30 V, 0 < V_{CS5} - V_{FB5} < 90 mV		-3	0	3	%
Line Regulation	V_{IN} = 6.0 V to 30 V				±0.5	%
	V_{IN} = 4.5 V to 30 V				±1.0	%
Load Regulation	0 < V_{CSB} - V_{FBB} < 90 mV				±0.5	%
Current Limit	V_{CSB} - V_{FBB}	V_{OUT} > 2.5 V	90	125	160	mV
		V_{OUT} < 2.5 V	100		180	mV
Bandwidth	L = 10 µH, C = 330 µF			50		kHz
Phase Margin	R_{SENSE} = 20 mΩ			65		°
Minimum Duty Cycle				7		%
Auxiliary Controller C						
Total Regulation (Line, Load, and Temperature) Output Voltage Set to 12 V	V_{IN} = 4.5 V to 30 V, 0 < V_{CSP} - V_{CSN} < 300 mV R_5 = 26.4 kΩ, R_6 = 10 kΩ (See Figure 1)		-5	0	5	%
Line Regulation	V_{IN} = 6.0 V to 30 V				±0.5	%
	V_{IN} = 4.5 V to 30 V				±1.0	%
Load Regulation	0 < V_{CSP} - V_{FBN} < 300 mV				±0.5	%
Current Limit	V_{CSP} - V_{CSN}		280	360	450	mV
Bandwidth	L = 10 µH, C = 100 µF			10		kHz
Phase Margin	R_{SENSE} = 100 mΩ, C_{comp} = 120 pF			65		°
Current-Sense Common Mode Voltage Range			0.0		2.1	V
Feedback Input Voltage Range			0.0		2.1	V
Minimum Duty Cycle				7		%
Maximum Duty Cycle	V_{IN} = 5 V			85		%

SPECIFICATIONS

Parameter	Test Conditions V_{IN} = 15 V , I_{VL} = I_{REF} = 0 mA T_A = -40°C to 85°C, All Controllers ON	Limits			Unit
		Min[a]	Typ[b]	Max[a]	
Internal 5-V Regulator					
V_L Output Current (Internal and External)			30	60	mA
V_L Output	All Controllers OFF, V_{IN} >5.5 V, 0 <I_L <30 mA	4.7		5.5	V
V_L Fault Lockout Voltage	V_L Falling Edge	3.6		4.2	
V_L Fault Lockout Hysteresis			75		mV
Reference					
REF Output		3.24	3.3	3.36	V
REF Load Regulation	0 to 1 mA		25	60	mV
Auxiliary Feedback Voltage	FB_C Pin	1.20	1.24	1.28	V
Supply Current					
Supply Current – Shutdown	All Converters OFF, No Load		25	60	µA
Supply Current – Operation	All Controllers ON, No Load, f_{OSC} = 300 kHz		1100	1800	
Oscillator					
Oscillator Frequency		270	300	330	kHz
Maximum Duty Cycle		92	95		%
Fault Detection $SMPS_A$ and $SMPS_B$ Outputs					
Overvoltage Trip Threshold	With Respect To Unloaded Output Voltage	6	10	14	%
Overvoltage-Fault Propagation Delay	CS_A or CS_B Driven 2% Above Overvoltage Trip Threshold		1.5		µs
Output Undervoltage Threshold	With Respect to Unloaded Output Voltage	-40	-30	-20	%
Output Undervoltage Lockout Time	From each SMPS Enabled	16	20	24	ms
RESET					
$\overline{\text{RESET}}$ Start Threshold	With Respect To Unloaded Output Voltage Rising Edge		-5.5		%
$\overline{\text{RESET}}$ Propagation Delay (Falling)	Falling Edge, FB_A or FB_B Driven 2% Above Overvoltage or 2% Below Undervoltage Lockout Thresholds		1.5		µs
$\overline{\text{RESET}}$ Delay Time (Rising)	With Respect to 2nd SMPS Lockout Time Done	92	107	122	ms
Inputs and Outputs					
Feedback Input Leakage Current	FB_C = 1.24 V			1	µA
Input Leakage Current	ON_A, ON_B, V_{IN} = 0 V or V_L			±1	
Gate Driver Sink/Source Current (Buck)	DL_A, DH_A, DL_B, DH_B Forced to 2 V		1		A
Gate Driver On-Resistance (Buck)	High or Low		2	7	Ω
Gate Driver Sink/Source Current (Auxiliary)	DH_C, DL_C Forced to 2 V		0.2		A
Gate Driver On-Resistance (Auxiliary)	High or Low			15	Ω
$\overline{\text{RESET}}$ Output Low Voltage	$\overline{\text{RESET}}$, I_{SINK} = 4 mA			0.4	V
$\overline{\text{RESET}}$ Output High Leakage	$\overline{\text{RESET}}$ = 5 V			1	µA
ON_A, ON_B					
Logic Low	V_{IL}			0.8	V
Logic High	V_{IH}	2.4			

Notes
a. The algebraic convention is used whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing, and are measured at T_A = 25°C.

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Symbol	Description
1	$\overline{\text{RESET}}$	Open drain NMOS output active-low timed reset output. $\overline{\text{RESET}}$ swings GND to V_L. Goes high after a fixed 32,000 clock cycle delay following proper power-up of all supply outputs indicating Power_Good.
2	FB_C	Feedback for Auxiliary controller C. Normally connected to an external resistor divider used to set the Auxiliary output voltage.
3	BST_C	Boost capacitor connection for Auxiliary SMPS controller C
4	DH_C	Gate-drive output for Auxiliary SMPS controller C high-side MOSFET
5	LX_C	Inductor connection for Auxiliary SMPS controller C
6	DL_C	Gate-drive output for Auxiliary SMPS controller C low-side MOSFET
7	CSP	Current sense positive input for Auxiliary SMPS controller C
8	CSN	Current sense negative input for Auxiliary SMPS controller C
9	COMP	Auxiliary SMPS controller C compensation connection, if required
10	GND	Analog ground
11	REF	3.3-V internal reference
12	ON_A	Logic High enables the SMPS controller A
13	ON_B	Logic High enables the SMPS controller B and the Auxiliary SMPS controller C adjustable SMPS controllers
14	CS_B	Current sense input for SMPS controller B
15	DH_B	Gate-drive output for SMPS controller B high-side MOSFET
16	LX_B	Inductor connection for SMPS controller B
17	BST_B	Boost capacitor connection for SMPS controller B
18	DL_B	Gate-drive output for SMPS controller B low-side MOSFET
19	PGND	Power ground
20	FB_B	Feedback for SMPS controller B
21	V_L	5-V logic supply voltage for internal circuitry
22	V_{IN}	Input voltage
23	DL_A	Gate-drive output for SMPS controller A low-side MOSFET
24	BST_A	Boost capacitor connection for SMPS controller A
25	LX_A	Gate-drive output for SMPS controller A high-side MOSFET
26	DH_A	Inductor connection for SMPS controller A low-side MOSFET
27	FB_A	Feedback for SMPS controller A
28	CS_A	Current sense input for SMPS controller A

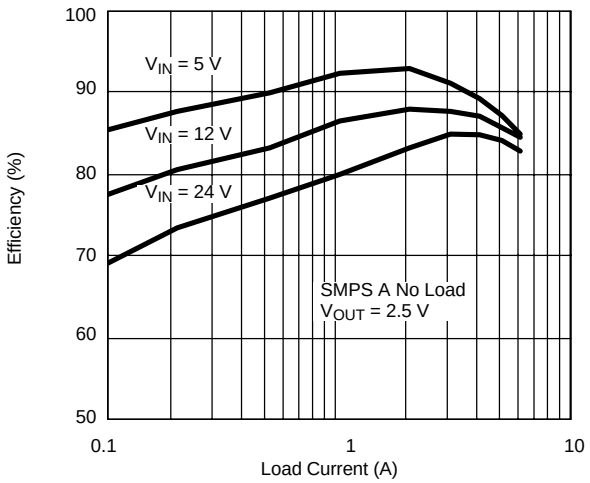
ORDERING INFORMATION

Part Number	Temperature Range	$SMPS_B$, $SMPS_A$ Output Voltages
Si9139DG – 3328	-40 to 85°C	3.3 V, 2.8 V
Si9139DG – 3325		3.3 V, 2.5 V
Si9139DG – 3322		3.3 V, 2.2 V
Si9139DG – 3320		3.3 V, 2.0 V
Si9139DG – 3318		3.3 V, 1.8 V
Si9139DG – 3315		3.3 V, 1.5 V
Si9139DG – 2825		2.8 V, 2.5 V
Si9139DG – 2822		2.8 V, 2.2 V
Si9139DG – 2820		2.8 V, 2.0 V
Si9139DG – 2818		2.8 V, 1.5 V
Si9139DG – 2815		2.8 V, 1.8 V
Si9139DG – 2522		2.5 V, 2.2 V
Si9139DG – 2520		2.5 V, 2.0 V
Si9139DG – 2518		2.5 V, 1.8 V
Si9139DG – 2515		2.5 V, 1.5 V
Si9139DG – 2220		2.2 V, 2.0 V
Si9139DG – 2218		2.2 V, 1.8 V
Si9139DG – 2215		2.2 V, 1.5 V
Si9139DG – 2018		2.0 V, 1.8 V
Si9139DG – 2015		2.0 V, 1.5 V
Si9139DG – 1815		1.8 V, 1.5 V
Si9139DG		Contact factory for other voltages

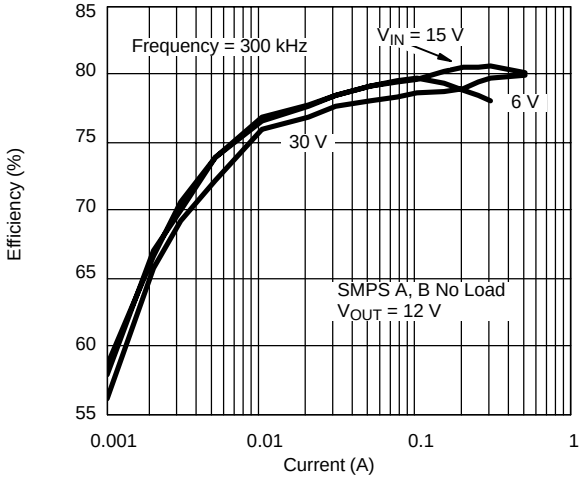
Evaluation Board	Temperature Range	Board Type
Si9139DB	-40 to 85°C	Surface Mount

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Efficiency vs. SMPS B Output Current

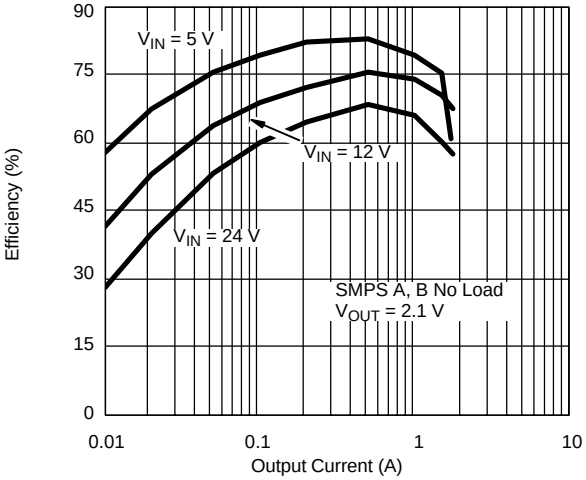


Efficiency vs. Auxiliary SMPS C Output Current (Buck-Boost Configuration)

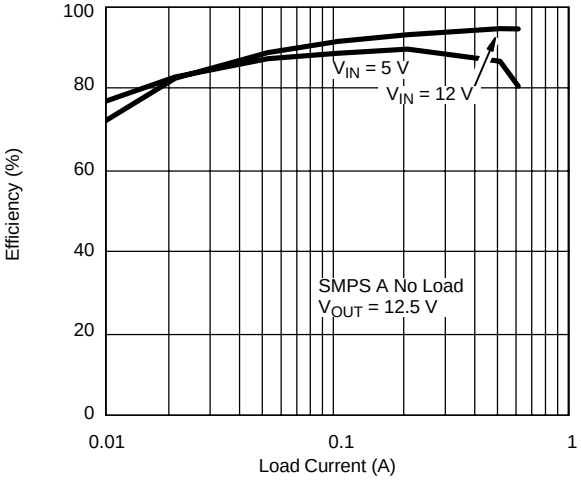


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Efficiency vs. Auxiliary SMPS C Output Current (Buck Configuration)

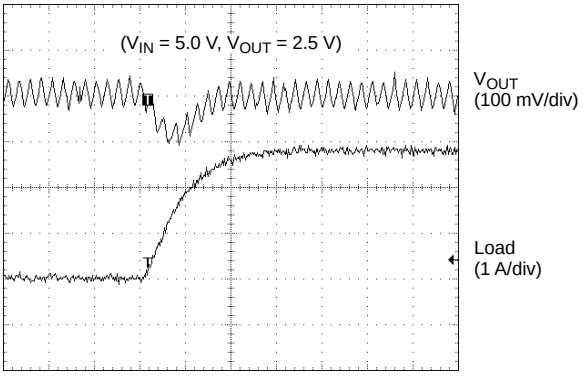


Efficiency vs. SMPS B Output Current

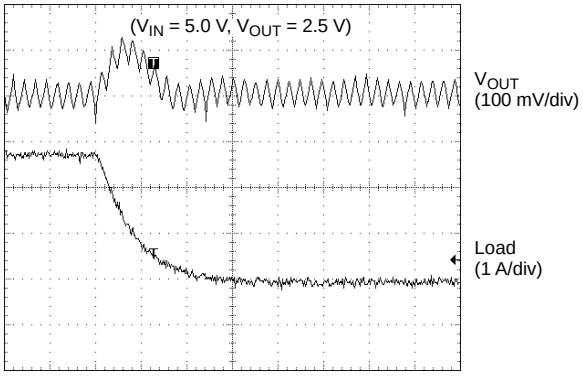


TYPICAL WAVEFORMS

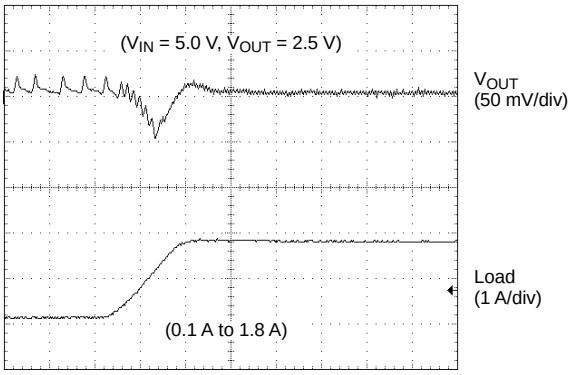
PWM Loading B Converter



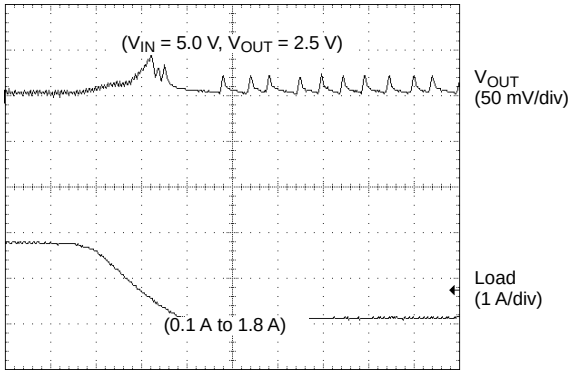
PWM Unloading B Converter



PSM to PWM B Converter

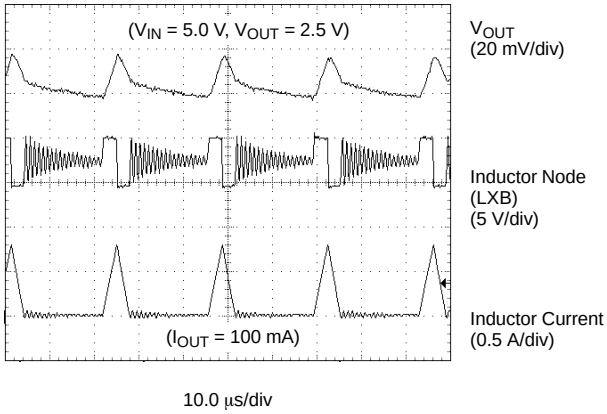


PWM to PSM B Converter

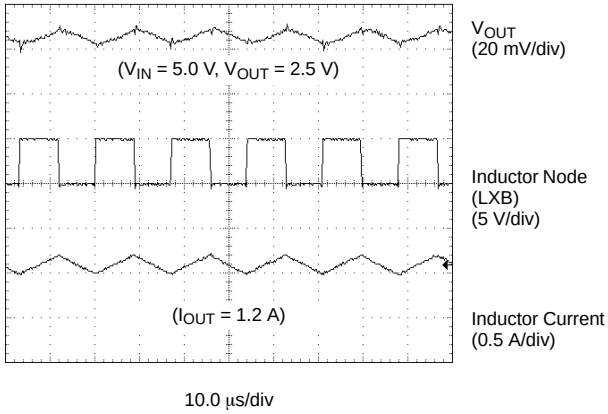


TYPICAL WAVEFORMS

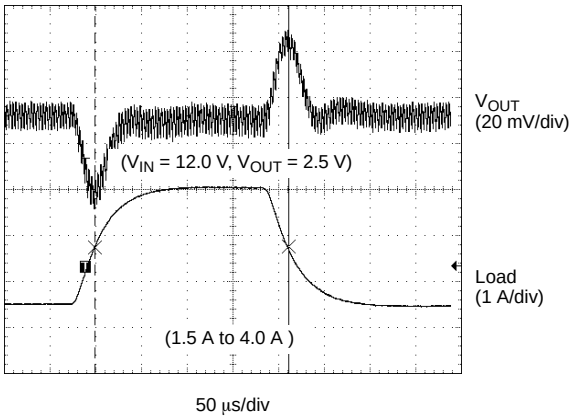
PSM Operation B Converter



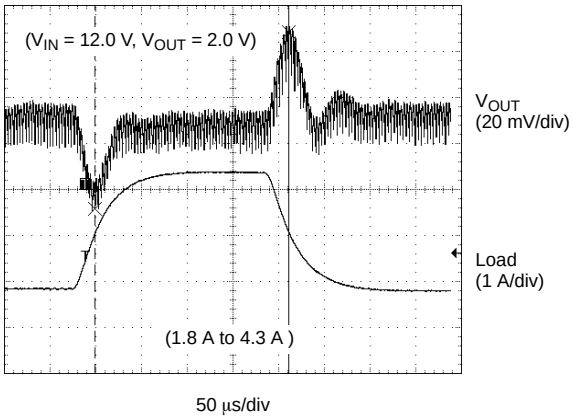
PSM Operation B Converter



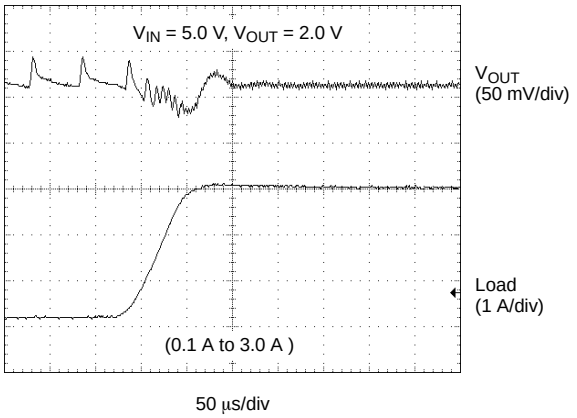
PWM Loading B Converter



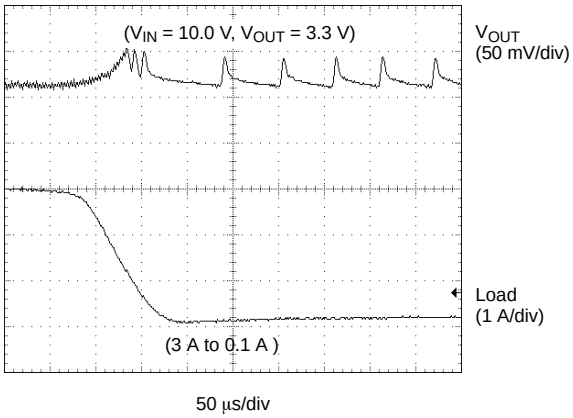
PWM Unloading A Converter



PSM to PWM A Converter

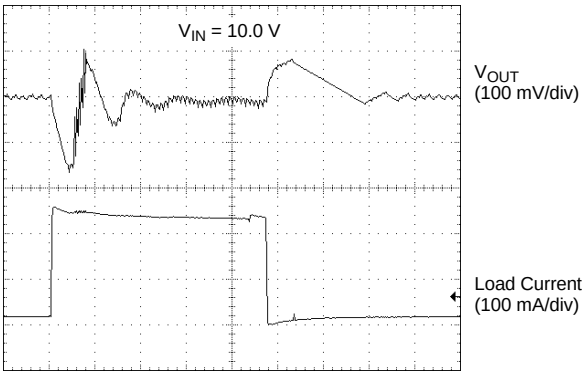


PWM to PSM A Converter

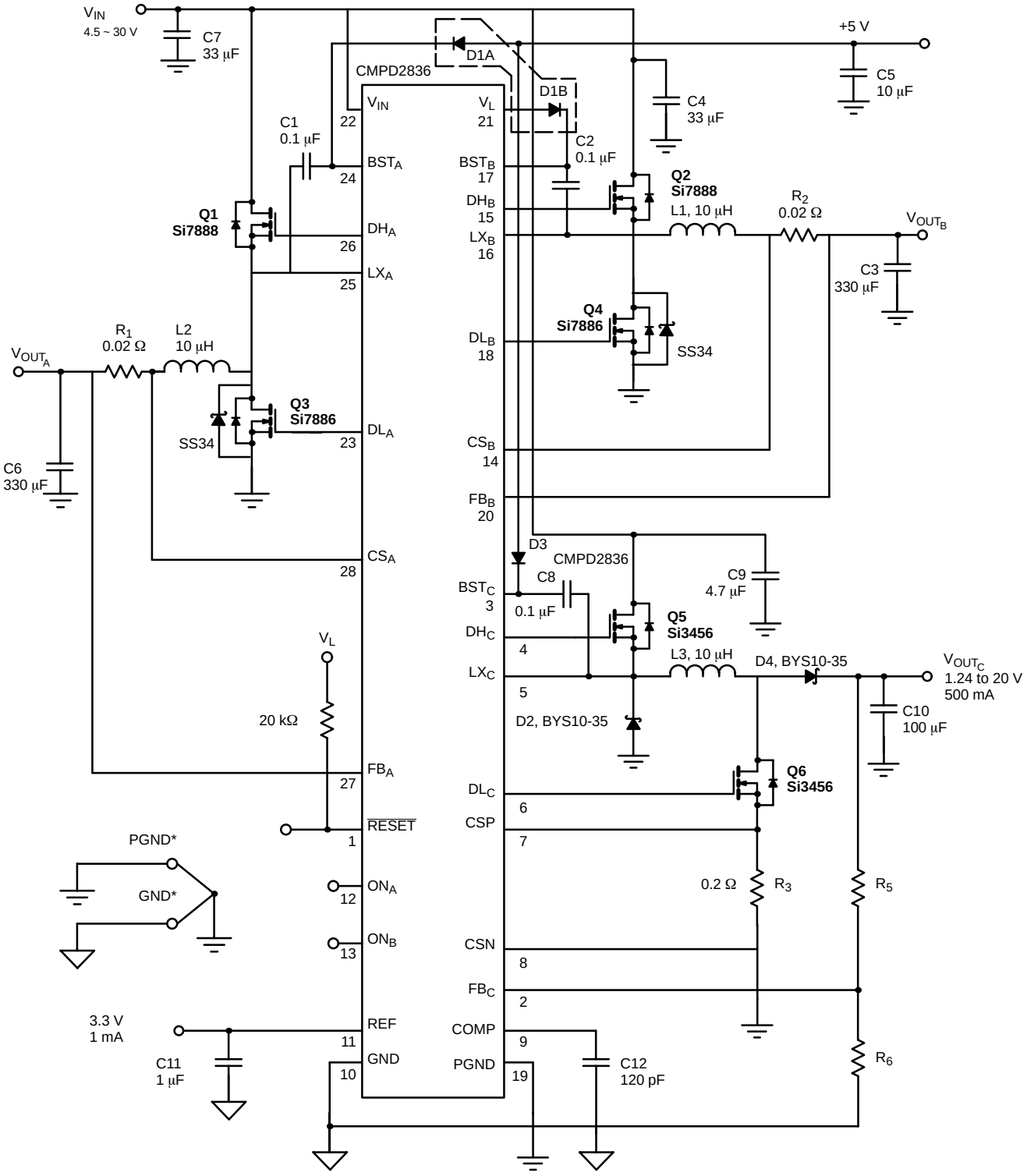


TYPICAL WAVEFORMS

250-mA Transient Auxiliary Converter C
(Buck-Boost Mode—Output Set To 12 V)



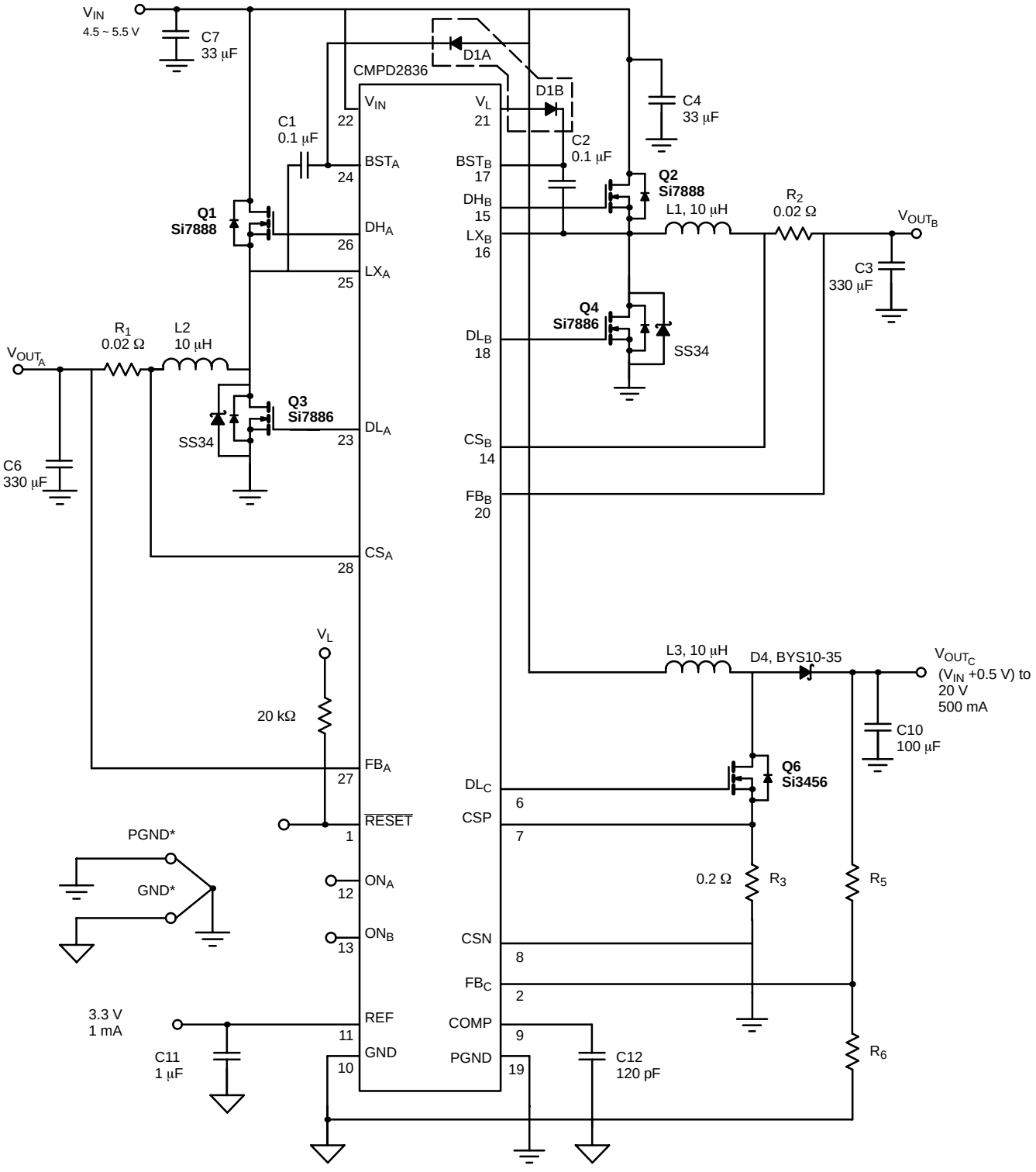
STANDARD APPLICATION CIRCUIT (BUCK-BOOST AUXILIARY)



*PGND and GND planes should be connected to a single point (star) ground.

Figure 1.A

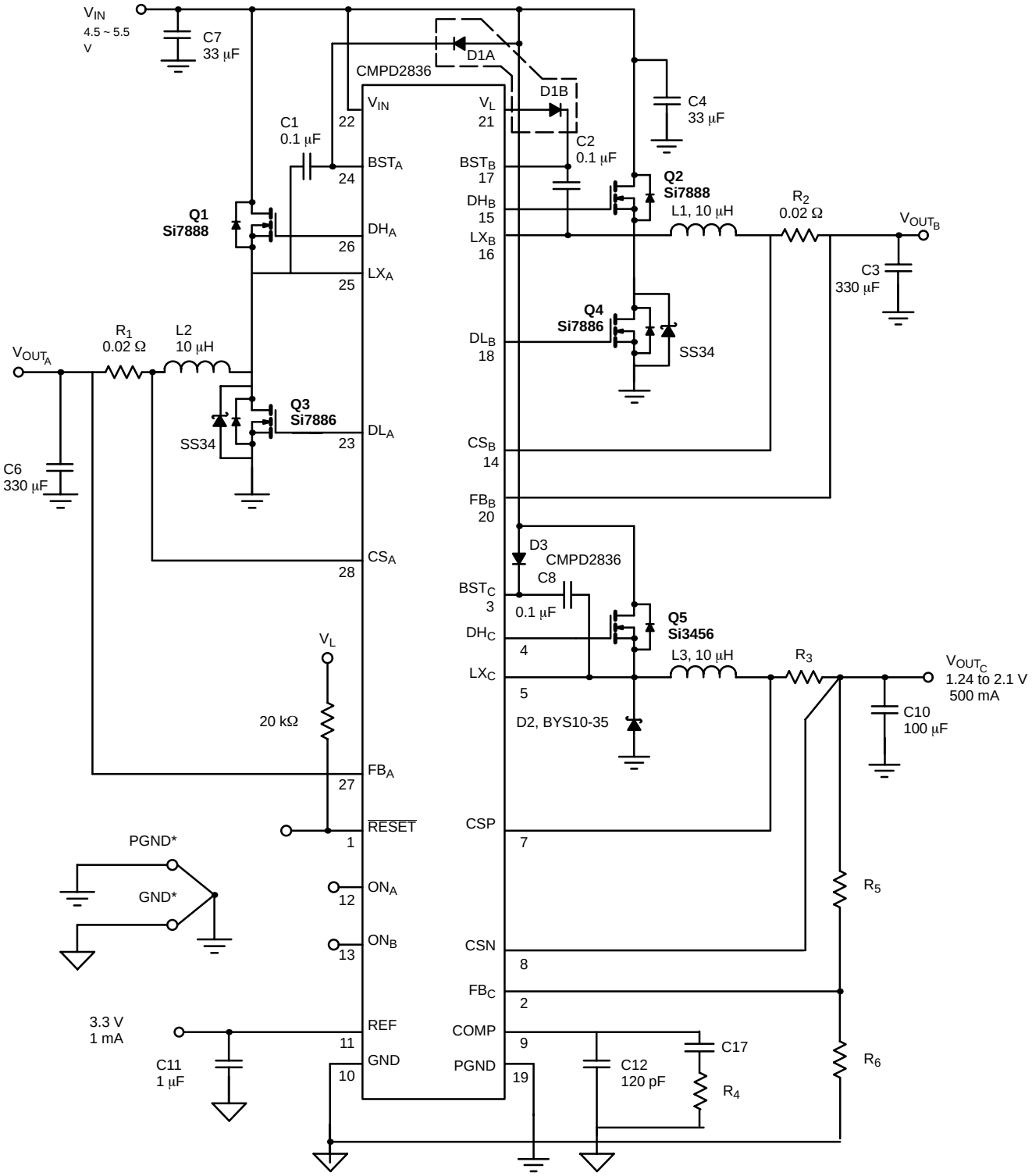
STANDARD APPLICATION CIRCUIT (5-V INPUT — AUXILIARY IN BOOST MODE)



*PGND and GND planes should be connected to a single point (star) ground.

Figure 1.B

STANDARD APPLICATION CIRCUIT (5-V INPUT — AUXILIARY IN BUCK MODE)



*PGND and GND planes should be connected to a single point (star) ground.

Figure 1.C

TIMING DIAGRAMS

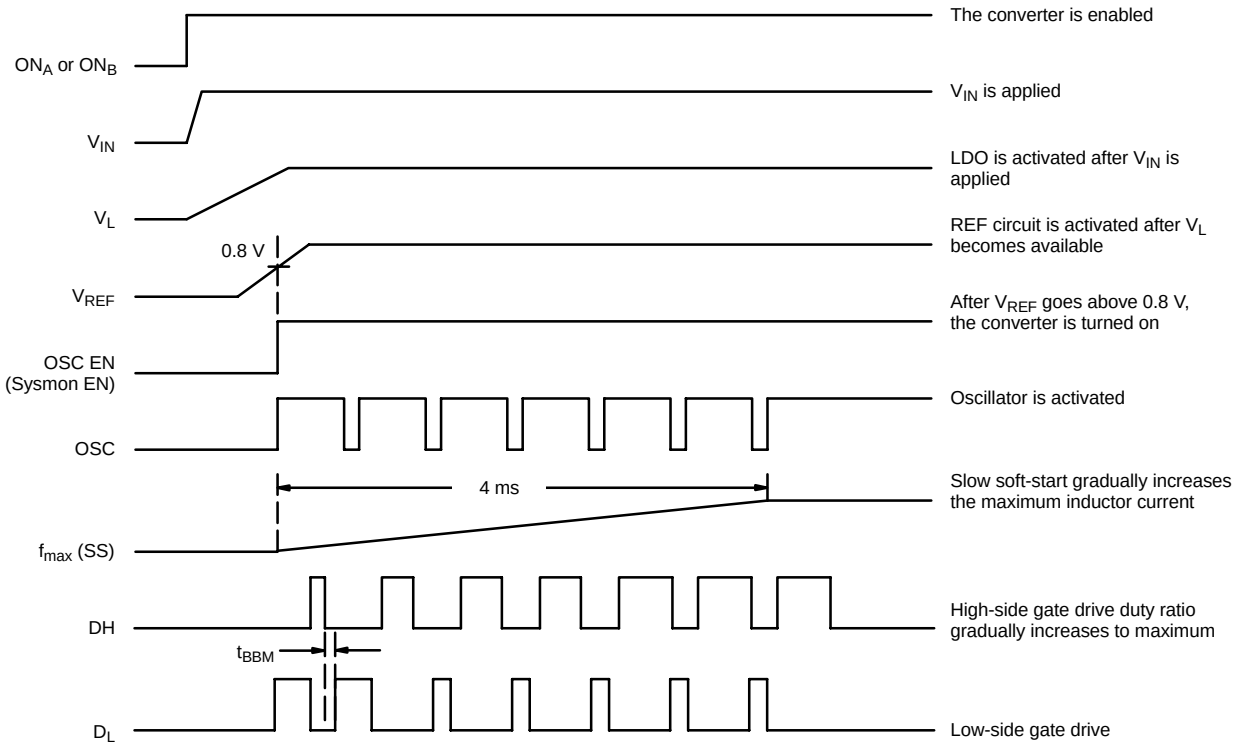


FIGURE 2. Converter is Enabled Before V_{IN} is Applied, A or B controllers

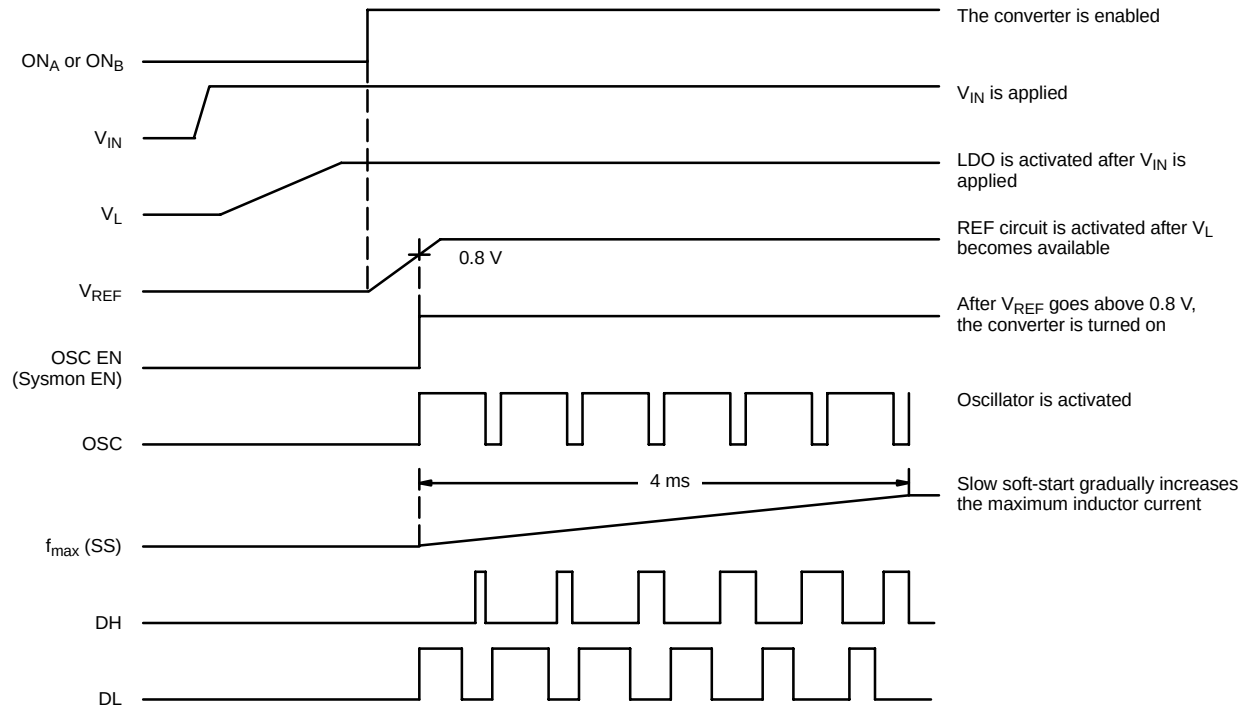


FIGURE 3. Converter is Enabled After V_{IN} is Applied, A or B Controllers

TIMING DIAGRAMS

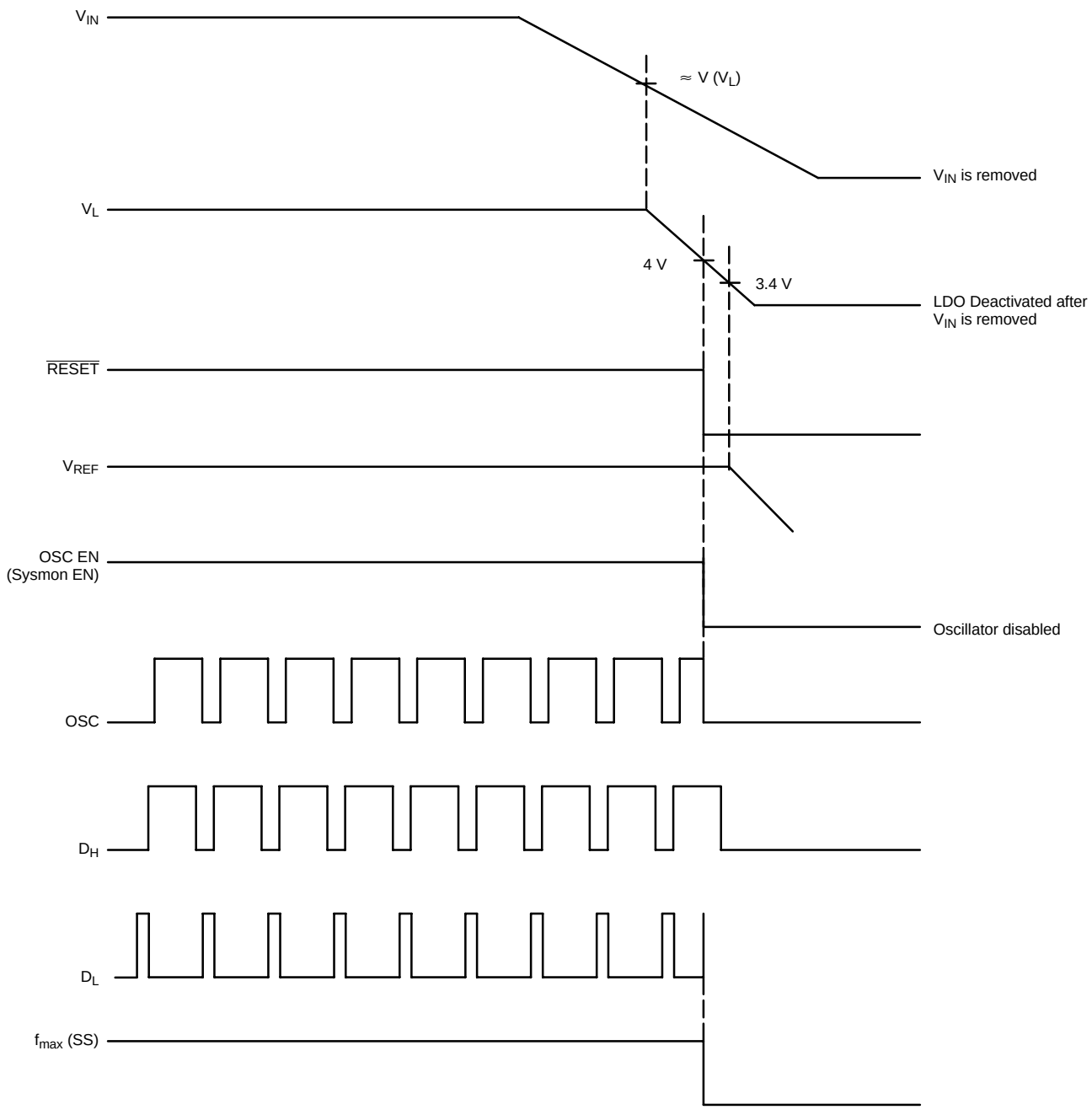


FIGURE 4. Power Off Sequence

DETAILED FUNCTIONAL BLOCK DIAGRAMS

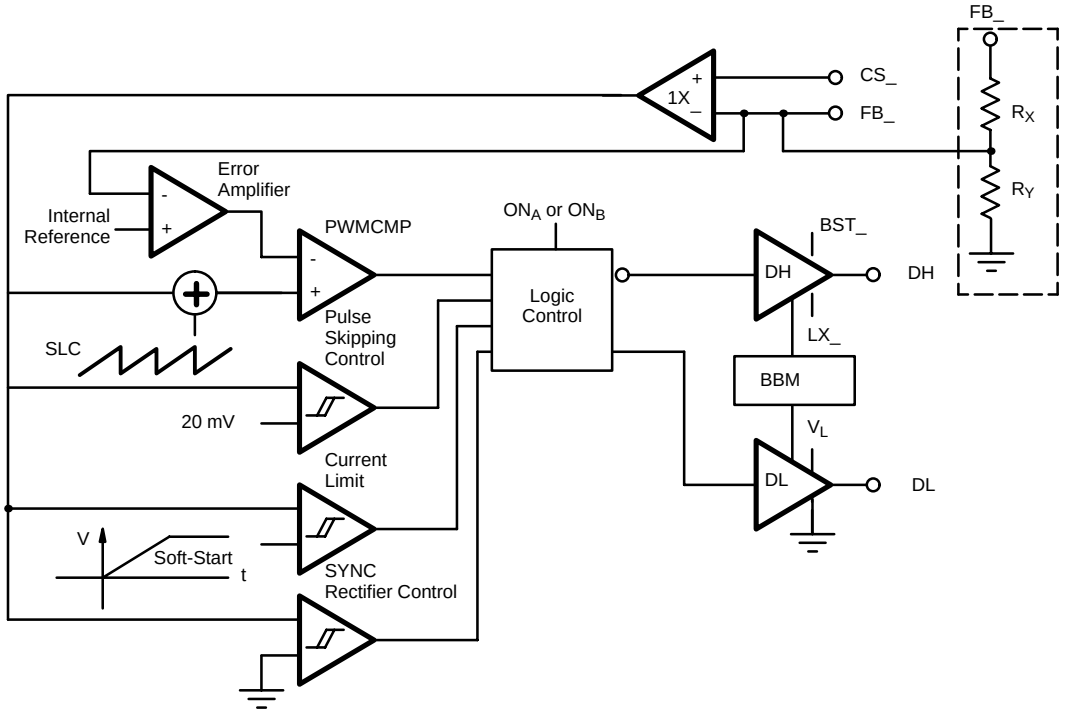


FIGURE 5. Buck Block Diagram (SMPS A and B Controllers)

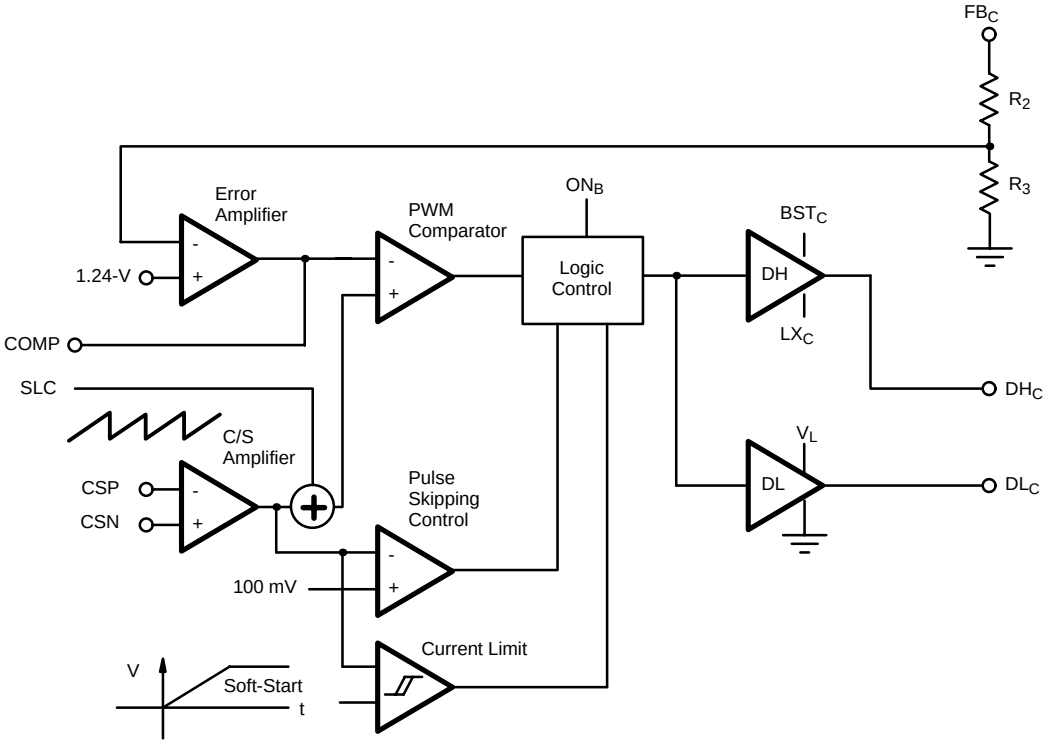


FIGURE 6. Buck-Boost Block Diagram (Auxiliary SMPS Controller C)

DETAILED FUNCTIONAL BLOCK DIAGRAMS

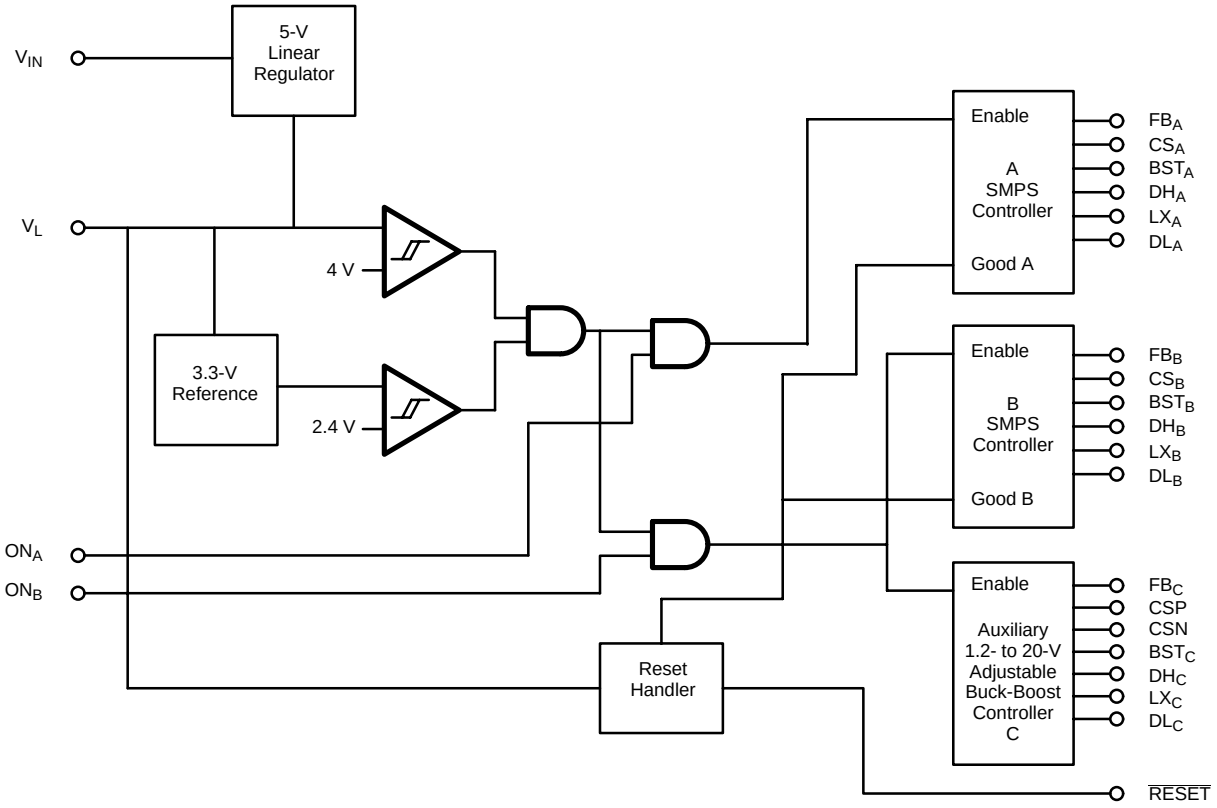


FIGURE 7. Complete Si9139 Block Diagram

DESCRIPTION OF OPERATION

Shutdown Mode

The logic threshold for the ON_A and ON_B pins is 1.6 V. Input voltage must be 0.8 V or less for logic low and 2.4 V or higher for logic high.

Start-up Sequence

Start-up is controlled by individual ON/OFF control. The A output is controlled by ON_A whilst the B and the C adjustable outputs are both controlled by ON_B.

When both the A and B SMPS outputs are within tolerance and 32,000 clock cycles (typically equal to 107 ms) have elapsed since the second SMPS output went into regulation, the $\overline{RESET}$ pin will go high, signifying that all converters are operating correctly (see $\overline{RESET}$ Power Good Voltage Monitor).

The Si9139 converts a 4.5-V to 30-V input voltage to five different output voltages; two buck (step-down) high current, PWM, switch-mode supplies of 1.5-V to 3.3-V, one “Buck-Boost” PWM switch-mode supply adjustable from 1.24 V to 20 V, one precision 3.3-V reference and one 5-V low drop out (LDO) linear regulator output. Switch-mode supply output current capabilities depend on external components (can be selected to exceed 10 A). In the standard application circuit illustrated in Figure 1, each buck converter is capable of delivering 5 A, with the buck-boost converter delivering 500 mA.

DESCRIPTION OF OPERATION (CONT'D)

Buck Converter Operation: Converters A and B

The A and B buck converters are both current-mode PWM and PSM (during light load operation) regulators using high-side bootstrap n-channel and low-side n-channel MOSFETs. At light load conditions, the converters switch at a lower frequency than the clock frequency. This operating condition is defined as pulse-skipping. The operation of the converter(s) switching at clock frequency is defined as normal operation.

Normal Operation PWM: Buck Converters A and B

In normal operation, the buck converter high-side MOSFET is turned on with a delay (known as break-before-make time - t_{BBM}), after the rising edge of the clock. After a certain on time, the high-side MOSFET is turned off and then after a delay (t_{BBM}), the low-side MOSFET is turned on until the next rising edge of the clock, or the inductor current reaches zero. The t_{BBM} (approximately 25 ns to 60 ns), has been optimized to guarantee the efficiency is not adversely affected at the high switching frequency and a specified minimum to account for variations of possible MOSFET gate capacitances.

During the normal operation, the high-side MOSFET switch on-time is controlled internally to provide excellent line and load regulation over temperature. Both buck converters have load, line, regulation to within 1.0% tolerance.

Pulse Skipping Operation: Buck Converters A and B

When the buck converter switching frequency is less than the internal clock frequency, its operation mode is defined as pulse skipping mode. During this mode, the high-side MOSFET is turned on until V_{CS}-V_{FB} reaches 20 mV, or the on time reaches its maximum duty ratio. After the high-side MOSFET is turned off, the low-side MOSFET is turned on after the t_{BBM} delay, which will remain on until the inductor current reaches zero. The output voltage will rise slightly above the regulation voltage after this sequence, causing the controller to stay idle for the next clock cycle, or several clock cycles. When the output voltage falls slightly below the regulation level, the high-side MOSFET will be turned on again at the next clock cycle. With the converter remaining idle during some clock cycles, the switching losses are reduced preserving conversion efficiency during the light output current condition.

Current Limit: Buck Converters

When the buck converter inductor current is too high, the voltage across pin CS3 and pin FB will exceed the 125 mV current limit threshold, causing the high-side MOSFET to be turned off instantaneously regardless of the input, or output condition. The Si9139 features clock cycle by clock cycle current limiting capability.

Auxiliary Converter C Operation: Buck-Boost Operation

The Si9139 has an auxiliary adjustable 1.24-V to 20-V output non-isolated buck-boost converter, called for brevity a Buck-Boost. The input voltage range can span above or below the regulated output voltage. It consists of two n-channel MOSFET switches that are turned on and off in phase, and two diodes. Similar to the buck converter, during the light load conditions, the Buck-Boost converter will switch at a frequency lower than the internal clock frequency, which can be defined as pulse skipping mode (PSM); otherwise, it operates in normal PWM mode.

The output voltage of the Buck-Boost converter is set by two resistors (R_5 and R_6, see Figure 1.A) where,

$$V_{OUT_C} = \frac{(R_5 + R_6)}{R_6} \times V_{FB}$$

Auxiliary Converter C Normal Operation: Buck-Boost Mode

In buck-boost operation mode, the two MOSFETs are turned on at the rising edge of the clock, and then turned off. The on time is controlled internally to provide excellent load, line, and temperature regulation. The Buck-Boost converter has load, line and temperature regulation well within 5%.

Auxiliary Converter C Pulse Skipping Operation: Buck-Boost Converter

Under the light load conditions, similar to the buck converter, the Buck-Boost converter will enter pulse skipping mode. The MOSFETs will be turned on until the inductor current increases to such a level that the voltage across the pin CSP and pin CSN reaches 360 mV, or the on time reaches the maximum duty cycle. After the MOSFETs are turned off, the inductor current will conduct through two diodes until it reaches zero. At this point, the Buck-Boost converter output will rise slightly above the regulation level, and the converter will stay idle for one or several clock cycle(s) until the output falls back slightly below the regulation level. The switching losses are reduced by skipping pulses preserving the efficiency during light load.

DESCRIPTION OF OPERATION (CONT'D)

Auxiliary Converter C Normal Operation: Boost Mode

The auxiliary converter may be operated in boost mode as shown in Figure 1.B when operating from a 5 V ± 10% input supply voltage. This ability reduces the component count of the converter and provides a high efficiency output voltage of in the range of 6 V to 20 V at up to10 W of power. Operation is similar to the buck-boost mode described above.

Auxiliary Converter C Normal Operation: Buck Mode

The auxiliary converter may also be operated in buck mode as shown in Figure 1.C when operating from a 5 V ± 10% input supply voltage. This ability reduces the component count of the converter and provides a high efficiency output voltage of in the range of 1.24 V to 2.1 V with 1 W of power. Operation is similar to the buck-boost mode described above.

Auxiliary Converter C Current Limit

Similar to the buck converter; when the voltage across pin CSP and pin CSN exceeds 360-mV typical, the two MOSFETs will be turned off regardless of the input and output conditions.

Grounding:

There are two separate grounds on the Si9139, analog signal ground (GND) and power ground (PGND). The purpose of two separate grounds is to prevent the high currents on the power devices (both external and internal) from interfering with the analog signals. The internal components of Si9139 have their grounds tied (internally) together. These two grounds are then tied together (externally) at a single point, to ensure Si9139 noise immunity.

This separation of grounds should be maintained in the external circuitry, with the power ground of all power devices being returned directly to the input capacitors, and the small signal ground being returned to the GND pin of Si9139.

$\overline{\text{RESET}}$ Handler

The power-good monitor generates a system $\overline{\text{RESET}}$ signal. At first power-up ($ON_{A/B}$ going high), $\overline{\text{RESET}}$ is held low until the A and B outputs are in regulation and beyond the UVLO timer. At this point, an internal timer begins counting oscillator pulses and $\overline{\text{RESET}}$ continues to be held low until 32,000 cycles have elapsed. After this timeout period, 107 ms @ 300 kHz, $\overline{\text{RESET}}$ is actively pulled up to V_L, when the recommended 20-kΩ resistor to V_L is on the $\overline{\text{RESET}}$ pin.

Output Overvoltage Protection

The A and B SMPS outputs are monitored for overvoltage. If either output is more than 10% above the nominal regulation point, all low-side gate drivers are latched high until ON_A and ON_B are toggled. This action turns on the synchronous rectifier MOSFETs with a 100% duty cycle, in turn rapidly discharging the output capacitors and forcing all SMPS outputs to ground.

Output Undervoltage Protection

In Si9139, each of the A and B SMPS outputs has an undervoltage protection circuit that is activated 6,144 clock cycles (20.48 ms) after the SMPS is enabled. If either SMPS output is typically under 70% of the nominal value, all SMPSs are latched off and their outputs are clamped to ground by the synchronous rectifier MOSFETs. The SMPS will not restart until both ON_A and ON_B are toggled.

Stability:

Buck Converters:

In order to simplify designs, the A and B supplies do not require external frequency compensation. Meanwhile, it achieves excellent regulation and efficiency. The converters are current mode control, with a bandwidth substantially higher than the LC tank dominant pole frequency of the output filter. To ensure stability, the minimum capacitance and maximum ESR values are:

$$C_{LOAD} \geq \frac{V_{REF}}{2\pi \times V_{OUT} \times R_{CS} \times BW} \qquad ESR \leq \frac{V_{OUT} \times R_{cs}}{V_{REF}}$$

where V_{REF} = 3.3 V, V_{OUT} is the output voltage (A or B), Rcs is the current sensing resistor in ohms and BW = 50 khz. With the components specified in the application circuit (L = 10 μH, R_{CS} = 0.02 Ω, C_{OUT} = 330 μF, ESR approximately 0.1 Ω), the converter has a bandwidth of approximately 50 kHz, with minimum phase margin of 65°, and dc gain above 50 dB.

Other Outputs

The Si9139 also provides a 3.3-V reference which can be externally loaded up to 1 mA, as well as, a 5-V LDO output which can be loaded up to 30 mA, or even more depending on the system application. For stability, the 3.3-V reference output requires a 1-μF capacitor, and the 5-V LDO output requires a 10-μF capacitor.

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