

## DS34LV87T Enhanced CMOS Quad Differential Line Driver

Check for Samples: [DS34LV87T](#)

### FEATURES

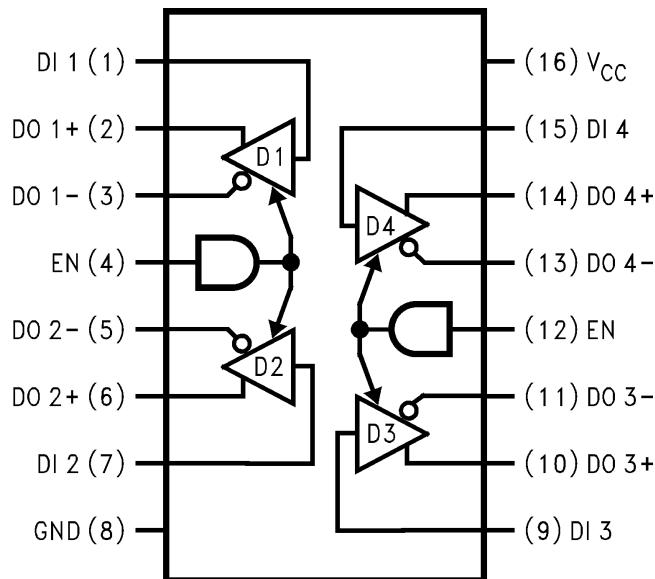
- Meets TIA/EIA-422-B (RS-422) and ITU-T V.11 Recommendation
- Interoperable With Existing 5V RS-422 Networks
- Ensured  $V_{OD}$  of 2V Min Over Operating Conditions
- Balanced Output Crossover for Low EMI (Typical Within 40 mV of 50% Voltage Level)
- Low Power Design (330  $\mu$ W @ 3.3V Static)
- ESD  $\geq 7$  kV on Cable I/O Pins (HBM)
- Industrial Temperature Range
- Ensured AC Parameter:
  - Maximum Driver Skew: 2 ns
  - Maximum Transition Time: 10 ns
- Pin Compatible With DS26C31
- Available in SOIC Packaging

### DESCRIPTION

The DS34LV87T is a high speed quad differential CMOS driver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS34LV87T features low static  $I_{CC}$  of 100  $\mu$ A max which makes it ideal for battery powered and power conscious applications. The TRI-STATE enable, EN, allows the device to be disabled when the device is not in use to minimize power. The dual enable scheme allows for flexibility in turning devices on or off.

Protection diodes protect all the driver inputs against electrostatic discharge. The driver and enable inputs (DI and EN) are compatible with LVTTTL and LVC MOS devices. Differential outputs have the same  $V_{OD}$  ( $\geq 2$ V) ensure as the 5V version. The outputs have enhanced ESD Protection providing greater than 7 kV tolerance.

### Connection Diagram



**Figure 1. Dual-In-Line Package (Top View)**  
See Package Number D0016A

### TRUTH TABLE<sup>(1)</sup>

| Enables | Input | Outputs |     |
|---------|-------|---------|-----|
| EN      | DI    | DO+     | DO- |
| L       | X     | Z       | Z   |
| H       | H     | H       | L   |
| H       | L     | L       | H   |

- (1) L = Low logic state  
X = Irrelevant  
H = High logic state  
Z = TRI-STATE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>

|                                             |                       |                          |
|---------------------------------------------|-----------------------|--------------------------|
| Supply Voltage ( $V_{CC}$ )                 |                       | -0.5V to +7V             |
| Enable Input Voltage (EN)                   |                       | -0.5V to $V_{CC} + 0.5V$ |
| Driver Input Voltage ( $D_I$ )              |                       | -0.5V to $V_{CC} + 0.5V$ |
| Clamp Diode Current                         |                       | $\pm 20$ mA              |
| DC Output Current, per pin                  |                       | $\pm 150$ mA             |
| Driver Output Voltage                       | (Power Off: DO+, DO-) | -0.5V to +7V             |
| Maximum Package Power Dissipation<br>@+25°C | D Package             | 1226 mW                  |
| Derate D Package                            |                       | 9.8 mW/°C above +25°C    |
| Storage Temperature Range                   |                       | -65°C to +150°C          |
| Lead Temperature Range (Soldering, 4 sec.)  |                       | +260°C                   |
| ESD Ratings (HBM, 1.5k, 100 pF)             | Driver Outputs        | $\geq 7$ kV              |
|                                             | Other Pins            | $\geq 2.5$ kV            |

- (1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (2) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The table of [Electrical Characteristics](#) specifies conditions of device operation.

## RECOMMENDED OPERATING CONDITIONS

|                             |                                          | Min | Typ | Max | Units |
|-----------------------------|------------------------------------------|-----|-----|-----|-------|
| Supply Voltage ( $V_{CC}$ ) |                                          | 3.0 | 3.3 | 3.6 | V     |
| Operating Free Air          | Temperature Range ( $T_A$ )<br>DS34LV87T | -40 | 25  | +85 | °C    |
| Input Rise and Fall Time    |                                          |     |     | 500 | ns    |

## ELECTRICAL CHARACTERISTICS<sup>(1)(2)</sup>

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

| Symbol            | Parameter                                          | Conditions                                                                       | Pin             | Min  | Typ   | Max             | Units |
|-------------------|----------------------------------------------------|----------------------------------------------------------------------------------|-----------------|------|-------|-----------------|-------|
| V <sub>OD1</sub>  | Output Differential Voltage                        | R <sub>L</sub> = ∞, (No Load)                                                    | DO+,<br>DO–     |      | 3.3   | 4.0             | V     |
| V <sub>OD2</sub>  | Output Differential Voltage                        | R <sub>L</sub> = 100Ω See <a href="#">Figure 2</a>                               |                 | 2    | 2.6   |                 | V     |
| ΔV <sub>OD2</sub> | Change in Magnitude of Output Differential Voltage |                                                                                  |                 | –400 | 7     | 400             | mV    |
| V <sub>OD3</sub>  | Output Differential Voltage                        | R <sub>L</sub> = 3900Ω (V.11), See <a href="#">Figure 2</a> <sup>(3)</sup>       |                 |      | 3.2   | 3.5             | V     |
| V <sub>OC</sub>   | Common Mode Voltage                                | R <sub>L</sub> = 100Ω See <a href="#">Figure 2</a>                               |                 |      | 1.5   | 2               | V     |
| ΔV <sub>OC</sub>  | Change in Magnitude of Common Mode Voltage         |                                                                                  |                 | –400 | 6     | 400             | mV    |
| I <sub>OZ</sub>   | TRI-STATE Leakage Current                          | V <sub>OUT</sub> = V <sub>CC</sub> or GND<br>Drivers Disabled                    |                 |      | ±0.5  | ±20             | μA    |
| I <sub>SC</sub>   | Output Short Circuit Current                       | V <sub>OUT</sub> = 0V<br>V <sub>IN</sub> = V <sub>CC</sub> or GND <sup>(4)</sup> |                 | –40  | –70   | –150            | mA    |
| I <sub>OFF</sub>  | Output Leakage Current                             | V <sub>CC</sub> = 0V, V <sub>OUT</sub> = 3V                                      |                 |      | 0.03  | 100             | μA    |
|                   |                                                    | V <sub>CC</sub> = 0V, V <sub>OUT</sub> = –0.25V                                  |                 |      | –0.08 | –100            | μA    |
| V <sub>IH</sub>   | High Level Input Voltage                           |                                                                                  | DI,<br>EN       | 2.0  |       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>   | Low Level Input Voltage                            |                                                                                  |                 | GND  |       | 0.8             | V     |
| I <sub>IH</sub>   | High Level Input Current                           | V <sub>IN</sub> = V <sub>CC</sub>                                                |                 |      |       | 10              | μA    |
| I <sub>IL</sub>   | Low Level Input Current                            | V <sub>IN</sub> = GND                                                            |                 | –10  |       |                 | μA    |
| V <sub>CL</sub>   | Input Clamp Voltage                                | I <sub>IN</sub> = –18 mA                                                         |                 |      |       | –1.5            | V     |
| I <sub>CC</sub>   | Power Supply Current                               | No Load, V <sub>IN</sub> (all) = V <sub>CC</sub> or GND                          | V <sub>CC</sub> |      |       | 100             | μA    |

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages V<sub>OD1</sub>, V<sub>OD2</sub>, V<sub>OD3</sub>.
- (2) All typical values are given for V<sub>CC</sub> = 3.3V and T<sub>A</sub> = +25°C.
- (3) This specification limit is for compliance with TIA/EIA-422-B and ITU-T V.11.
- (4) Only one output shorted at a time. The output (true or complement) is configured High.

**SWITCHING CHARACTERISTICS<sup>(1)(2)</sup>**

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

| Symbol     | Parameter                                                | Conditions                                                                                            | Min | Typ  | Max | Units |
|------------|----------------------------------------------------------|-------------------------------------------------------------------------------------------------------|-----|------|-----|-------|
| $t_{PHLD}$ | Differential Propagation Delay<br>High to Low            | $R_L = 100\Omega$ , $C_L = 50\text{ pF}$<br>See <a href="#">Figure 3</a> and <a href="#">Figure 4</a> | 6   | 10.5 | 16  | ns    |
| $t_{PLHD}$ | Differential Propagation Delay<br>Low to High            |                                                                                                       | 6   | 11   | 16  | ns    |
| $t_{SKD}$  | Differential Skew<br>$ t_{PHLD} - t_{PLHD} $             |                                                                                                       |     | 0.5  | 2.0 | ns    |
| $t_{SK1}$  | Skew, Pin to Pin (same device)                           |                                                                                                       |     | 1.0  | 2.0 | ns    |
| $t_{SK2}$  | Skew, Part to Part <sup>(3)</sup>                        |                                                                                                       |     | 3.0  | 5.0 | ns    |
| $t_{TLH}$  | Differential Transition Time<br>Low to High (20% to 80%) |                                                                                                       |     | 4.2  | 10  | ns    |
| $t_{THL}$  | Differential Transition Time<br>High to Low (80% to 20%) |                                                                                                       |     | 4.7  | 10  | ns    |
| $t_{PHZ}$  | Disable Time High to Z                                   | See <a href="#">Figure 5</a> and <a href="#">Figure 6</a>                                             |     | 12   | 20  | ns    |
| $t_{PLZ}$  | Disable Time Low to Z                                    |                                                                                                       |     | 9    | 20  | ns    |
| $t_{PZH}$  | Enable Time Z to High                                    |                                                                                                       |     | 22   | 32  | ns    |
| $t_{PZL}$  | Enable Time Z to Low                                     |                                                                                                       |     | 22   | 32  | ns    |
| $f_{MAX}$  | Maximum Operating Frequency <sup>(4)</sup>               |                                                                                                       |     | 32   |     | MHz   |

(1)  $f = 1\text{ MHz}$ ,  $t_r$  and  $t_f \leq 6\text{ ns}$  (10% to 90%).

(2) See TIA/EIA-422-B specifications for exact test conditions.

(3) Devices are at the same  $V_{CC}$  and within  $5^\circ\text{C}$  within the operating temperature range.

(4) All channels switching, output duty cycle criteria is 40%/60% measured at 50%. This parameter is ensured by design and characterization.

## PARAMETER MEASUREMENT INFORMATION

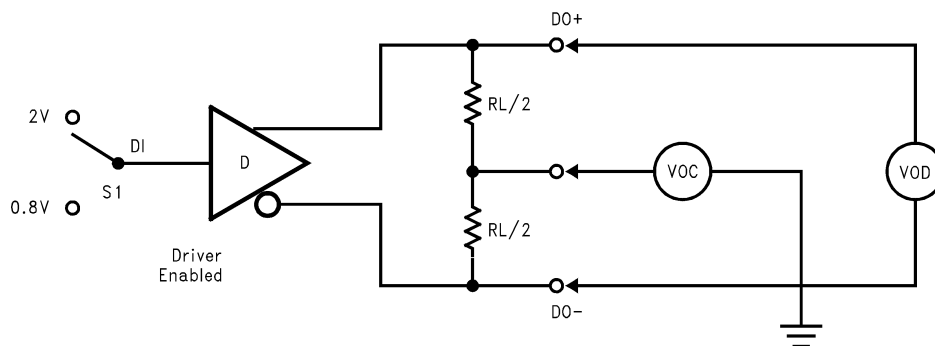


Figure 2. Differential Driver DC Test Circuit

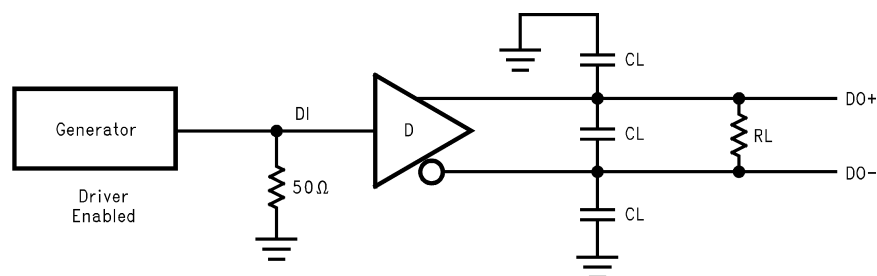
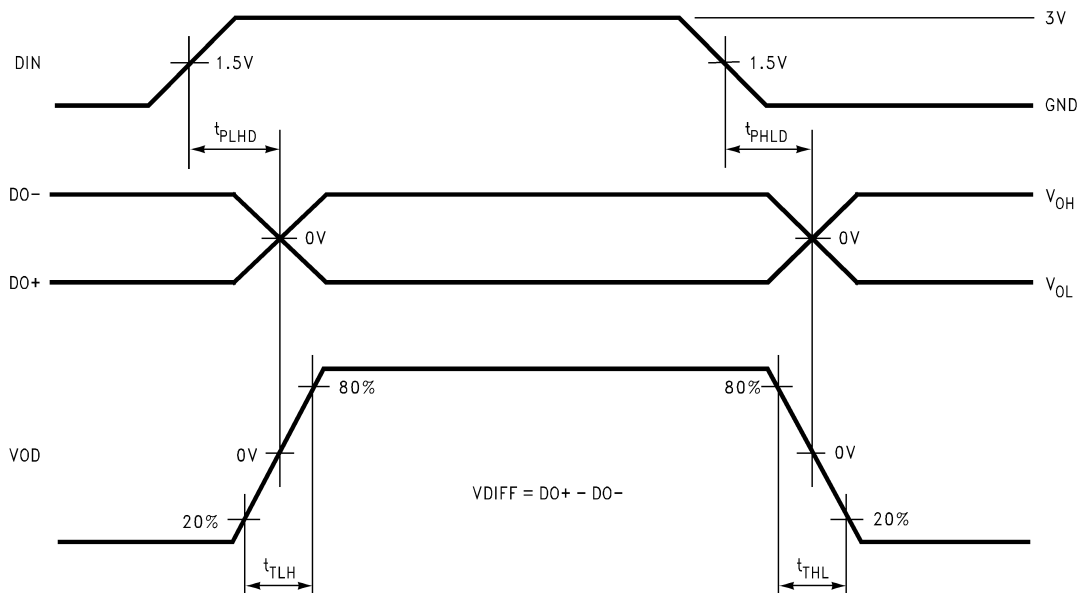


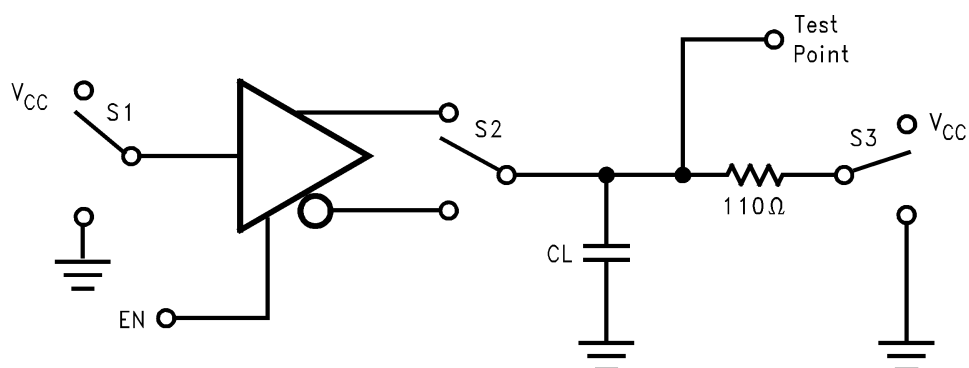
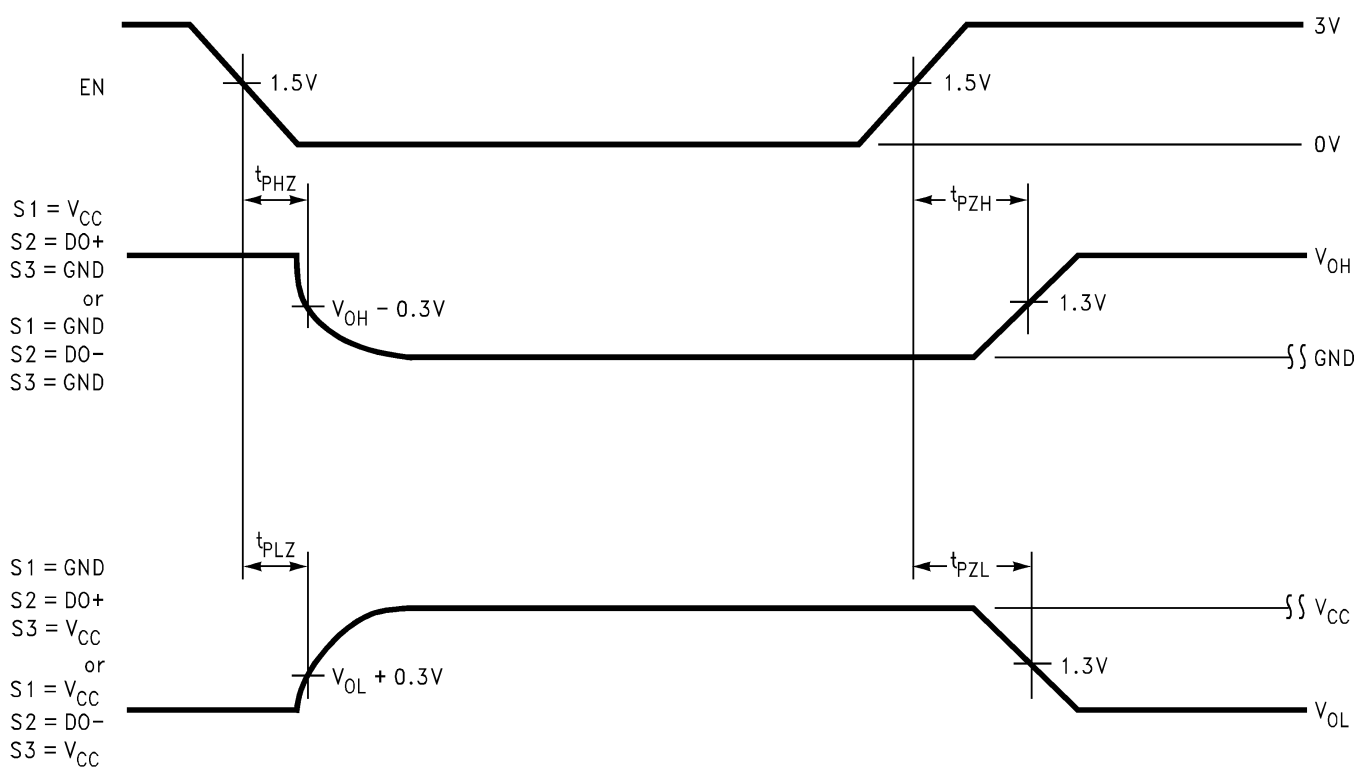
Figure 3. Differential Driver Propagation Delay and Transition Time Test Circuit



Generator waveform for all tests unless otherwise specified:  $f = 1\text{ MHz}$ , Duty Cycle = 50%,  $Z_o = 50\Omega$ ,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

$C_L$  includes probe and fixture capacitance.

Figure 4. Differential Driver Propagation Delay and Transition Time Waveforms

**PARAMETER MEASUREMENT INFORMATION (continued)****Figure 5. Driver Single-Ended Tri-state Test Circuit****Figure 6. Driver Single-Ended Tri-state Waveforms**

## TYPICAL APPLICATION INFORMATION

General application guidelines and hints for differential drivers and receivers may be found in the following application notes:

- Transmission Line Drivers and Receivers for TIA/EIA Standards RS-422 and RS-423([SNLA137](#))
- A Comparison of Differential Termination Techniques([SNLA304](#))

Power Decoupling Recommendations:

Bypass caps must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1  $\mu\text{F}$  in parallel with 0.01  $\mu\text{F}$  at the power supply pin. A 10  $\mu\text{F}$  or greater tantalum or electrolytic should be connected at the power entry point on the printed circuit board.

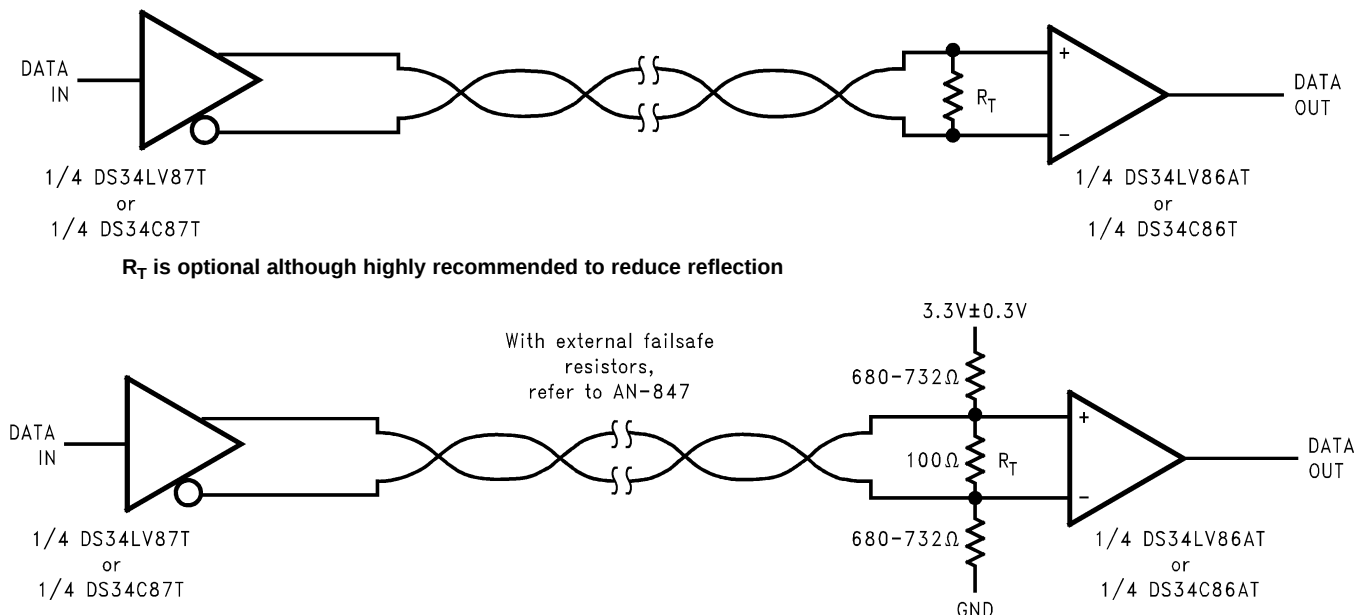


Figure 7. Typical Driver Connection

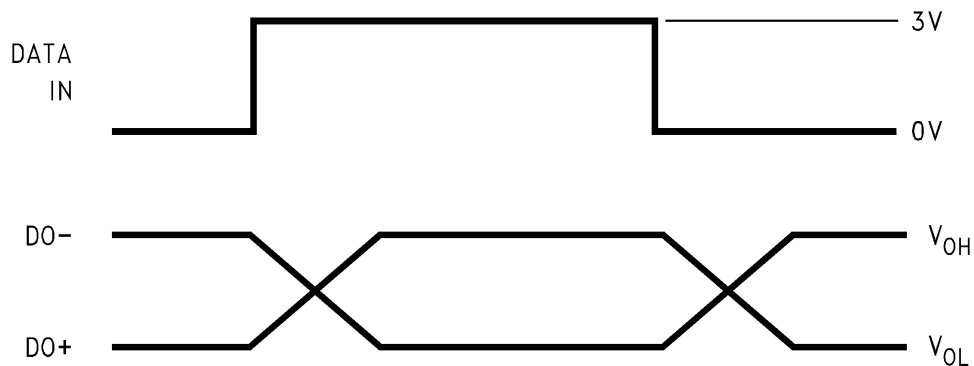


Figure 8. Typical Driver Output Waveforms

## REVISION HISTORY

### Changes from Revision C (April 2013) to Revision D

### Page

- Changed layout of National Data Sheet to TI format ..... [7](#)

## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">DS34LV87TM/NOPB</a>  | Active        | Production           | SOIC (D)   16  | 48   TUBE             | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | DS34LV87<br>TM      |
| DS34LV87TM/NOPB.A                | Active        | Production           | SOIC (D)   16  | 48   TUBE             | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | DS34LV87<br>TM      |
| <a href="#">DS34LV87TMX/NOPB</a> | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | DS34LV87<br>TM      |
| DS34LV87TMX/NOPB.A               | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | DS34LV87<br>TM      |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS34LV87TMX/NOPB | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.3     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS34LV87TMX/NOPB | SOIC         | D               | 16   | 2500 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device            | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| DS34LV87TM/NOPB   | D            | SOIC         | 16   | 48  | 495    | 8      | 4064   | 3.05   |
| DS34LV87TM/NOPB.A | D            | SOIC         | 16   | 48  | 495    | 8      | 4064   | 3.05   |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

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