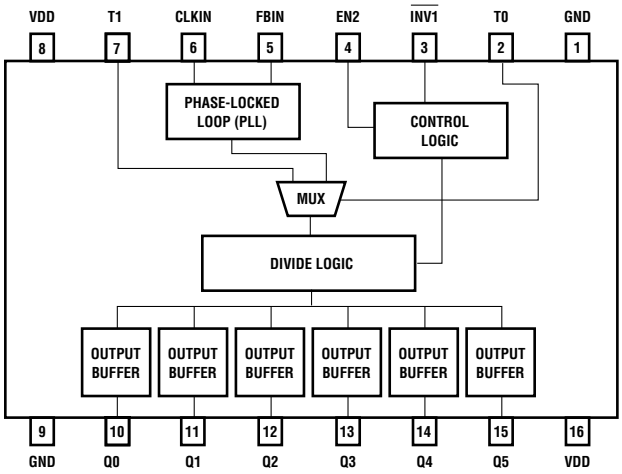
# GA1210E

## *Clock Doubler / Two-Phase Generator*

***Figure 1. Block Diagram***




TriQuint's GA1210E is a low-skew TTL-level clock doubler chip. It produces multiple clock outputs, at precisely 2X the input frequency, which are all phase-aligned to a periodic clock input signal. The GA1210E can generate clocks up to 100 MHz, making it an ideal solution for high-speed clock generation and routing.

The GA1210E guarantees precise clock control. The delay through the part is typically ± 250 ps. Skew at all six outputs is maintained to ± 250 ps, typically. When used with TriQuint's GA1110E multi-phase low-skew buffer, a complete system clocking solution can be achieved.

The capability to double clock signals while maintaining tight control over the phase and frequency of the output clocks is accomplished with the use of a 400 MHz internal phase-locked loop (PLL). By feeding back one of the 1X frequency output clocks (to FBIN), the on-chip PLL can continuously maintain synchronization between the input clock (CLKIN) and all six outputs. Any drift or variation in the system clock will be matched and tracked at the six outputs of the GA1210E.

The GA1210E offers several different configurations to accommodate the designer's high-speed clocking requirements. In addition to providing 2X outputs at 40–100 MHz frequencies, the GA1210E can also be configured to generate non-overlapping two-phase clocks. The combination of high speed and a selectable two-phase capability makes it ideal for clocking state machine and pipeline logic.

### *Features*

- *2X clock multiple generator*
- *Two-phase clock generator*
- *Zero propagation delay*
- *Output skew controlled to ± 250 ps (typ) ± 500 ps (max)*
- *Available in 20, 25, 33, 40 and 50 MHz versions*
- *High-drive, symmetric TTL-compatible outputs with rise time of 1.0 ns*
- *Self-contained on-chip 400 MHz phase-locked loop (PLL)*
- *Special test mode*
- *130 mA operating current (typ), 160 mA (max)*
- *Standard 16-pin DIP and 28-pin surface-mount packages*

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The GA1210E is fabricated using TriQuint's One-Up™ gallium arsenide technology to achieve precise timing control and to guarantee 100% TTL compatibility. The 20, 25, 33, 40, and 50 MHz input frequencies make this device ideal for high-speed clock generation and skew control in high-performance RISC- and CISC-based systems.

### *Functional Description*

The GA1210E TTL-level clock doubler and two-phase generator chip is capable of generating multiple 2X outputs from a periodic clock input. Two control pins, EN2 and $\overline{\text{INV1}}$, provide additional flexibility by selecting two-phase and inverted clocks, respectively.

Table 1 enumerates the four available sets of output clock configurations generated by the GA1210E. The first two columns represent the signal levels for the two control signals. EN2 is an active-HIGH signal which enables the two-phase clocking on outputs Q4 and Q5. $\overline{\text{INV1}}$ is an active-LOW signal which inverts the Q1 output to provide a $\overline{\text{1X}}$ clock output. The six columns specify the resulting waveforms on each output; they are shown in detail in Figure 4. Specifications for the phase and skew parameters associated with the output clocks are listed in the AC Characteristics table.

The GA1210E's primary function is to offer precisely phase-aligned, low-skew 2X versions of the CLKIN input. Since the 2X clocks are all synchronous to the input, high-frequency clocks can be generated locally. This relieves the difficulty of routing high-frequency clocks on a board or across a backplane. They can also be cascaded with other GA1210E devices to generate synchronous 4X clocks.

The GA1210E also has the capability to generate non-overlapping two-phase clocks. By setting the EN2 pin HIGH, two-phase clocks are generated at outputs Q4 and Q5. This is ideal for state machines and other logic structures which can be optimized through two-phase clocking. The two-phase clocks are synchronous to the remaining outputs at 1X and 2X frequencies, providing maximum flexibility in board- and system-level clocking solutions.

In all configurations, the 1X clock must be fed back, either directly or indirectly, to the FBIN input, enabling the on-chip PLL to maintain phase and frequency synchronization.

### *Multiple-Chip Applications*

Because of the tight input-output phase control, the GA1210E can be easily cascaded to build low-skew clock chains and clock trees. The generation and distribution of high-speed clocks can be accomplished with minimal skew allowance, permitting the system designer to obtain maximum performance from the microprocessor and other high-speed circuits in their designs. When combined with TriQuint's GA1110E low-skew, multi-phase clock buffer, a complete system clocking solution can be achieved. See Figure 5(Typical Applications).

### *Breaking the Feedback Loop*

There is no requirement that the external feedback connection be a direct hardwire from an output pin to the FBIN pin. So long as the signal at FBIN is derived directly from the Q0 output pin and maintains its frequency, additional logic incorporating any delay whatsoever can be accommodated. The internal phase-

locked loop will adjust the output clocks on the GA1210E to ensure continuous phase alignment between the FBIN and CLKIN signals. This feature is extremely valuable in synchronizing ASICs to the system clock.

*Caution:* The signal at FBIN must be continuous (i.e. not a gated or conditional signal), and must be derived directly from one of the GA1210E's 1X outputs.

### *Power-Up/Reset Synchronization*

The GA1210E utilizes on-chip phase-locked loop technology to maintain synchronization between inputs and outputs. Whenever the device is powered up, or the system clock (CLKIN) is reset, the phase-locked loop requires a synchronization time ($t_{SYNC}$) before lock is achieved. The maximum time required is specified in the AC Characteristics table.

For lock to occur, the Q0 output must always be connected (either directly or through additional ICs) to the FBIN input.

***Table 1. Configuration Table***

| *EN2* | *$\overline{INV1}$* | *Q0* | *Q1* | *Q2* | *Q3* | *Q4* | *Q5* |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1X | 1X | 2X | 2X | 2X | 2X |
| 0 | 1 | 1X | 1X | 2X | 2X | 2X | 2X |
| 1 | 0 | 1X | 1X | 2X | 2X | j1 | j2 |
| 1 | 1 | 1X | 1X | 2X | 2X | j1 | j2 |

*Notes:*
1. *1X: The output clock is a phase-aligned 1X copy of the CLKIN signal.*
2. *1X: The output clock is a 1X copy of CLKIN, 180° out of phase (i.e., inverted).*
3. *2X: The output clock is a phase-aligned 2X frequency of the CLKIN signal.*
4. *j1, j2: The outputs are the first and second of two phases, synchronous to CLKIN.*

### *GA1210E Test Mode*

The GA1210E has a test mode which can be enabled if the test pin T0 is HIGH. Under that condition, the clock signal from the test pin T1 is used as the clock input to the configuration logic, instead of the output from the PLL. This mode can be used to test only the internal state machine and associated logic. Each speed type and configuration has a unique signature which is present at the output after "n" number of input clock pulses. (For the GA1210E-25 there will be one output clock cycle for every 16 input clock cycles from $t_0$.) Figures 2 and 3 show the test mode and associated timing for Configuration 1.

When powered up, the Q0 through Q5 outputs can be in any state. It can take up to 16 clocks to get the outputs to the predetermined state at $t_0$. The number of clock cycles at input T1 required for one output clock cycle is 20 for GA1210E-20, 12 for the GA1210E-33, 8 for the GA1210E-40 and 8 for the GA1210E-50. The test input clock at T1 can either be used to single-step the outputs, or it can be clocked at rates up to 200 MHz. Please note that for the normal mode of operation, T0 is LOW (GND) and T1 is HIGH ($V_{DD}$) or No Connect (N/C).

***Figure 2. Test Mode for the GA1210E-25***

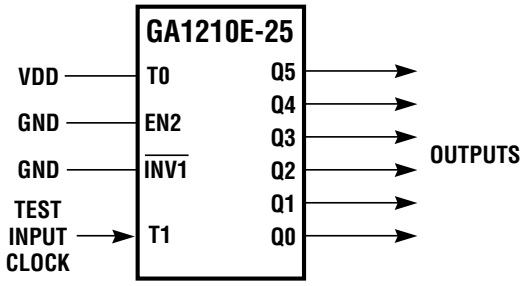


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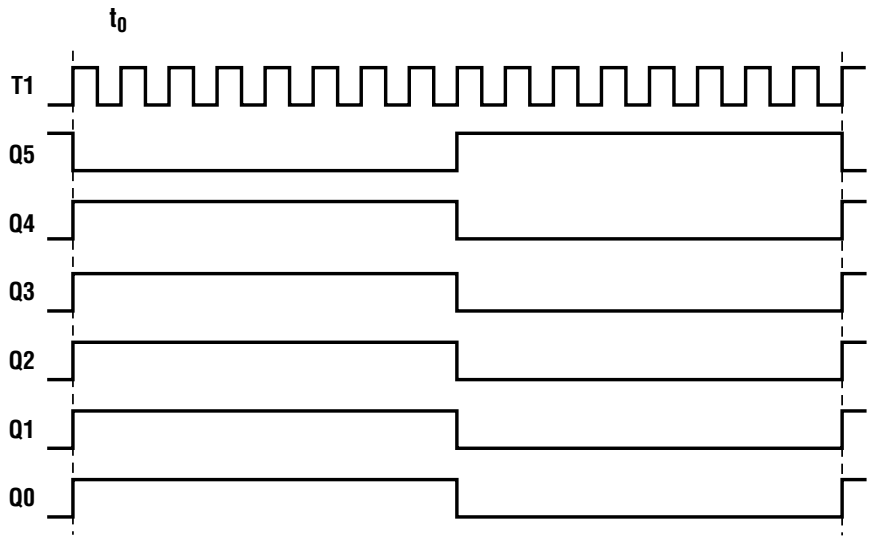
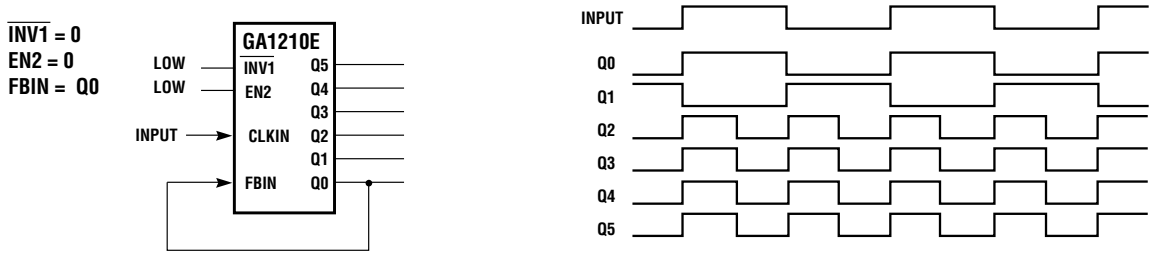
***Figure 3. GA1210E-25 Timing in Test Mode***
*(Configuration 1)*



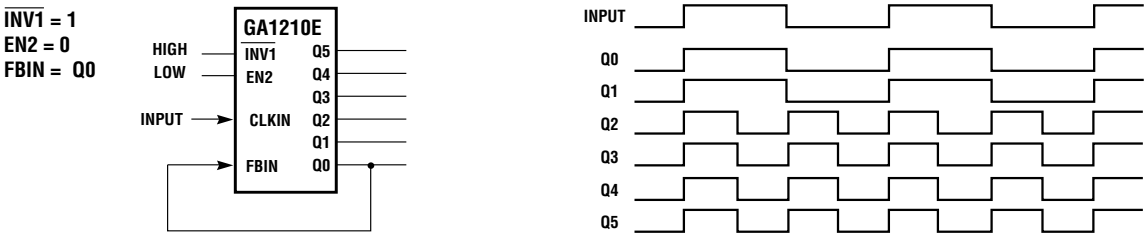

*Note: The above timing applies to the case when S1 = S0 = 0 and T0 = 1 (test mode).*

***Figure 4. Possible Configurations***

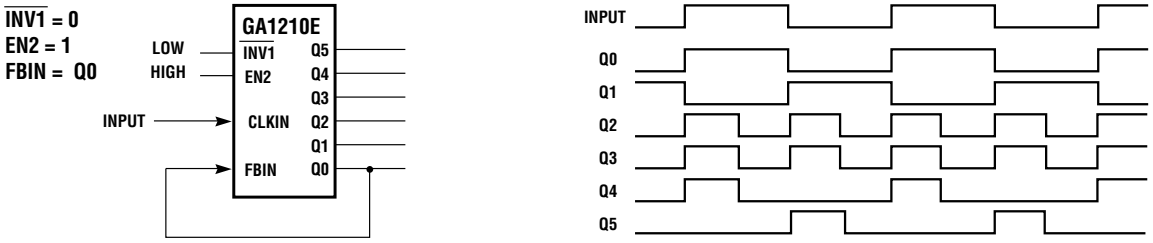
*Configuration 1*




***Configuration 2***




***Configuration 3***




***Configuration 4***

## *Typical Applications*

The GA1210E is designed to satisfy a wide range of system clocking requirements. It provides an ideal companion to the GA1110E multi-phase clock generator. Several application examples are illustrated below.

### 1) High-Frequency Low-Skew Clock Generation

The GA1210E's basic capability is the generation of multiple phase-aligned, low-skew clocks at 2X the input frequency.

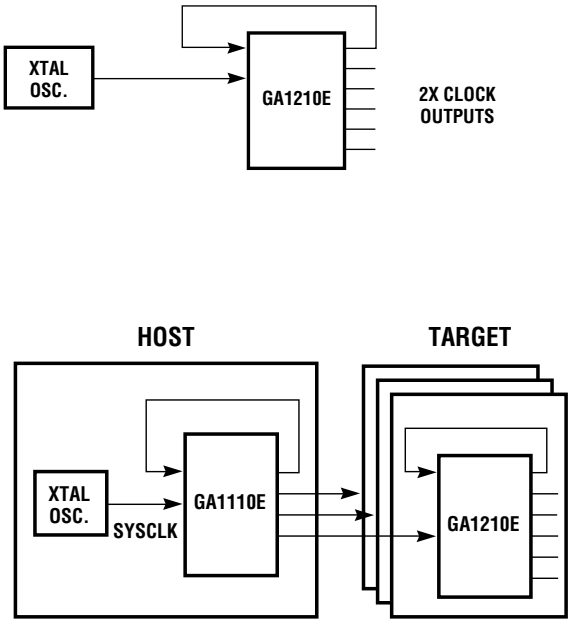
*• The GA1210E guarantees low skew among all clocks in the system by controlling both the input-to-output delay and the skew among all six clock outputs.*

### 2) Board-to-Board Clock Synchronization

Many computing systems today consist of multiple boards and cards designed to run synchronously. The skew associated with routing clocks across a backplane presents a major hurdle to maximizing system performance.

*• The tightly controlled input/output delay of the GA1210E ensures all boards in the system are running synchronously.*
*• The GA1210E can be used with the GA1110E to route lower frequency clocks across a backplane; the low-frequency signal is then doubled on the target boards, enabling them to run synchronously with the host board.*

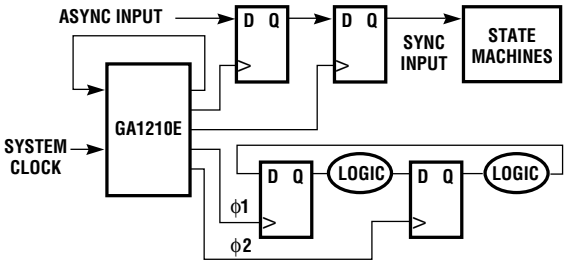
***Figure 5. Typical Applications***



### 3) Two-Phase Clocking

The GA1210E can be configured to generate synchronous two-phase clocks.

- *The two-phase clocks can be used for pipelined logic forms.*
- *Synchronous two-phase clocks can be used to eliminate metastability concerns by synchronizing asynchronous system inputs to the system clock.*




### 4) Clock Trees and Clock Chains

Used alone or with the GA1110E, the GA1210E distributes multiple copies of high-frequency clocks to the various blocks of a system. All of the clock signals at all of the destinations will run synchronously.

- *The controlled input-to-output delay allows long clock chains and trees.*

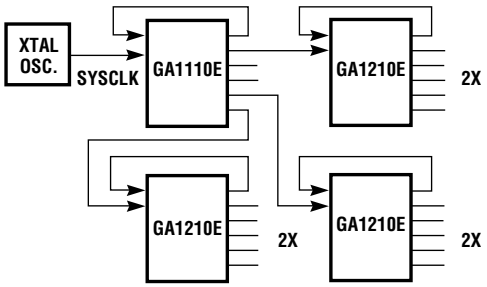



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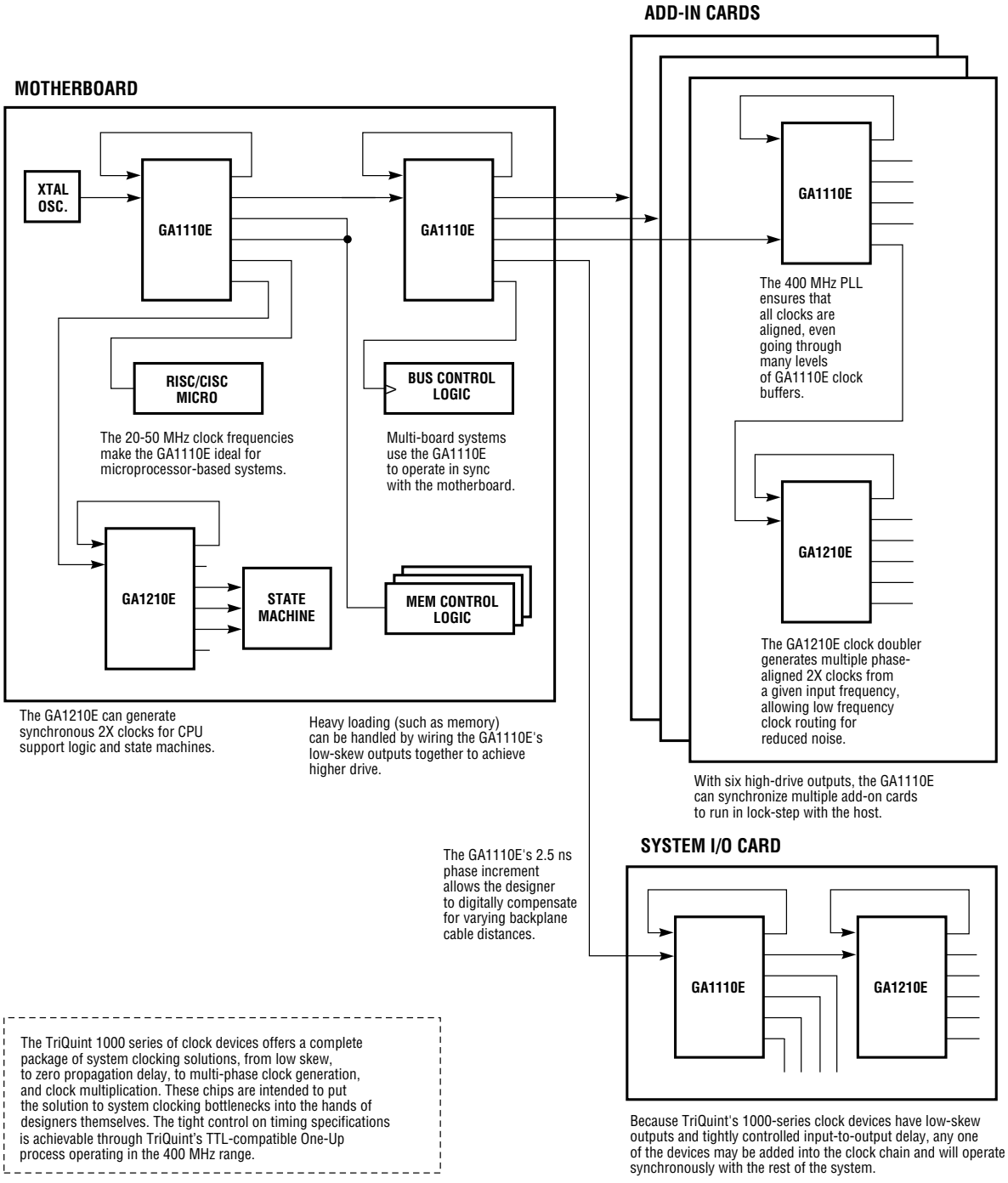
***Figure 6. System Clocking Solutions***




The TriQuint 1000 series of clock devices offers a complete package of system clocking solutions, from low skew, to zero propagation delay, to multi-phase clock generation, and clock multiplication. These chips are intended to put the solution to system clocking bottlenecks into the hands of designers themselves. The tight control on timing specifications is achievable through TriQuint's TTL-compatible One-Up process operating in the 400 MHz range.

### *Absolute Maximum Ratings*

| | |
|---|---|
| Storage temperature | –65 °C to +150 °C |
| Ambient temperature with power applied | –55 °C to +125 °C |
| Supply voltage to ground potential | –0.5 V to +7.0 V |
| DC input voltage | –0.5 V to +($V_{DD}$ + 0.5) |
| DC input current | –30 mA to +5 mA |

### *DC Characteristics* *(Supply voltage: +5 V ± 5% Ambient temp: 0 °C to +70 °C)*

| *Symbol* | *Description* | *Test Conditions* | *Limits [1] Min* | *Typ* | *Max* | *Unit* |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH voltage | $V_{DD}$ = Min $I_{OH}$= –24 mA<br>$V_{IN}$= $V_{IH}$ or $V_{IL}$ | 2.4 | 3.55 | | V |
| $V_{OL}$ | Output LOW voltage | $V_{DD}$ = Min $I_{OL}$ = 24 mA<br>$V_{IN}$= $V_{IH}$ or $V_{IL}$ | | 0.23 | 0.5 | V |
| $V_{IH}$ [2] | Input HIGH level | Guaranteed input logical HIGH<br>Voltage for all Inputs | 2.0 | | | V |
| $V_{IL}$ [2] | Input LOW level | Guaranteed input logical LOW<br>Voltage for all inputs | | | 0.8 | V |
| $I_{IL}$ | Input LOW current | $V_{DD}$ = Max $V_{IN}$ = 0.40 V | | –210 | –400 | µA |
| $I_{IH}$ | Input HIGH current | $V_{DD}$ = Max $V_{IN}$ = 2.7 V | | 0 | 25 | µA |
| $I_I$ | Input HIGH current | $V_{DD}$ = Max $V_{IN}$ = 5.5 V | | 2 | 1000 | µA |
| $I_{SC}$ [3] | Output short-circuit current | $V_{DD}$ = Max $V_{OUT}$ = 0.5 V | | –80 | | mA |
| $I_{DD}$ | Power supply current | $V_{DD}$ = Max | | 130 | 160 | mA |
| $V_I$ | Input clamp voltage | $V_{DD}$ = Min $I_{IN}$ = –18 mA | | –0.62 | –1.2 | V |
| $I_{OLD}$ | Dynamic switching | $V_{DD}$ = Max $V_{OLD}$ = 1.5 V | | 70 | | mA |
| $I_{OHD}$ | current | $V_{DD}$ = Max $V_{OHD}$ = 1.5 V | | –80 | | mA |

### *Capacitance [4]*

| *Symbol* | *Description* | *Test Conditions* | *Min* | *Typ* | *Max* | *Unit* |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 2.0 V at f = 1 MHz | | 6 | | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 2.0 V at f = 1 MHz | | 9 | | pF |

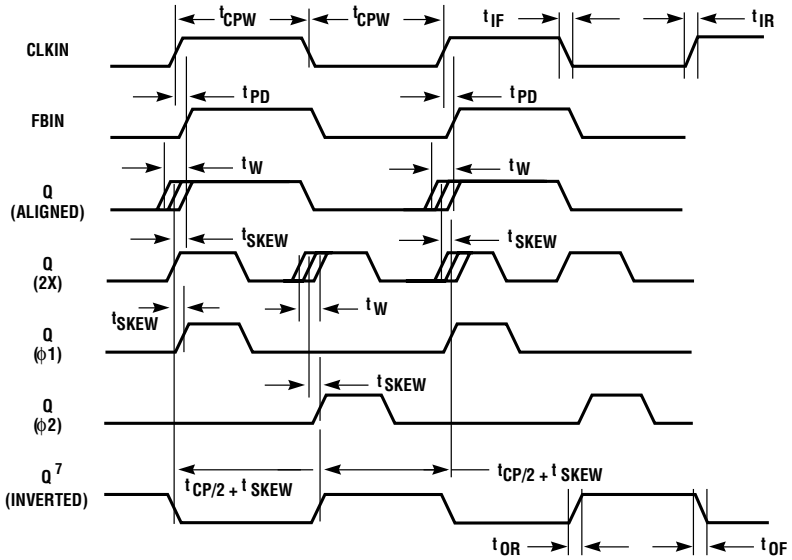
*Notes: 1. Typical limits are at $V_{DD}$ = 5.0 V and $T_A$ = 25 °C.*
*2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
*3. No more than one output should be tested at a time. Duration of the short circuit should not be more than one second. $V_{OUT}$ has been chosen to avoid test problems caused by tester ground degradation.*
*4. These parameters are not 100% tested, but are periodically sampled.*

***AC Characteristics*** *(Supply voltage: +5 V ± 5%; Ambient temperature: 0 °C to 70 °C)*

| | | –50 | | | – 40 | | | –33 | | | –25 | | | –20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ***Symbol*** | ***Description*** | ***Min*** | ***Typ*** | ***Max*** | ***Min*** | ***Typ*** | ***Max*** | ***Min*** | ***Typ*** | ***Max*** | ***Min*** | ***Typ*** | ***Max*** | ***Min*** | ***Typ*** | ***Max*** | ***Unit*** |
| $F_{IN}$ | CLKIN frequency [1] | — | 50 | — | — | 40 | — | — | 33 | — | — | 25 | — | — | 20 | — | MHz |
| $t_{CP}$ | CLKIN period | — | 20 | — | — | 25 | — | — | 30 | — | — | 40 | — | — | 50 | — | ns |
| $t_{CPW}$ | CLKIN pulse width | 5 | 10 | — | 6.25 | 12.5 | — | 7.5 | 15 | — | 10 | 20 | — | 12.5 | 25 | — | ns |
| $t_{IR}$,$t_{IF}$ | Input rise/fall time (20 – 80%) | — | — | 3.0 | — | — | 3.0 | — | — | 3.0 | — | — | 3.0 | — | — | 3.0 | ns |
| $t_{OR}$,$t_{OF}$ | Output rise/fall time (80 – 20%) | — | 1.0 | 3.0 | — | 1.0 | 3.0 | — | 1.0 | 3.0 | — | 1.0 | 3.0 | — | 1.0 | 3.0 | ns |
| $t_R$ | Output rise time (0.8 V to 2.0 V) | — | 0.5 | 1.5 | — | 0.5 | 1.5 | — | 0.5 | 1.5 | — | 0.5 | 1.5 | — | 0.5 | 1.5 | ns |
| $t_{PD}$ | CLKIN Î to FBIN Î [2] | — | ±250 | ±1000 | — | ±250 | ±1000 | — | ±250 | ±1000 | — | ±250 | ±1000 | — | ±250 | ±1000 | ps |
| $t_{SKEW}$ | Output Skew [3] | — | ±250 | ±500 | — | ±250 | ±500 | — | ±250 | ±500 | — | ±250 | ±500 | — | ±250 | ±500 | ps |
| $t_W$ | Output Window [4] | — | 0.5 | 1.0 | — | 0.5 | 1.0 | — | 0.5 | 1.0 | — | 0.5 | 1.0 | — | 0.5 | 1.0 | ns |
| $t_{CYC}$ | Duty-cycle Variation [6] | — | 1.0 | — | — | 1.0 | — | — | 1.0 | — | — | 1.0 | — | — | 1.0 | — | ns |
| $t_{SYNC}$ | Synchronization Time [7] | — | 200 | 500 | — | 200 | 500 | — | 200 | 500 | — | 200 | 500 | — | 200 | 500 | µs |

*Note: All AC specifications are measured with a 75 Ω transmission line load terminated with 75 Ω to 1.5 V. The skew specifications are guaranteed for equal loading at each output.*

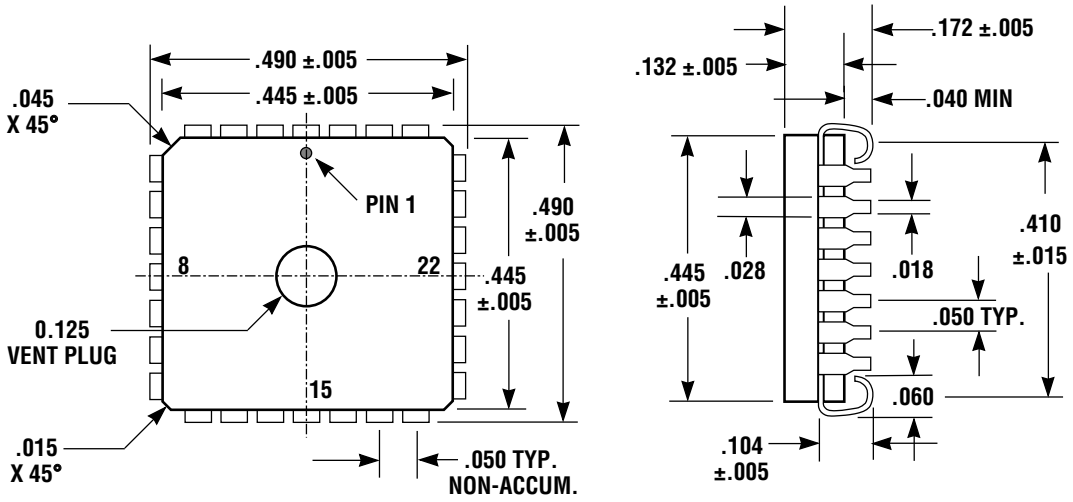
***Figure 7. Switching Waveforms***




*Notes:*
1. *The min, max range on CLKIN frequency is ±5%*
2. *The PLL maintains alignment of CLKIN and FBIN at all times. This specification applies to the rising edge only because the input duty cycle can vary while the output duty cycle is typically 50/50.*
3. *The output skew is measured from the middle of the output window . The maximum skew is guaranteed across all voltages and temperatures.*
4. *$t_W$ specifies the width of the window in which all outputs will switch.*
5. *This specification represents the deviation from 50/50 on the outputs; it is sampled periodically but is not guaranteed.*
6. *$t_{SYNC}$ is the time required for the PLL to synchronize; this assumes the presence of a CLKIN signal and a connection from one of the outputs to FBIN.*
7. *All specifications for inverted outputs apply to the rising edge only.*
8. *The device is AC tested only in the EN2=0, INV1=1 mode.*

### *28-Pin MQuad J-Leaded Package Mechanical Specifications*

*(All dimensions are in inches)*



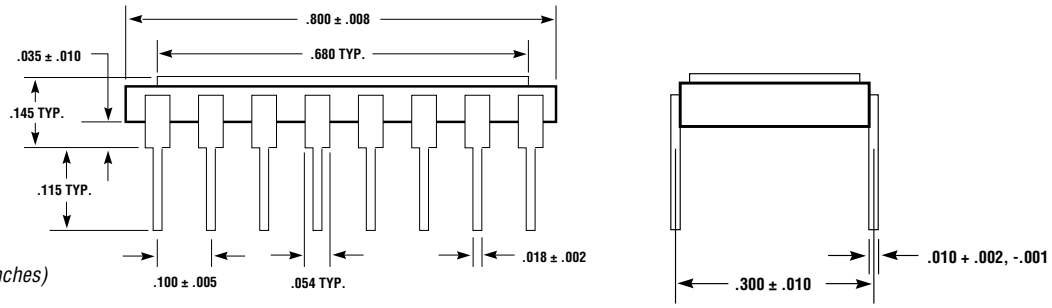

### *28-Pin MQuad Pin Description*

| *Pin #* | *Pin Name* | *Description* | *I/O* |
|---|---|---|---|
| 1 | N/C | No Connect | — |
| 2 | GND | Ground | — |
| 3 | T0 | Test 0 | I [1] |
| 4 | N/C | No Connect | — |
| 5 | N/C | No Connect | — |
| 6 | $\overline{\text{INV1}}$ | Inverted Clocks | I |
| 7 | EN2 | 2-Phase Clocks | I |
| 8 | N/C | No Connect | — |
| 9 | FBIN | Feedback In | I |
| 10 | CLKIN | System Clock | I |
| 11 | N/C | No Connect | — |
| 12 | N/C | No Connect | — |
| 13 | T1 | Test 1 | I [1] |
| 14 | GND | Ground | — |

| *Pin #* | *Pin Name* | *Description* | *I/O* |
|---|---|---|---|
| 15 | N/C | No Connect | — |
| 16 | VDD | +5 V | — |
| 17 | Q0 | Output Clock 0 | O |
| 18 | N/C | No Connect | — |
| 19 | N/C | No Connect | — |
| 20 | Q1 | Output Clock 1 | O |
| 21 | Q2 | Output Clock 2 | O |
| 22 | Q3 | Output Clock 3 | O |
| 23 | Q4 | Output Clock 4 | O |
| 24 | Q5 | Output Clock 5 | O |
| 25 | N/C | No Connect | — |
| 26 | N/C | No Connect | — |
| 27 | VDD | +5 V | — |
| 28 | VDD | +5 V | — |

*Note: 1. For normal operation, T0 is GND and T1 is $V_{DD}$ or N/C (No Connect). For Test Mode, T0 is HIGH and T1 is Clock Pulse(s).*

### 16-Pin DIP Package Mechanical Specifications




*(All dimensions in inches)*

### DIP Pin Descriptions

| Pin # | Pin Name | Description | I/O |
|---|---|---|---|
| 1 | GND | Ground | — |
| 2 | T0 | Test 0 | I [1] |
| 3 | $\overline{INV1}$ | Inverted Clock | I |
| 4 | EN2 | 2-Phase Clocks | I |
| 5 | FBIN | Feedback In | I |
| 6 | CLKIN | System Clock | I |
| 7 | T1 | Test 1 | I [1] |
| 8 | VDD | +5 V | — |

| Pin # | Pin Name | Description | I/O |
|---|---|---|---|
| 9 | GND | Ground | — |
| 10 | Q0 | Output Clock 0 | O |
| 11 | Q1 | Output Clock 1 | O |
| 12 | Q2 | Output Clock 2 | O |
| 13 | Q3 | Output Clock 3 | O |
| 14 | Q4 | Output Clock 4 | O |
| 15 | Q5 | Output Clock 5 | O |
| 16 | VDD | +5 V | — |

*Note: 1. For normal operation, T0 is GND and T1 is $V_{DD}$ or N/C. For Test Mode, T0 is HIGH and T1 is Clock Pulse(s).*

## Ordering Information

To order, please specify as below shown:

**GA1210E – nn P C**

*Input Frequency*

- ***20*** – 20 MHz input
- ***25*** – 25 MHz input
- ***33*** – 33 MHz input
- ***40*** – 40 MHz input
- ***50*** – 50 MHz input

*Temperature*

- ***C*** – Commercial

*Package*

- ***S*** – 16-Pin DIP (side-brazed)
- ***M*** – 28-Pin MQuad Surface-Mount

## Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

**Web: www.triquint.com** **Tel: (503) 615-9000**
**Email: sales@tqs.com** **Fax: (503) 615-8900**

For technical questions and additional information on specific applications:

**Email: applications@tqs.com**



Revision 1.1.A November 1997



TriQuint SEMICONDUCTOR