

**DESCRIPTION**

The '92 is a 4-bit, ripple-type Divide-by-12 Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-six section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset (MR<sub>1</sub>·MR<sub>2</sub>) is provided which overrides both clocks and resets (clears) all the flip-flops.

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT
7492	28MHz	28mA
74LS92	42MHz	9mA

**ORDERING CODE**

PACKAGES	COMMERCIAL RANGE
	$V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7492N, N74LS92N

**NOTE:**

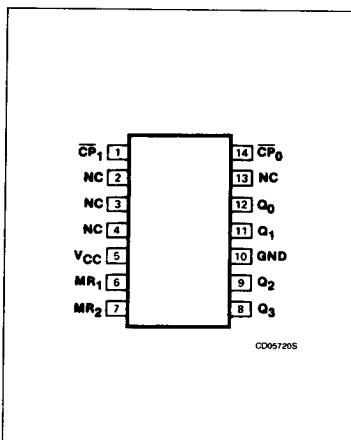
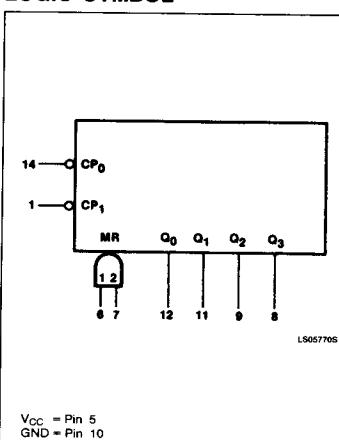
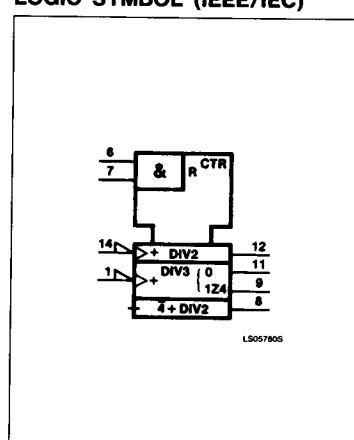
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

**INPUT AND OUTPUT LOADING AND FAN-OUT TABLE**

PINS	DESCRIPTION	74	74LS
MR	Master reset inputs	1 <ul style="list-style-type: none"></ul>	1LS <ul style="list-style-type: none"></ul>
CP <sub>0</sub>	Input	2 <ul style="list-style-type: none"></ul>	6LS <ul style="list-style-type: none"></ul>
CP <sub>1</sub>	Input	4 <ul style="list-style-type: none"></ul>	8LS <ul style="list-style-type: none"></ul>
Q <sub>0</sub> – Q <sub>3</sub>	Outputs	10 <ul style="list-style-type: none"></ul>	10LS <ul style="list-style-type: none"></ul>

**NOTE:**

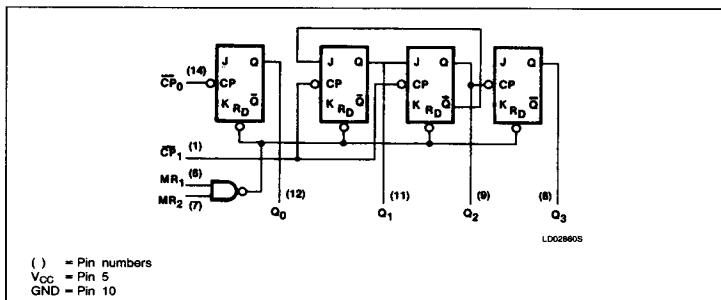
Where a 74 unit load (ul) is understood to be 40 $\mu A$  I<sub>IH</sub> and -1.6mA I<sub>IL</sub>, and a 74LS unit load (LSul) is 20 $\mu A$  I<sub>IH</sub> and -0.4mA I<sub>IL</sub>.

**PIN CONFIGURATION****LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

## Counters

## 7492, LS92

## LOGIC DIAGRAM



Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a Modulo-12, Divide-by-12 Counter the  $\overline{CP}_1$  input must be externally connected to the  $Q_0$  output. The  $\overline{CP}_0$  input receives the incoming count and  $Q_3$  produces a symmetrical divide-by-12 square wave output. In a divide-by-six counter no external connections are required. The first flip-flop is used as a binary element for the divide-by-two function. The  $CP_1$  input is used to obtain divide-by-three operation at the  $Q_1$  and  $Q_2$  outputs and divide-by-six operation at the  $Q_3$  output.

## FUNCTION TABLE

COUNT	OUTPUTS			
	$Q_0$	$Q_1$	$Q_2$	$Q_3$
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

## NOTE:

Output  $Q_0$  connected to input  $\overline{CP}_1$ .

## MODE SELECTION

RESET INPUTS		OUTPUTS			
MR <sub>1</sub>	MR <sub>2</sub>	$Q_0$	$Q_1$	$Q_2$	$Q_3$
H	H	L	L	L	L
L	H				Count
H	L				Count
L	L				Count

H = HIGH voltage level

L = LOW voltage level

X = Don't care

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
	Min	Nom	
$V_{CC}$ Supply voltage	7.0	7.0	V
$V_{IN}$ Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
$I_{IN}$ Input current	-30 to +5	-30 to +1	mA
$V_{OUT}$ Voltage applied to output in HIGH output state	-0.5 to + $V_{CC}$	-0.5 to + $V_{CC}$	V
$T_A$ Operating free-air temperature range	0 to 70		°C

## NOTE:

$V_{IN}$  is limited to 5.5V on  $\overline{CP}_0$  and  $\overline{CP}_1$  inputs only on the 74LS92.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
$V_{CC}$ Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
$V_{IH}$ HIGH-level input voltage	2.0			2.0			V
$V_{IL}$ LOW-level input voltage			+0.8			+0.8	V
$I_{IK}$ Input clamp current			-12			-18	mA
$I_{OH}$ HIGH-level output current			-800			-400	$\mu$ A
$I_{OL}$ LOW-level output current			16			8	mA
$T_A$ Operating free-air temperature	0		70	0		70	°C

## Counters

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## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS <sup>1</sup>	7492			74LS92			UNIT	
		Min	Typ <sup>2</sup>	Max	Min	Typ <sup>2</sup>	Max		
$V_{OH}$ HIGH-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = \text{MIN}$ , $V_{IL} = \text{MAX}$ , $I_{OH} = \text{MAX}$	2.4	3.4		2.7	3.4		V	
$V_{OL}$ LOW-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = \text{MIN}$ , $V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$	0.2	0.4		0.35	0.5	V	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = I_{IK}$			-1.5			-1.5	V	
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5V$	All inputs '92		1.0			mA	
		$V_I = 7.0V$	MR inputs				0.1	mA	
		$V_I = 5.5V$	$\overline{CP}_0$ input				0.2	mA	
			$\overline{CP}_1$ input				0.4	mA	
$I_{IH}$ HIGH-level input current	$V_{CC} = \text{MAX}$	$V_I = 2.4V$	MR inputs		40			$\mu A$	
			$\overline{CP}_0$ input		80			$\mu A$	
			$\overline{CP}_1$ input		160			$\mu A$	
		$V_I = 2.7V$	MR inputs				20	$\mu A$	
			$\overline{CP}_0$ input <sup>5</sup>				40	$\mu A$	
			$\overline{CP}_1$ input <sup>5</sup>				80	$\mu A$	
$I_{IL}$ LOW-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4V$	MR inputs		-1.6		-0.4	mA	
			$\overline{CP}_0$ input		-3.2		-2.4	mA	
			$\overline{CP}_1$ input		-6.4		-3.2	mA	
$I_{OS}$ Short-circuit output current <sup>3</sup>	$V_{CC} = \text{MAX}$		-18		-55	-20		-100	mA
$I_{CC}$ Supply current <sup>4</sup> (total)	$V_{CC} = \text{MAX}$				51		9	15	mA

## NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .
3.  $I_{OS}$  is tested with  $V_{OUT} = +0.5V$  and  $V_{CC} = \text{MAX} + 0.5V$ . Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4.  $I_{CC}$  is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
5. The maximum limit for the 54LS92 only is 80 $\mu A$  for  $\overline{CP}_0$  and 160 $\mu A$  for  $\overline{CP}_1$  inputs.

## Counters

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AC ELECTRICAL CHARACTERISTICS  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ 

PARAMETER	TEST CONDITIONS	74		74LS		UNIT	
		$C_L = 15\text{pF}$ , $R_L = 400\Omega$		$C_L = 15\text{pF}$ , $R_L = 2\text{k}\Omega$			
		Min	Max	Min	Max		
$f_{MAX}$	$\overline{CP}_0$ input count frequency	Waveform 1	10		32	MHz	
$f_{MAX}$	$\overline{CP}_1$ input count frequency	Waveform 1	10		16		
$t_{PLH}$	Propagation delay $\overline{CP}_0$ input to $Q_0$ output	Waveform 1			16	ns	
$t_{PHL}$	Propagation delay $CP_1$ input to $Q_1$ output	Waveform 1			16	ns	
$t_{PLH}$	Propagation delay $CP_1$ input to $Q_2$ output	Waveform 1			16	ns	
$t_{PHL}$	Propagation delay $CP_1$ input to $Q_3$ output	Waveform 1			32	ns	
$t_{PLH}$	Propagation delay $CP_0$ input to $Q_3$ output	Waveform 1		100	48	ns	
$t_{PHL}$	MR input to any output	Waveform 2		100	50	ns	
					40	ns	

## NOTE:

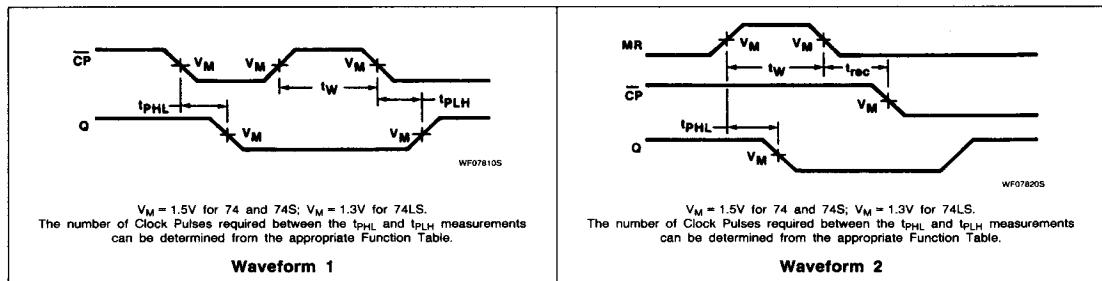
Per industry convention,  $f_{MAX}$  is the worst case value of the maximum device operating frequency with no constraints on  $t_r$ ,  $t_f$ , pulse width or duty cycle.

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AC SET-UP REQUIREMENTS  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ 

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
$t_W$	$\overline{CP}_0$ pulse width	Waveform 1	50		15	ns
$t_W$	$\overline{CP}_1$ pulse width	Waveform 1	50		30	ns
$t_W$	MR pulse width	Waveform 2	50		15	ns
$t_{rec}$	Recovery time, MR to $\overline{CP}$	Waveform 2			25	ns

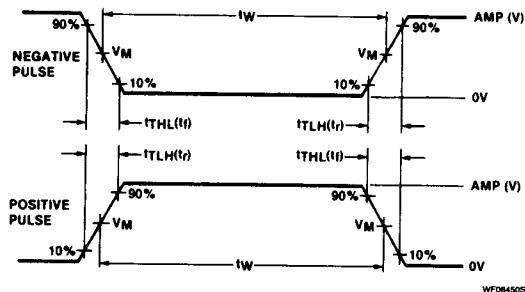
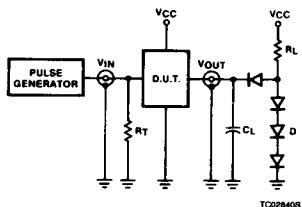
## AC WAVEFORMS



## Counters

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## TEST CIRCUITS AND WAVEFORMS



VM = 1.3V for 74LS; VM = 1.5V for all other TTL families.

## Test Circuit For 74 Totem-Pole Outputs

## DEFINITIONS

$R_L$  = Load resistor to  $V_{CC}$ ; see AC CHARACTERISTICS for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$t_{TLH}$ ,  $t_{THL}$  Values should be less than or equal to the table entries.

## Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	$t_{TLH}$	$t_{THL}$
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns