

DATA SHEET

74ABT16827A

74ABTH16827A

20-bit buffer/line driver, non-inverting
(3-State)

Product specification
Supersedes data of 1998 Feb 27

2002 Dec 17

20-bit buffer/line driver, non-inverting (3-State)

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FEATURES

- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- 3-State output buffers
- Power-up 3-State
- 74ABTH16827A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64 mA / –32 mA
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16827A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16827A 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($\overline{nOE1}$, $\overline{nOE2}$) for maximum control flexibility.

Two options are available, 74ABT16827A which does not have the bus-hold feature and 74ABTH16827A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25\text{ }^{\circ}\text{C}$; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	$C_L = 50\text{ pF}$; $V_{CC} = 5\text{ V}$	1.7 1.4	ns
C_{IN}	Input capacitance	$V_I = 0\text{ V}$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	$V_O = 0\text{ V}$ or V_{CC} ; 3-State	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{ V}$	500	μA
I_{CCL}		Outputs LOW; $V_{CC} = 5.5\text{ V}$	9	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	PART NUMBER	DWG NUMBER
56-Pin Plastic SSOP Type III	–40 °C to +85 °C	74ABT16827ADL	SOT371-1
56-Pin Plastic TSSOP Type II	–40 °C to +85 °C	74ABT16827ADGG	SOT364-1
56-Pin Plastic TSSOP Type II	–40 °C to +85 °C	74ABTH16827ADGG	SOT364-1

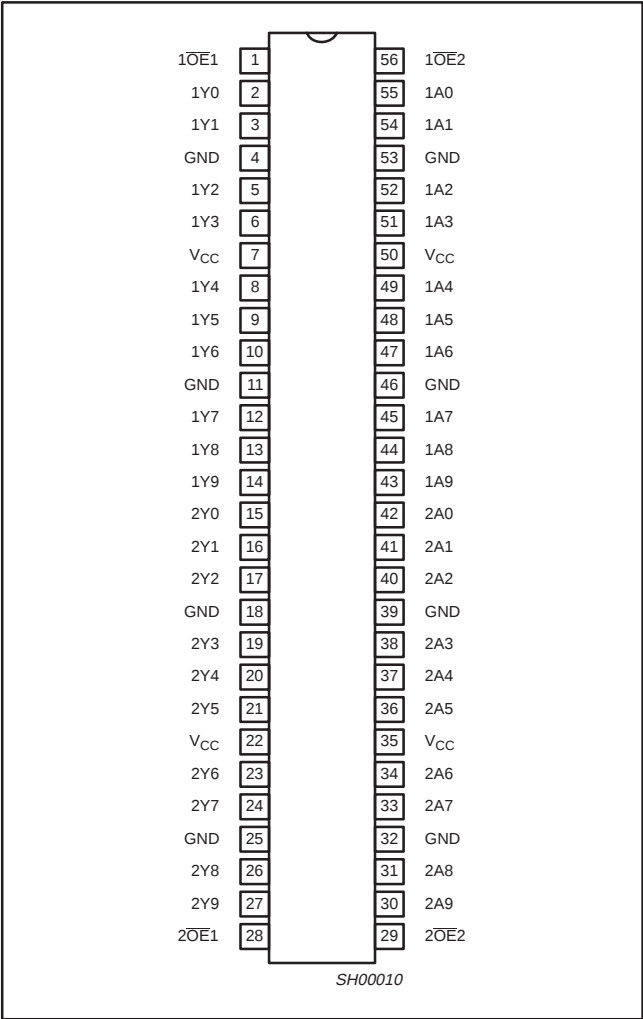
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1A0 – 1A9 2A0 – 2A9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Y0 – 1Y9 2Y0 – 2Y9	Data outputs
1, 56, 28, 29	$\overline{1OE0}$, $\overline{1OE1}$ $\overline{2OE0}$, $\overline{2OE1}$	Output enable inputs (active-LOW)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0 V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

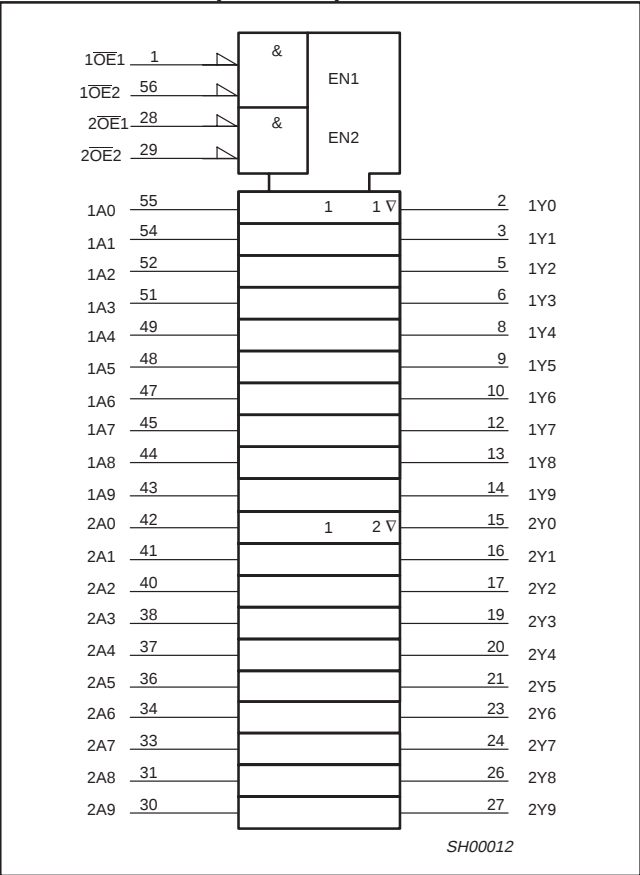
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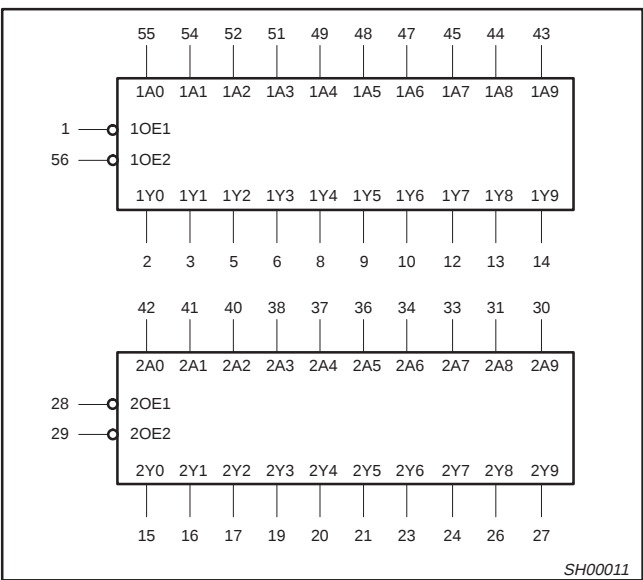
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTION TABLE

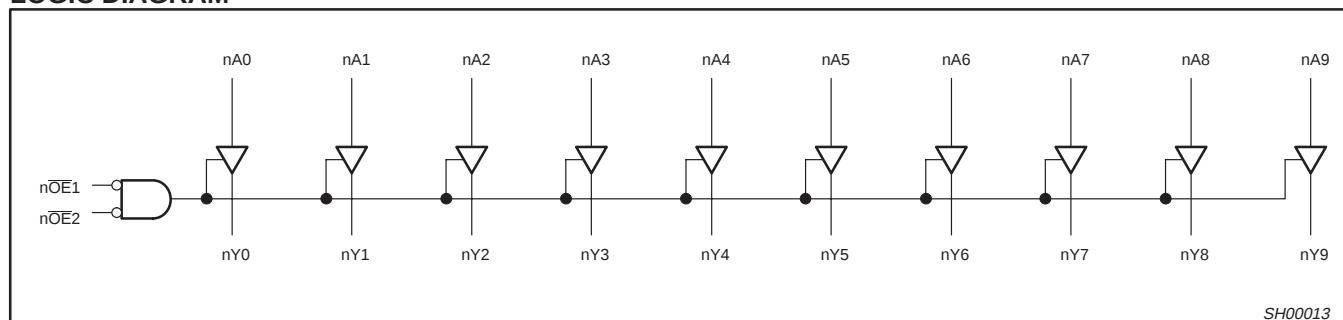
INPUTS		OUTPUTS	OPERATING MODE
nOE _x	nA _x	nY _x	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

X = Don't care
Z = High impedance "off" state
H = HIGH voltage level
L = LOW voltage level

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LOGIC DIAGRAM

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$ V	-18	mA
V_I	DC input voltage ³		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	-50	mA
V_{OUT}	DC output voltage ³	Output in Off or HIGH state	-0.5 to +5.5	V
I_{OUT}	DC output current	Output in LOW state	128	mA
		Output in HIGH state	-64	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0	—	V
V_{IL}	LOW-level Input voltage	—	0.8	V
I_{OH}	HIGH-level output current	—	-32	mA
I_{OL}	LOW-level output current	—	64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T _{amb} = +25 °C			T _{amb} = −40 °C to +85 °C		
				MIN	TYP	MAX	MIN	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 4.5 V; I _{IK} = −18 mA			−0.9	−1.2		−1.2	V
V _{OH}	HIGH-level output voltage	V _{CC} = 4.5 V; I _{OH} = −3 mA; V _I = V _{IL} or V _{IH}		2.5	2.9		2.5		V
		V _{CC} = 5.0 V; I _{OH} = −3 mA; V _I = V _{IL} or V _{IH}		3.0	3.4		3.0		V
		V _{CC} = 4.5 V; I _{OH} = −32 mA; V _I = V _{IL} or V _{IH}		2.0	2.4		2.0		V
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; I _{OL} = 64 mA; V _I = V _{IL} or V _{IH}			0.42	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5 V; V _I = GND or 5.5 V			±0.01	±1.0		±1.0	μA
I _I	Input leakage current 74ABTH16827A	V _{CC} = 5.5 V; V _I = 5.5 V			0.01	1		1	μA
		V _{CC} = 5.5 V; V _I = V _{CC} or GND	Control pins		±0.01	±1		±1	μA
		V _{CC} = 5.5 V; V _I = V _{CC}	Data pins ⁴		0.01	1		1	μA
		V _{CC} = 5.5 V; V _I = 0			−1	−3		−5	μA
I _{HOLD}	Bus Hold current A inputs ⁵ 74ABTH16827A	V _{CC} = 4.5 V; V _I = 0.8 V		35			35		μA
		V _{CC} = 4.5 V; V _I = 2.0 V		−75			−75		
		V _{CC} = 5.5 V; V _I = 0 to 5.5 V		±800					
I _{OFF}	Power-off leakage current	V _{CC} = 0.0 V; V _O = 4.5 V; V _I = 0 V or 5.5 V			±5.0	±100		±100	μA
I _{PU} /I _{PD}	Power-up/down 3-State output current ³	V _{CC} = 2.1 V; V _O = 0.5 V; V _I = GND or V _{CC} ; V _{OE} = Don't care			±5.0	±50		±50	μA
I _{OZH}	3-State output High current	V _{CC} = 5.5 V; V _O = 2.7 V; V _I = V _{IL} or V _{IH}			1.0	10		10	μA
I _{OZL}	3-State output Low current	V _{CC} = 5.5 V; V _O = 0.5 V; V _I = V _{IL} or V _{IH}			−1.0	−10		−10	μA
I _{CEX}	Output HIGH leakage current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC}			1.0	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5 V; V _O = 2.5 V		−50	−70	−180	−50	−180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5 V; Outputs HIGH, V _I = GND or V _{CC}			0.5	1		1	mA
I _{CCL}		V _{CC} = 5.5 V; Outputs LOW, V _I = GND or V _{CC}			9	19		19	mA
I _{CCZ}		V _{CC} = 5.5 V; Outputs 3-State; V _I = GND or V _{CC}			0.5	1		1	mA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5 V; one input at 3.4 V, other inputs at V _{CC} or GND			0.2	1		1	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4 V .
- This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 msec . From $V_{CC} = 2.1\text{ V}$ to $V_{CC} = 5\text{ V} \pm 10\%$ a transition time of up to $100\text{ }\mu\text{sec}$ is permitted.
- Unused pins at V_{CC} or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

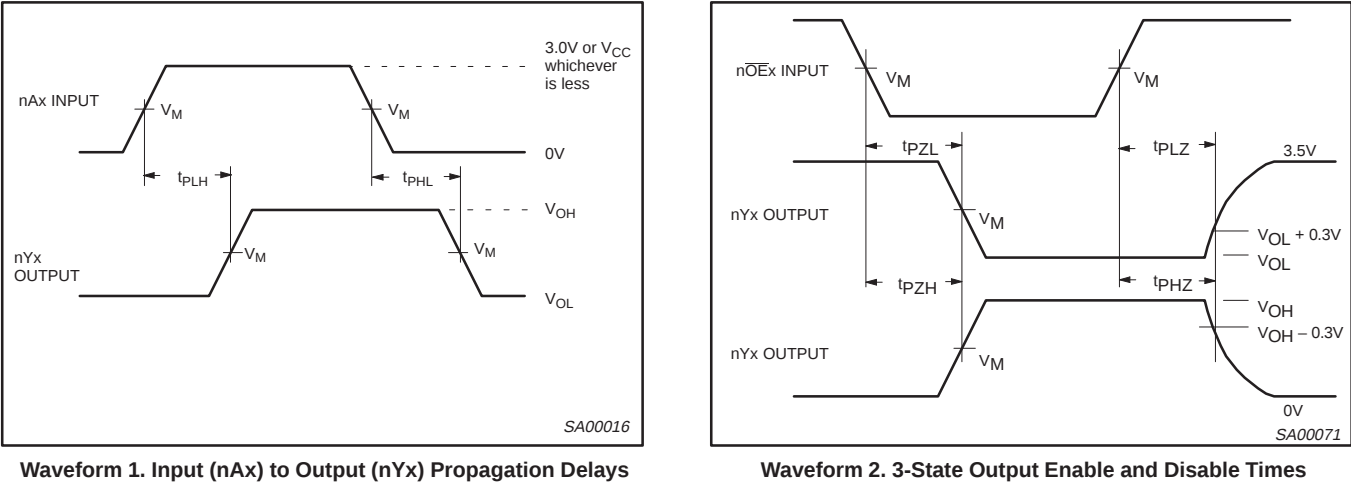
GND = 0 V, $t_R = t_F = 2.5\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 500\text{ }\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25 °C V _{CC} = +5.0 V			T _{amb} = −40 °C to +85 °C V _{CC} = +5.0 V ±0.5 V		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay nAx to nYx	1	1.0 0.6	1.7 1.4	2.4 2.0	1.0 0.6	2.7 2.3	ns
t _{PZH} t _{PZL}	Output enable time to HIGH and LOW level	2	1.0 1.0	3.0 3.0	4.1 4.0	1.0 1.0	5.0 5.0	ns
t _{PHZ} t _{PLZ}	Output disable time from HIGH and LOW level	2	2.0 1.6	3.2 2.4	4.3 3.2	2.0 1.6	5.0 3.5	ns

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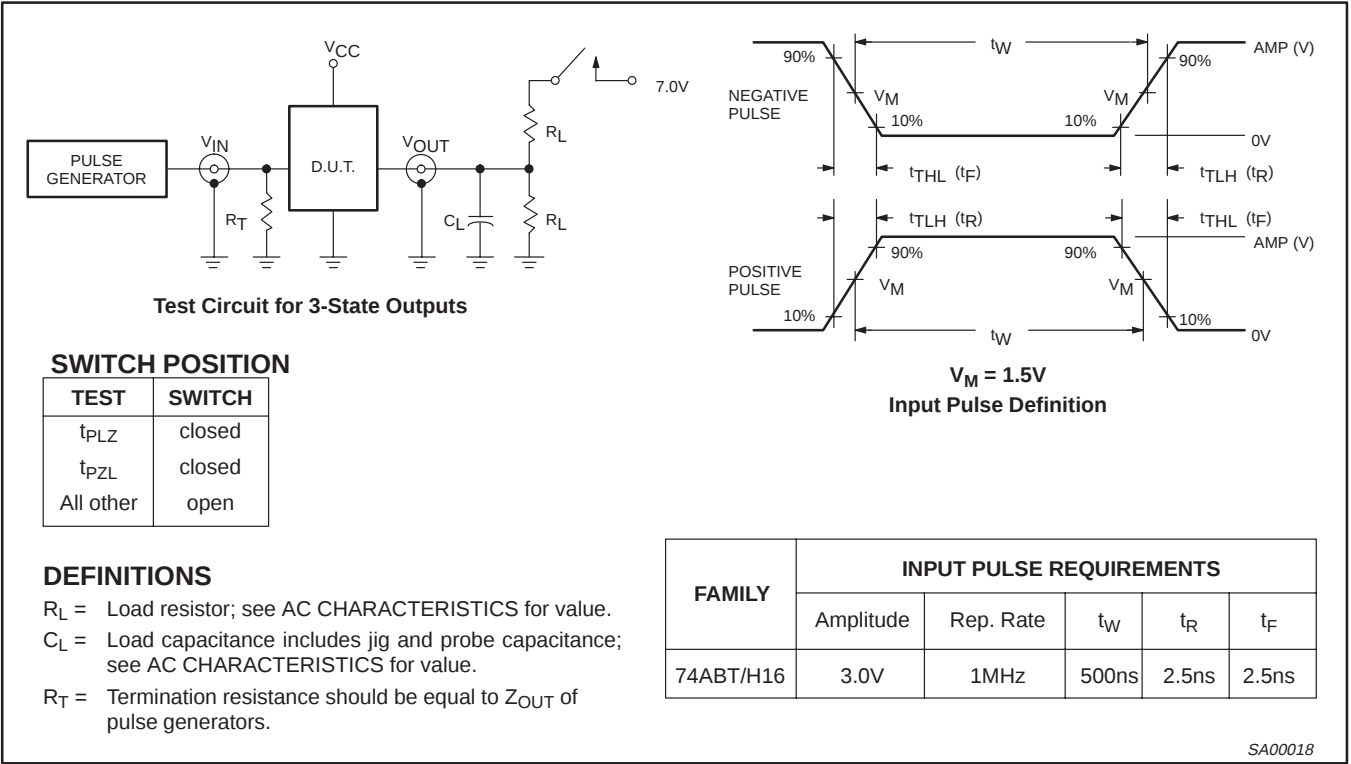
AC WAVEFORMS



Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



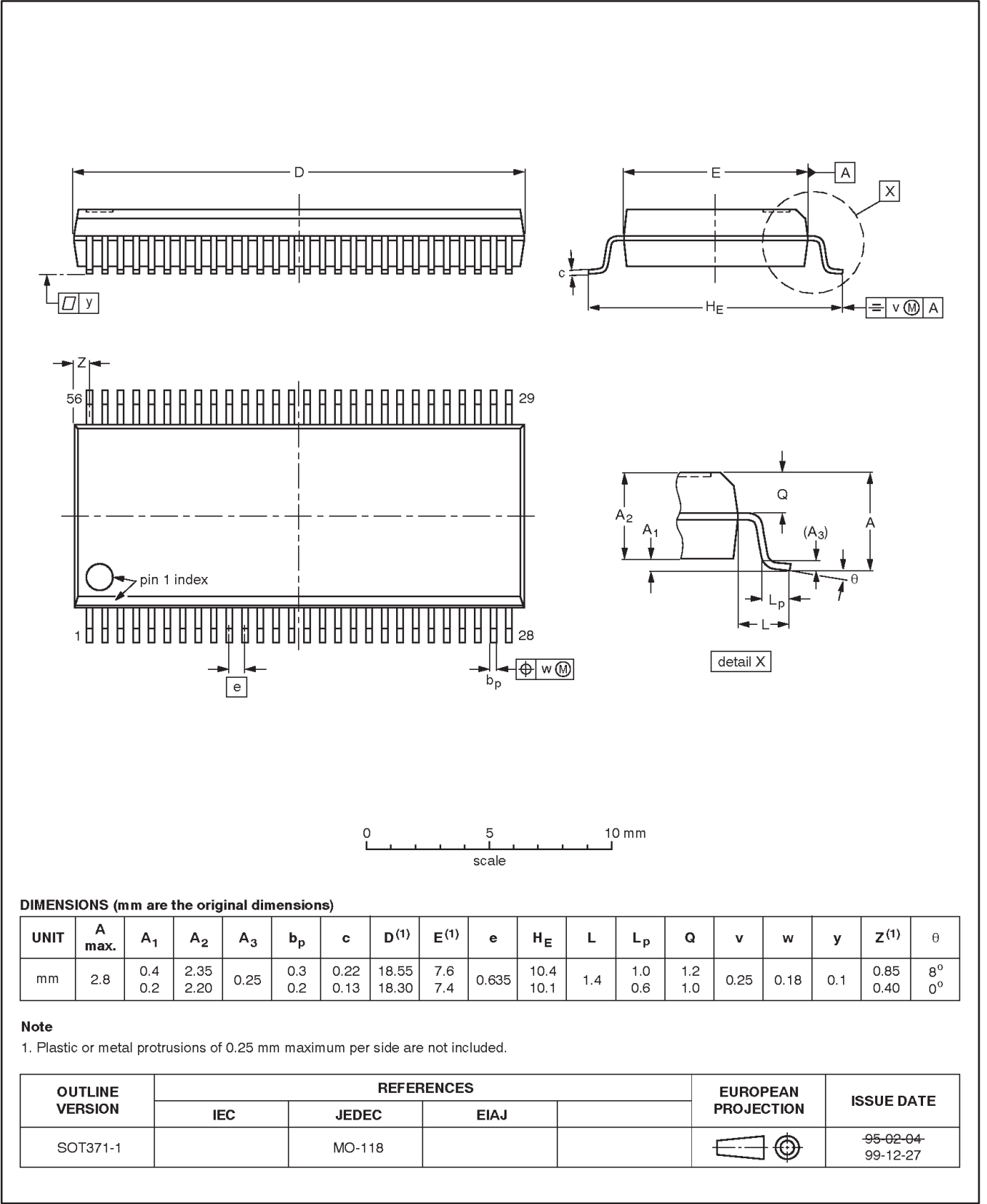
SA00018

20-bit buffer/line driver, non-inverting (3-State)

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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

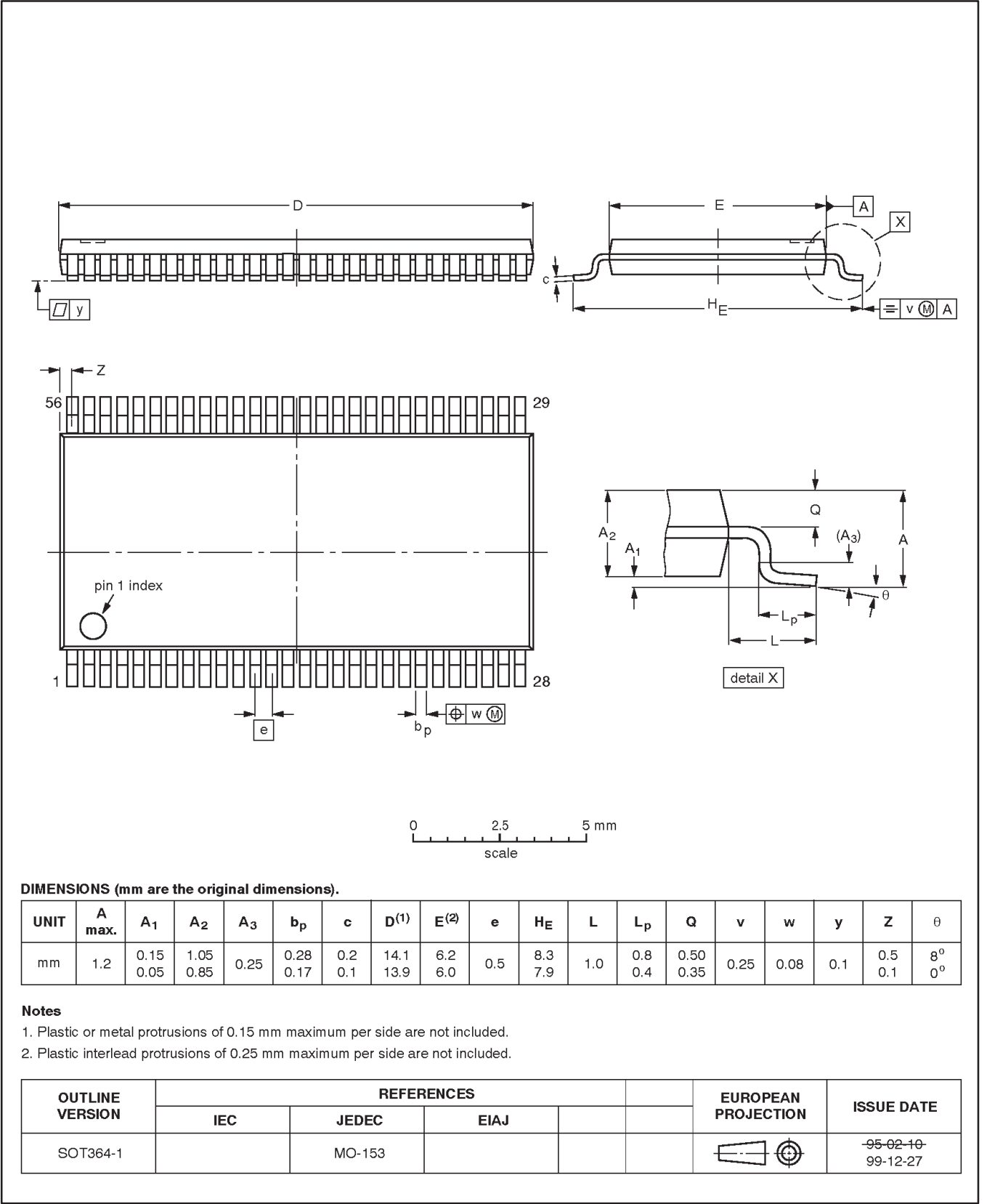


20-bit buffer/line driver, non-inverting (3-State)

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



20-bit buffer/line driver, non-inverting (3-State)74ABT16827A
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REVISION HISTORY

Rev	Date	Description
_2	20021217	Product data (9397 750 10858); ECN 853-1824 29295 of 12 December 2002. Supersedes data of 27 February 1998 (9397 750 03504). Modifications: ● Ordering information table: remove "North America" column; remove 74ABTH16827ADL package offering.
_1	19980227	Product specification (9397 750 03504). ECN 853-1824 19025 of 27 February 1998.

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Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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