

- Local Bus-Latch Capability
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, and Standard Plastic 300-mil DIPs

#### description

These octal bus transceivers are designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the output-enable (OEAB or  $\overline{OEBA}$ ) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of OEAB and  $\overline{OEBA}$ . Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be complementary for the 74AC11623.

The 74AC11623 is characterized for operation from –40°C to 85°C.

DW OR NT PACKAGE (TOP VIEW)		
A1	1	24
A2	2	23
A3	3	22
A4	4	21
GND	5	20
GND	6	19
GND	7	18
GND	8	17
A5	9	16
A6	10	15
A7	11	14
A8	12	13
		OEAB
		B1
		B2
		B3
		B4
		$V_{CC}$
		$V_{CC}$
		B5
		B6
		B7
		B8
		OEBA

FUNCTION TABLE

INPUTS		OPERATION
OEBA	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

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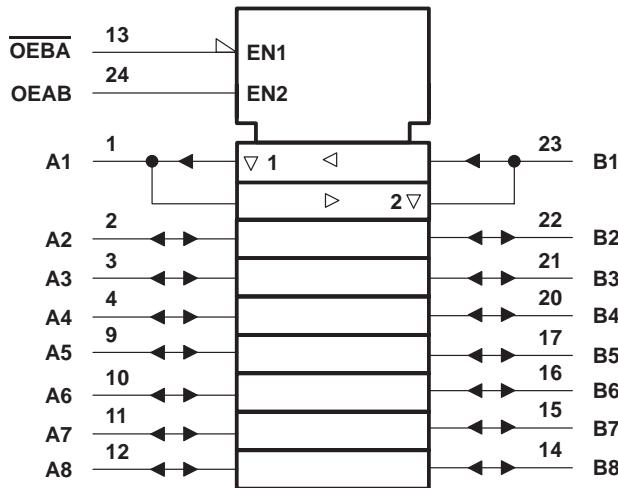
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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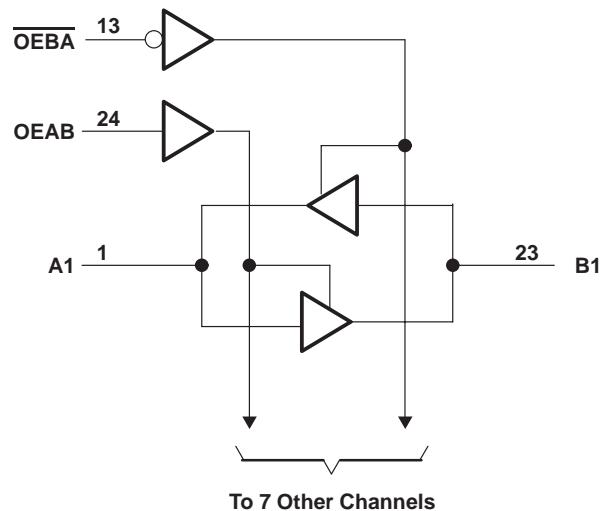


**74AC11623**  
**OCTAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**  
SCAS058A – JULY 1987 – REVISED APRIL 1993

**logic symbol†**



**logic diagram (positive logic)**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±50 mA
Continuous current through $V_{CC}$ or GND pins .....	±200 mA
Storage temperature range .....	–65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

**recommended operating conditions**

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		3	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3 V	2.1			V
		V <sub>CC</sub> = 4.5 V	3.15			
		V <sub>CC</sub> = 5.5 V	3.85			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9		V
		V <sub>CC</sub> = 4.5 V		1.35		
		V <sub>CC</sub> = 5.5 V		1.65		
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>		V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3 V		–4		mA
		V <sub>CC</sub> = 4.5 V		–24		
		V <sub>CC</sub> = 5.5 V		–24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3 V		12		mA
		V <sub>CC</sub> = 4.5 V		24		
		V <sub>CC</sub> = 5.5 V		24		
Δt/Δv	Input transition rise or fall rate		0	10	ns/V	
T <sub>A</sub>	Operating free-air temperature		–40	85	°C	

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			UNIT
			MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	3 V	2.9		2.9	V
		4.5 V	4.4		4.4	
		5.5 V	5.4		5.4	
	I <sub>OH</sub> = –4 mA	3 V	2.58		2.48	
	I <sub>OH</sub> = –24 mA	4.5 V	3.94		3.8	
		5.5 V	4.94		4.8	
V <sub>OL</sub>	I <sub>OH</sub> = –75 mA†	5.5 V			3.85	V
	I <sub>OL</sub> = 50 μA	3 V	0.1		0.1	
		4.5 V	0.1		0.1	
		5.5 V	0.1		0.1	
	I <sub>OL</sub> = 12 mA	3 V	0.36		0.44	
	I <sub>OL</sub> = 24 mA	4.5 V	0.36		0.44	
		5.5 V	0.36		0.44	
I <sub>I</sub>	I <sub>OL</sub> = 75 mA†	5.5 V			1.65	μA
	OEBA or OEAB	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		±0.1	
	I <sub>OZ</sub> ‡	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V	±0.5	
	I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND,	I <sub>O</sub> = 0	5.5 V	8	
	C <sub>i</sub>	OEBA or OEAB	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	4	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V	12		pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

74AC11623

OCTAL BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A or B	B or A	1.5	6.8	9.2	1.5	10.5	ns
$t_{PHL}$			1.5	6.3	8.2	1.5	9.3	
$t_{PZH}$	OEBA	A	1.5	8	10.6	1.5	12.2	ns
$t_{PZL}$			1.5	7.9	10.4	1.5	11.6	
$t_{PHZ}$	OEBA	A	1.5	7	8.7	1.5	9.3	ns
$t_{PLZ}$			1.5	8	9.9	1.5	10.7	
$t_{PZH}$	OEAB	B	1.5	8.2	10.4	1.5	12	ns
$t_{PZL}$			1.5	8.3	10.8	1.5	12.2	
$t_{PHZ}$	OEAB	B	1.5	7	8.8	1.5	9.4	ns
$t_{PLZ}$			1.5	8	9.9	1.5	10.6	

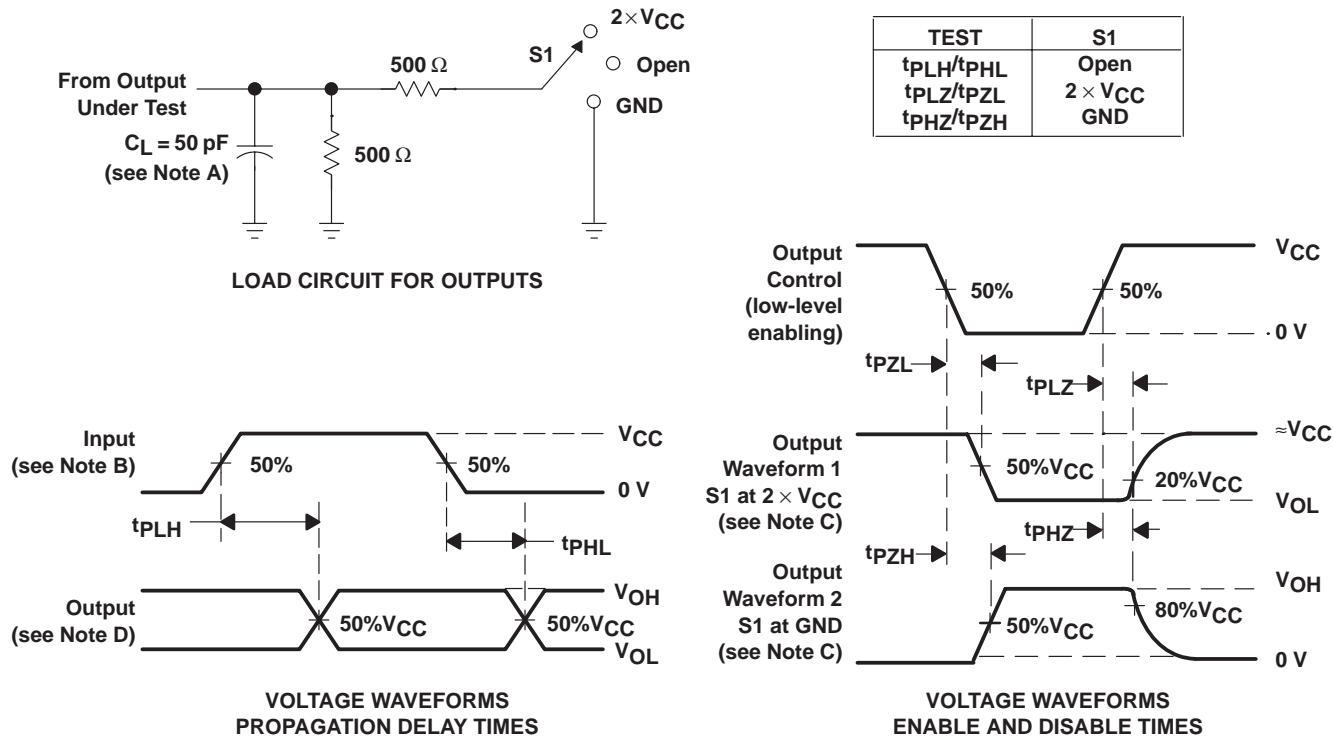
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A or B	B or A	1.5	4.9	6.8	1.5	7.8	ns
$t_{PHL}$			1.5	4.6	6.4	1.5	7.1	
$t_{PZH}$	OEBA	A	1.5	5.8	7.9	1.5	9	ns
$t_{PZL}$			1.5	5.9	8.1	1.5	9.1	
$t_{PHZ}$	OEBA	A	1.5	6.1	7.7	1.5	8.3	ns
$t_{PLZ}$			1.5	6.6	8.2	1.5	8.8	
$t_{PZH}$	OEAB	B	1.5	6.2	8	1.5	9.2	ns
$t_{PZL}$			1.5	6.1	8.3	1.5	9.4	
$t_{PHZ}$	OEAB	B	1.5	6.2	7.8	1.5	8.3	ns
$t_{PLZ}$			1.5	6.5	8.1	1.5	8.8	

operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50 \text{ pF}$ , $f = 1 \text{ MHz}$	49	pF
		Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .  
For testing pulse duration:  $t_r = t_f = 1$  to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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