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April 1, 2003

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# TBB1004

Twin Build in Biasing Circuit MOS FET IC  
VHF/UHF RF Amplifier



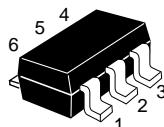
ADE-208-988H (Z)  
9th. Edition  
Dec. 2000

## Features

- Small SMD package CMPAK-6 built in twin BBFET; To reduce using parts cost & PC board space.
- Suitable for World Standard Tuner RF amplifier.
- Very useful for total tuner cost reduction.
- Withstanding to ESD; Build in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; CMPAK-6

## Outline

CMPAK-6



1. Drain(1)
2. Source
3. Gate-1(1)
4. Gate-1(2)
5. Gate-2
6. Drain(2)

Notes: 1. Marking is "DM".  
2. TBB1004 is individual type number of HITACHI TWIN BBFET.

**Absolute Maximum Ratings (Ta = 25°C)**

| Item                      | Symbol           | Ratings     | Unit |
|---------------------------|------------------|-------------|------|
| Drain to source voltage   | V <sub>DS</sub>  | 6           | V    |
| Gate1 to source voltage   | V <sub>G1S</sub> | +6<br>-0    | V    |
| Gate2 to source voltage   | V <sub>G2S</sub> | +6<br>-0    | V    |
| Drain current             | I <sub>D</sub>   | 30          | mA   |
| Channel power dissipation | Pch <sup>3</sup> | 250         | mW   |
| Channel temperature       | T <sub>ch</sub>  | 150         | °C   |
| Storage temperature       | T <sub>stg</sub> | -55 to +150 | °C   |

Notes: 3. Value on the glass epoxy board (49mm × 38mm × 1mm).

**Electrical Characteristics (Ta = 25°C)**

The below specification are applicable for UHF unit (FET1)

| Item                              | Symbol                | Min | Typ  | Max  | Unit | Test Conditions   |
|-----------------------------------|-----------------------|-----|------|------|------|---|
| Drain to source breakdown voltage | V <sub>(BR)DSS</sub>  | 6   | —    | —    | V    | I <sub>D</sub> = 200μA, V <sub>G1S</sub> = V <sub>G2S</sub> = 0   |
| Gate1 to source breakdown voltage | V <sub>(BR)G1SS</sub> | +6  | —    | —    | V    | I <sub>G1</sub> = +10μA, V <sub>G2S</sub> = V <sub>DS</sub> = 0   |
| Gate2 to source breakdown voltage | V <sub>(BR)G2SS</sub> | +6  | —    | —    | V    | I <sub>G2</sub> = +10μA, V <sub>G1S</sub> = V <sub>DS</sub> = 0   |
| Gate1 to source cutoff current    | I <sub>G1SS</sub>     | —   | —    | +100 | nA   | V <sub>G1S</sub> = +5V, V <sub>G2S</sub> = V <sub>DS</sub> = 0  |
| Gate2 to source cutoff current    | I <sub>G2SS</sub>     | —   | —    | +100 | nA   | V <sub>G2S</sub> = +5V, V <sub>G1S</sub> = V <sub>DS</sub> = 0  |
| Gate1 to source cutoff voltage    | V <sub>G1S(off)</sub> | 0.5 | 0.7  | 1.0  | V    | V <sub>DS</sub> = 5V, V <sub>G2S</sub> = 4V, I <sub>D</sub> = 100μA   |
| Gate2 to source cutoff voltage    | V <sub>G2S(off)</sub> | 0.5 | 0.7  | 1.0  | V    | V <sub>DS</sub> = 5V, V <sub>G1S</sub> = 5V, I <sub>D</sub> = 100μA   |
| Drain current                     | I <sub>D(op)</sub>    | 13  | 17   | 21   | mA   | V <sub>DS</sub> = 5V, V <sub>G1</sub> = 5V<br>V <sub>G2S</sub> = 4V, R <sub>G</sub> = 100kΩ   |
| Forward transfer admittance       | y <sub>fs</sub>       | 21  | 26   | 31   | mS   | V <sub>DS</sub> = 5V, V <sub>G1</sub> = 5V, V <sub>G2S</sub> = 4V<br>R <sub>G</sub> = 100kΩ, f = 1kHz   |
| Input capacitance                 | C <sub>iss</sub>      | 1.4 | 1.8  | 2.2  | pF   | V <sub>DS</sub> = 5V, V <sub>G1</sub> = 5V  |
| Output capacitance                | C <sub>oss</sub>      | 1.0 | 1.4  | 1.8  | pF   | V <sub>G2S</sub> = 4V, R <sub>G</sub> = 100kΩ   |
| Reverse transfer capacitance      | C <sub>rss</sub>      | —   | 0.02 | 0.04 | pF   | f = 1MHz  |
| Power gain                        | PG                    | 16  | 21   | —    | dB   | V <sub>DS</sub> = V <sub>G1</sub> = 5V, V <sub>G2S</sub> = 4V<br>R <sub>G</sub> = 100kΩ, f = 900MHz<br>Z <sub>i</sub> =S11*, Z <sub>o</sub> =S22*(PG) |
| Noise figure                      | NF                    | —   | 1.7  | 2.5  | dB   | Z <sub>i</sub> =S11opt (NF)   |

## Electrical Characteristics (Ta = 25°C)

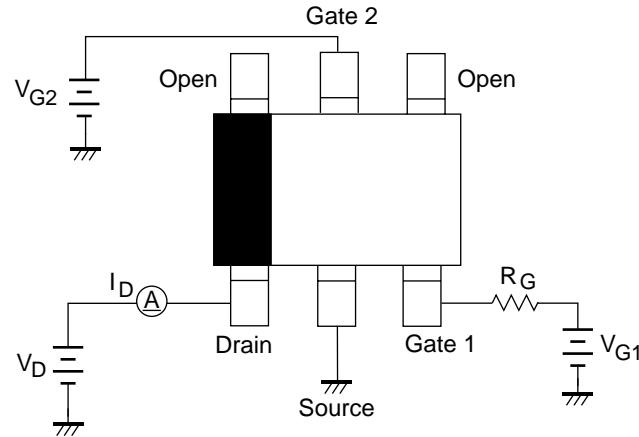
The below specification are applicable for VHF unit (FET2)

| Item                              | Symbol                | Min | Typ  | Max  | Unit | Test Conditions   |
|-----------------------------------|-----------------------|-----|------|------|------|---|
| Drain to source breakdown voltage | V <sub>(BR)DSS</sub>  | 6   | —    | —    | V    | I <sub>D</sub> = 200μA, V <sub>G1S</sub> = V <sub>G2S</sub> = 0                                       |
| Gate1 to source breakdown voltage | V <sub>(BR)G1SS</sub> | +6  | —    | —    | V    | I <sub>G1</sub> = +10μA, V <sub>G2S</sub> = V <sub>DS</sub> = 0                                       |
| Gate2 to source breakdown voltage | V <sub>(BR)G2SS</sub> | +6  | —    | —    | V    | I <sub>G2</sub> = +10μA, V <sub>G1S</sub> = V <sub>DS</sub> = 0                                       |
| Gate1 to source cutoff current    | I <sub>G1SS</sub>     | —   | —    | +100 | nA   | V <sub>G1S</sub> = +5V, V <sub>G2S</sub> = V <sub>DS</sub> = 0  |
| Gate2 to source cutoff current    | I <sub>G2SS</sub>     | —   | —    | +100 | nA   | V <sub>G2S</sub> = +5V, V <sub>G1S</sub> = V <sub>DS</sub> = 0  |
| Gate1 to source cutoff voltage    | V <sub>G1S(off)</sub> | 0.5 | 0.75 | 1.0  | V    | V <sub>DS</sub> = 5V, V <sub>G2S</sub> = 4V, I <sub>D</sub> = 100μA                                   |
| Gate2 to source cutoff voltage    | V <sub>G2S(off)</sub> | 0.5 | 0.75 | 1.0  | V    | V <sub>DS</sub> = 5V, V <sub>G1S</sub> = 5V, I <sub>D</sub> = 100μA                                   |
| Drain current                     | I <sub>D(op)</sub>    | 16  | 20   | 24   | mA   | V <sub>DS</sub> = 5V, V <sub>G1</sub> = 5V, V <sub>G2S</sub> = 4V, R <sub>G</sub> = 100kΩ             |
| Forward transfer admittance       | y <sub>fs</sub>       | 27  | 32   | 37   | mS   | V <sub>DS</sub> = 5V, V <sub>G1</sub> = 5V, V <sub>G2S</sub> = 4V<br>R <sub>G</sub> = 100kΩ, f = 1kHz |
| Input capacitance                 | C <sub>iss</sub>      | 2.3 | 2.7  | 3.1  | pF   | V <sub>DS</sub> = 5V, V <sub>G1</sub> = 5V  |
| Output capacitance                | C <sub>oss</sub>      | 1.4 | 1.8  | 2.2  | pF   | V <sub>G2S</sub> = 4V, R <sub>G</sub> = 100kΩ   |
| Reverse transfer capacitance      | C <sub>rss</sub>      | —   | 0.03 | 0.05 | pF   | f = 1MHz  |
| Power gain                        | PG                    | 24  | 29   | —    | dB   | V <sub>DS</sub> = V <sub>G1</sub> = 5V, V <sub>G2S</sub> = 4V   |
| Noise figure                      | NF                    | —   | 1.2  | 1.7  | dB   | R <sub>G</sub> = 100kΩ, f = 200MHz  |

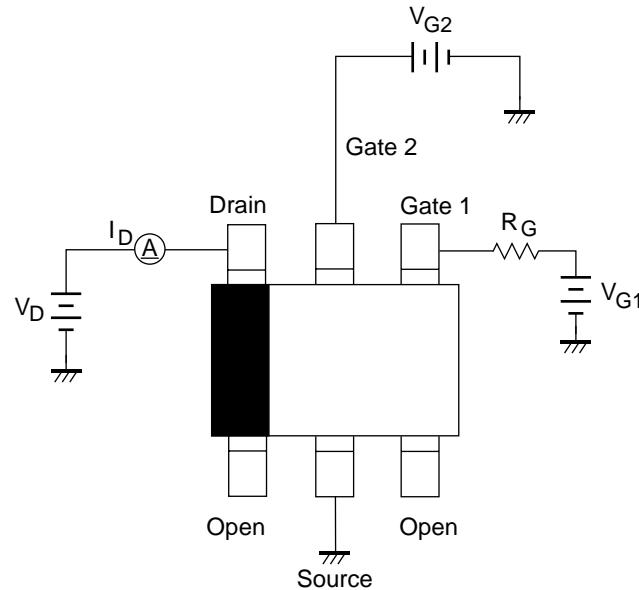
## Test Circuits

- DC Biasing Circuit for Operating Characteristic Items ( $I_{D(\text{op})}$ ,  $|y_{fs}|$ ,  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$ , NF, PG)

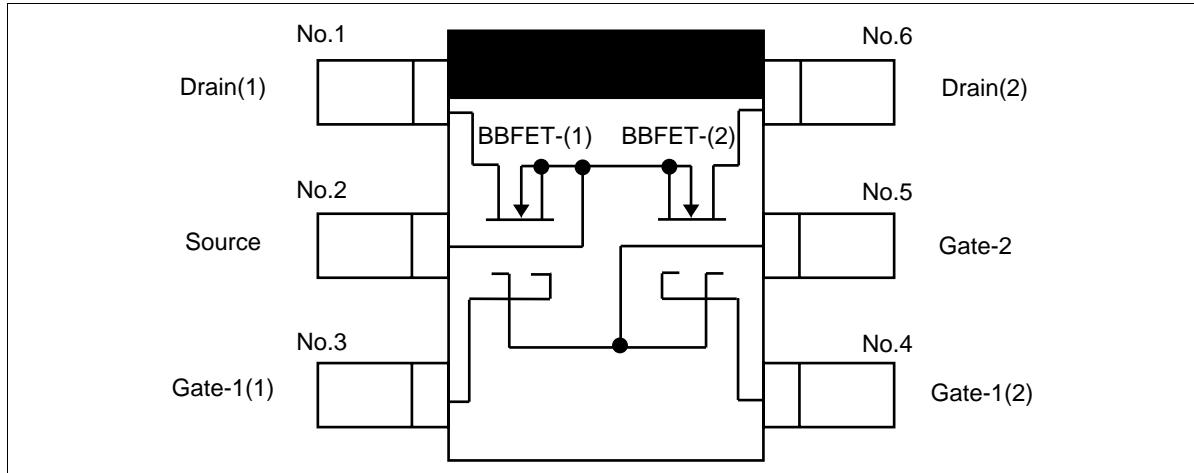
Measurment of FET1



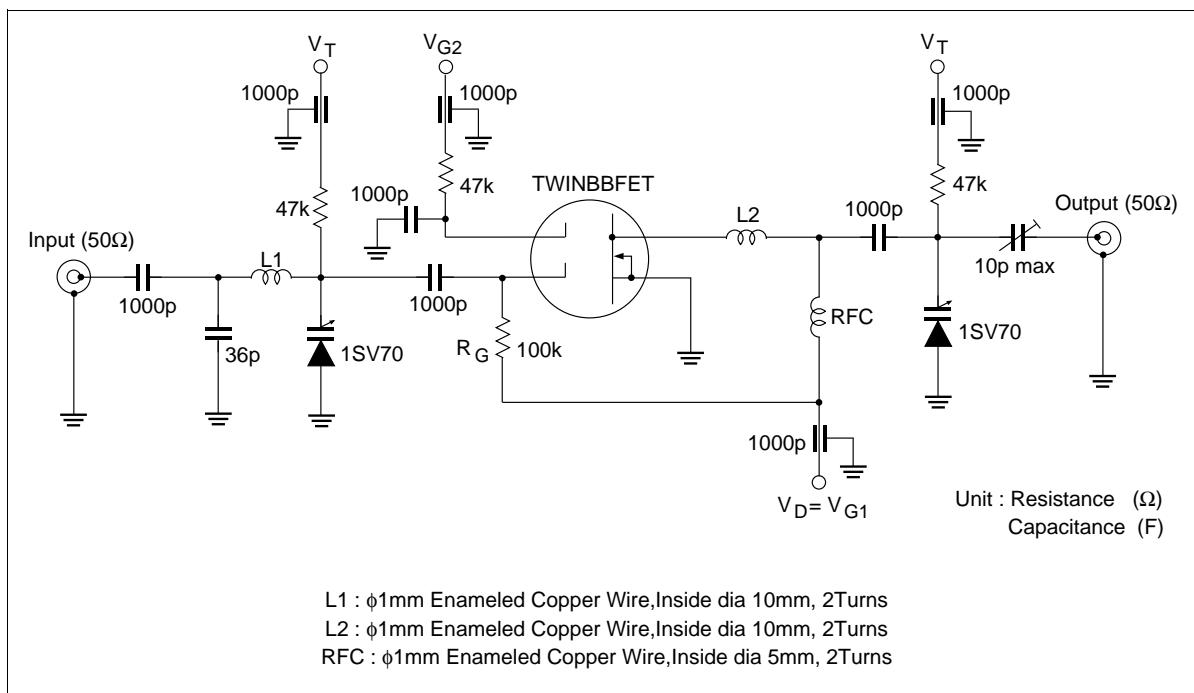
Measurment of FET2

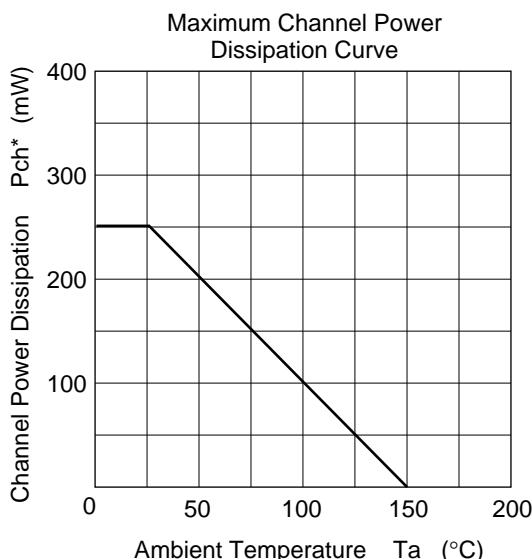


- **Equivalent Circuit**

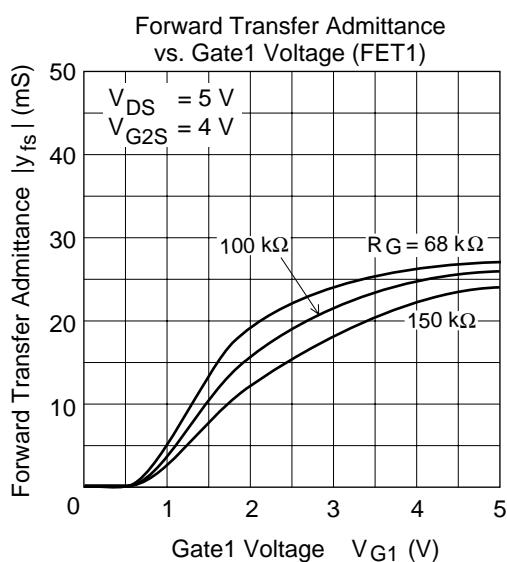
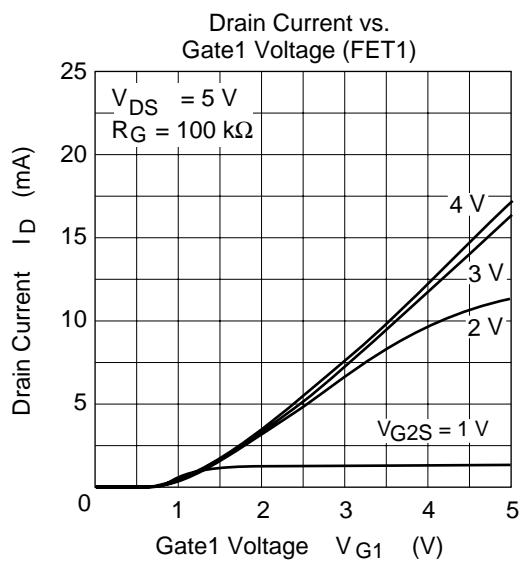
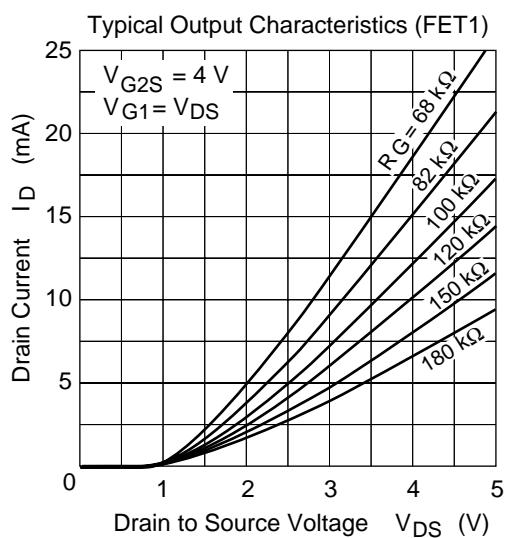


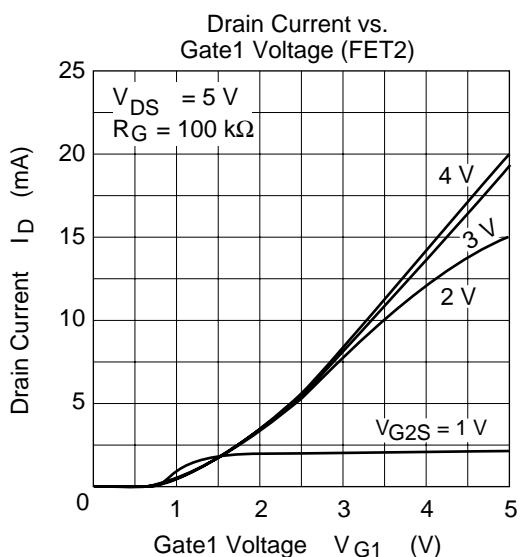
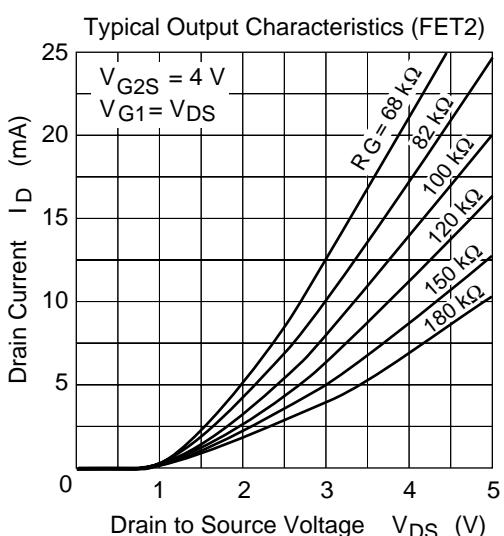
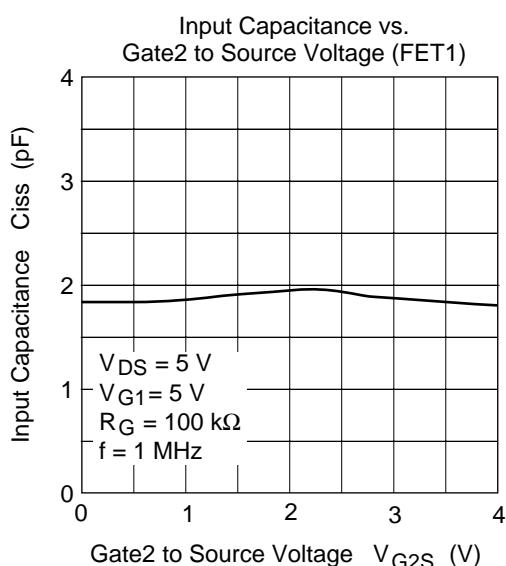
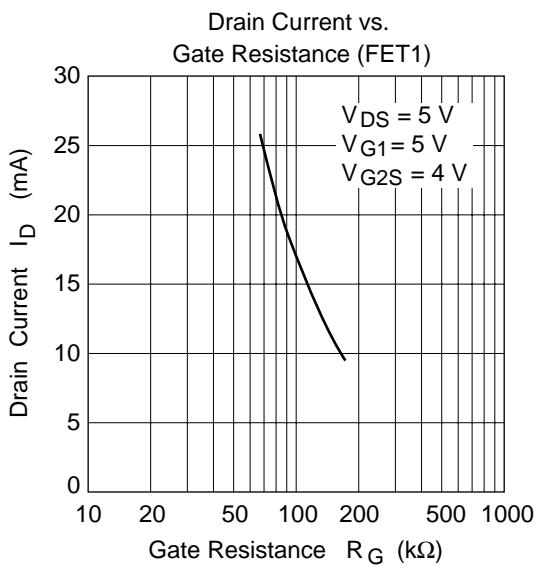
- **200 MHz Power Gain, Noise Figure Test Circuit**

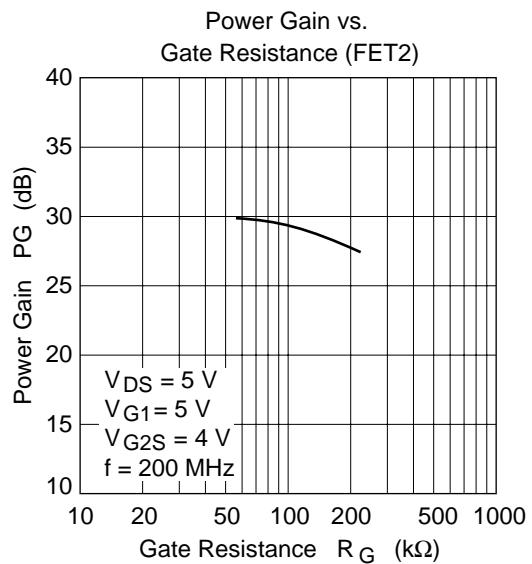
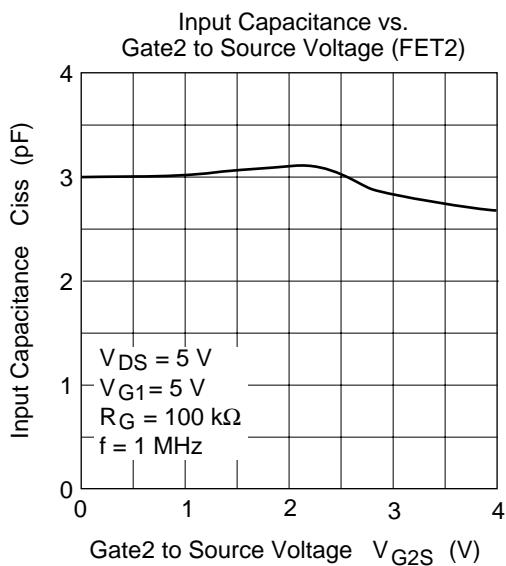
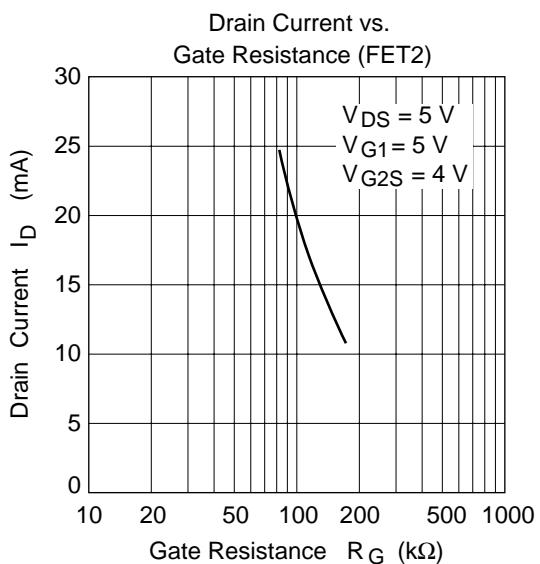
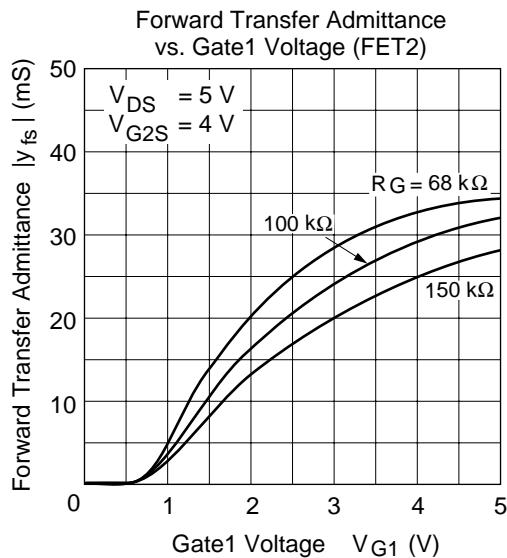


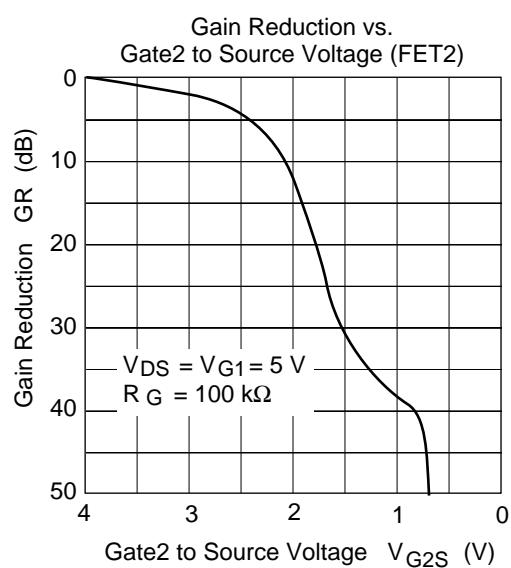
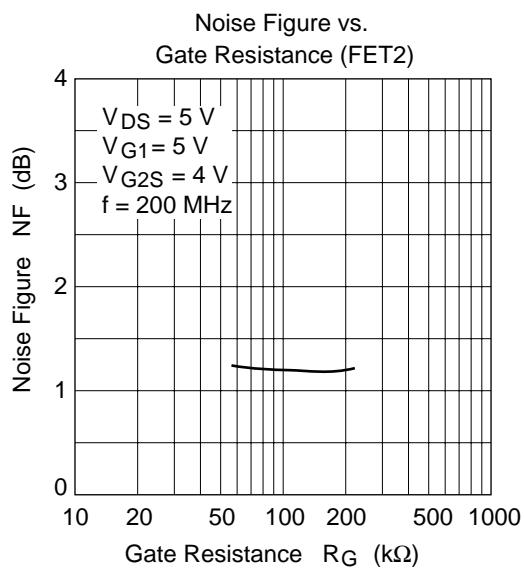


\* Value on the glass epoxy board (49mm × 38mm × 1mm)





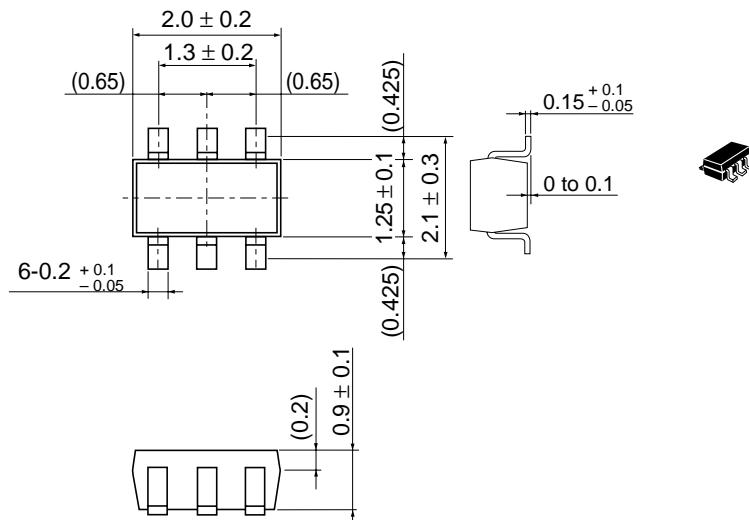




**Package Dimensions**

As of January, 2001

Unit: mm



|                        |          |
|------------------------|----------|
| Hitachi Code           | CMPAK-6  |
| JEDEC                  | —        |
| EIAJ                   | Conforms |
| Mass (reference value) | 0.006 g  |

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