

ON Semiconductor

Is Now



To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and onsemi. and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi does not convey any license under any of its intellectual property rights nor the rights of others. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application, Buyer shall indemnify and hold onsemi and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that onsemi was negligent regarding the design or manufacture of the part. onsemi is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

CM1215

1, 2 and 4-Channel Low Capacitance ESD Arrays

Product Description

The CM1215 family of diode arrays provides ESD protection for electronic components or sub-systems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive (VP) or negative (VN) supply rail. The CM1215 protects against ESD pulses up to ± 15 kV per the IEC 61000-4-2 standard.

This device is particularly well-suited for protecting systems using high-speed ports such as USB2.0, IEEE1394 (Firewire®, iLink™), Serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

Features

- One, two, and four channels of ESD Protection
- Provides ± 15 kV ESD Protection on Each Channel Per the IEC 61000-4-2 ESD Requirements
- Channel Loading Capacitance of 1.6 pF Typical
- Channel I/O to GND Capacitance Difference of 0.04 pF Typical
- Mutual Capacitance of 0.13 pF Typical
- Minimal Capacitance Change with Temperature and Voltage
- Each I/O Pin Can Withstand Over 1000 ESD Strikes
- SOT Packages
- These Devices are Pb-Free and are RoHS Compliant

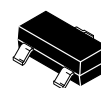
Applications

- IEEE1394 Firewire® Ports at 400 Mbps / 800 Mbps
- DVI Ports, HDMI Ports in Notebooks, Set Top Boxes, Digital TVs, LCD Displays
- Serial ATA Ports in Desktop PCs and Hard Disk Drives
- PCI Express Ports
- General Purpose High-Speed Data Line ESD Protection

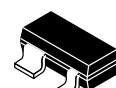


ON Semiconductor®

<http://onsemi.com>



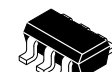
**SOT23-3
SO SUFFIX
CASE 419AH**



**SOT143
SR SUFFIX
CASE 527AF**

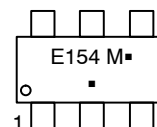
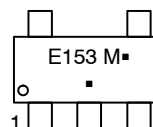
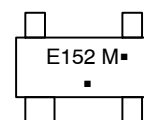
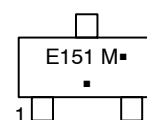


**SOT23-5
SO SUFFIX
CASE 527AH**



**SOT23-6
SO SUFFIX
CASE 527AJ**

MARKING DIAGRAM



XXXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

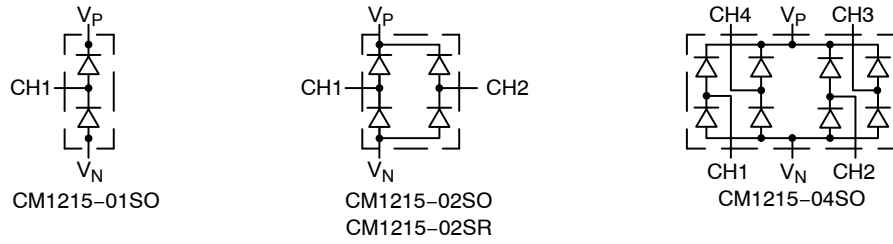
ORDERING INFORMATION

Device	Package	Shipping†
CM1215-01SO	SOT23-3 (Pb-Free)	3000/Tape & Reel
CM1215-02SR	SOT143 (Pb-Free)	3000/Tape & Reel
CM1215-02SO	SOT23-5 (Pb-Free)	3000/Tape & Reel
CM1215-04SO	SOT23-6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

CM1215

BLOCK DIAGRAM



PACKAGE / PINOUT DIAGRAMS

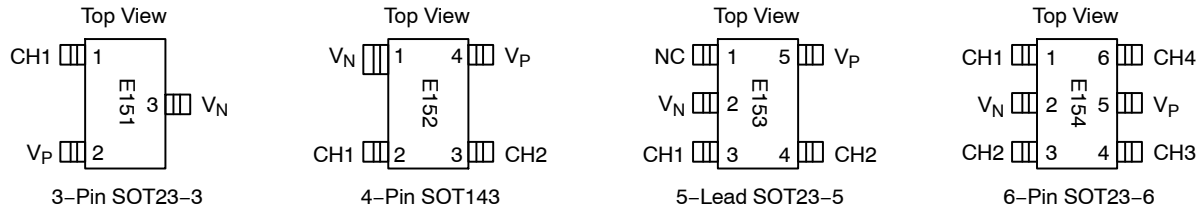


Table 1. PACKAGE PIN DESCRIPTIONS

Pin Name	SOT23-3	SOT143	SOT23-5	SOT23-6	Type	Description
	Pin No.	Pin No.	Pin No.	Pin No.		
CH1	1	2	3	1	I/O	ESD Channel
V _N	3	1	2	2	GND	Negative voltage supply rail
CH2	–	3	4	3	I/O	ESD Channel
CH3	–	–	–	4	I/O	ESD Channel
V _P	2	4	5	5	PWR	Positive voltage supply rail
CH4	–	–	–	6	I/O	ESD Channel
N/C	–	–	1	–	–	No Connection

CM1215

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Supply Voltage (V_P-V_N)	6	V
Diode Forward DC Current (Note 1)	20	mA
DC Voltage at any Channel Input	$(V_N-0.5)$ to $(V_P+0.5)$	V
Operating Temperature Range		
Ambient	-40 to +85	°C
Junction	-40 to +125	°C
Storage Temperature Range	-40 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	-40 to +85	°C
Package Power Rating SOT23-3 Package (CM1215-01SO) SOT143 Package (CM1215-02SR) SOT23-5 Package (CM1215-02SO) SOT23-6 Package (CM1215-04SO)	225 225 225 225	mW

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_P	Operating Supply Voltage (V_P-V_N)			3.3	5.5	V
I_P	Operating Supply Current	$(V_P-V_N) = 3.3$ V			8	μA
V_F	Diode Forward Voltage Top Diode Bottom Diode	$I_F = 20$ mA; $T_A = 25^\circ\text{C}$	0.6 0.6	0.8 0.8	0.95 0.95	V
I_{LEAK}	Channel Leakage Current	$T_A = 25^\circ\text{C}$; $V_P = 5$ V, $V_N = 0$ V		±0.1	±1.0	μA
C_{IN}	Channel Input Capacitance	At 1 MHz, $V_P = 3.3$ V, $V_N = 0$ V, $V_{IN} = 1.65$ V;		1.6	2.0	pF
ΔC_{IN}	Channel I/O to GND Capacitance Difference			0.04		pF
C_{MUTUAL}	Mutual Capacitance	$(V_P-V_N) = 3.3$ V		0.13		pF
V_{ESD}	ESD Protection Peak Discharge Voltage at any channel input, in system, contact discharge per IEC 61000-4-2 standard	$T_A = 25^\circ\text{C}$ (Notes 2 and 3)	±15			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	$I_{PP} = 1$ A, $t_P = 8/20$ μS; $T_A = 25^\circ\text{C}$;		$V_P+1.5$ $V_N-1.5$		V
R_{DYN}	Dynamic Resistance Positive transients Negative transients	$I_{PP} = 1$ A, $t_P = 8/20$ μS; $T_A = 25^\circ\text{C}$;		0.4 0.4		Ω

1. All parameters specified at $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted.
2. Standard IEC 61000-4-2 with $C_{Discharge} = 150$ pF, $R_{Discharge} = 330$ Ω, $V_P = 3.3$ V, V_N grounded.
3. From I/O pins to V_P or V_N only. V_P bypassed to V_N with low ESR 0.2 μF ceramic capacitor.

PERFORMANCE INFORMATION

Input Channel Capacitance Performance Curves

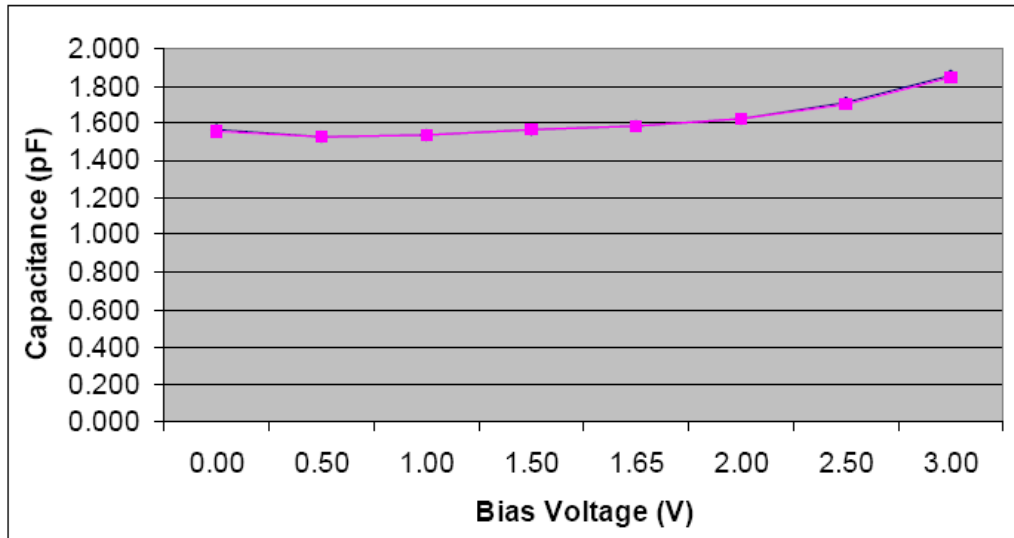


Figure 1. Typical Variation of C_{IN} vs. V_{IN}
 ($f = 1 \text{ MHz}$, $V_P = 3.3 \text{ V}$, $V_N = 0 \text{ V}$, $0.1 \mu\text{F}$ Chip Capacitor between V_P and V_N , $T_A = 25^\circ\text{C}$)

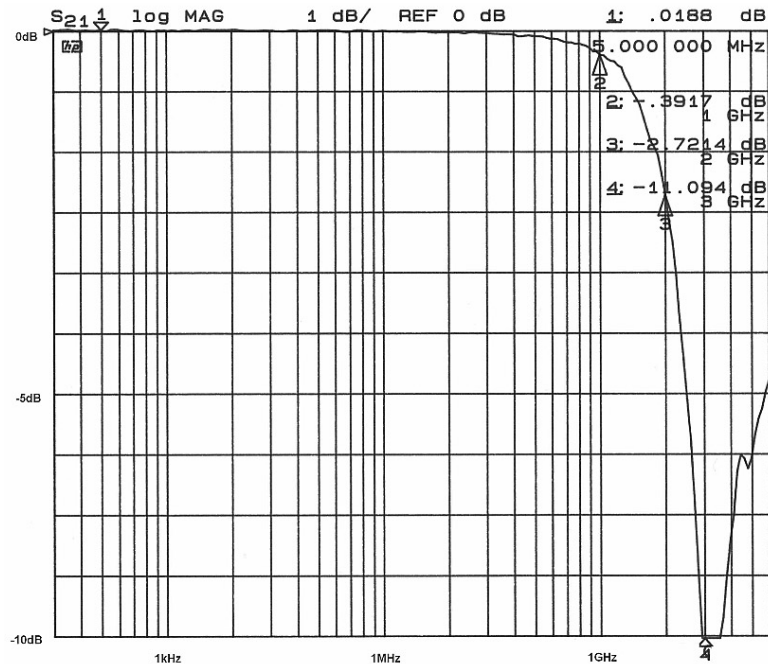


Figure 2. Typical Filter Performance (Nominal Conditions unless Specified Otherwise, 50 Ohm Environment)

APPLICATION INFORMATION

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/ Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Figure 1, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L1 and L2. The voltage VCL on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD}) / dt + L_2 \times d(I_{ESD}) / dt$$

where IESD is the ESD current pulse, and VSUPPLY is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1ns. Here d(IESD)/dt can be approximated by d(ESD)/dt, or 30/(1x10⁻⁹). So just 10 nH of series inductance (L1 and L2 combined) will lead to a 300 V increment in VCL!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See also ON Semiconductor Application Note, "Design Considerations for ESD Protection", in the Applications section.

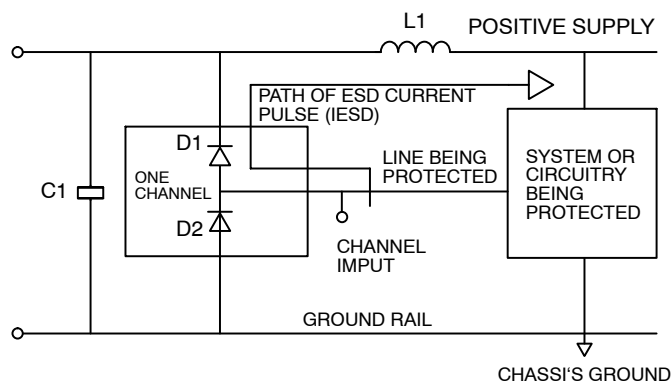
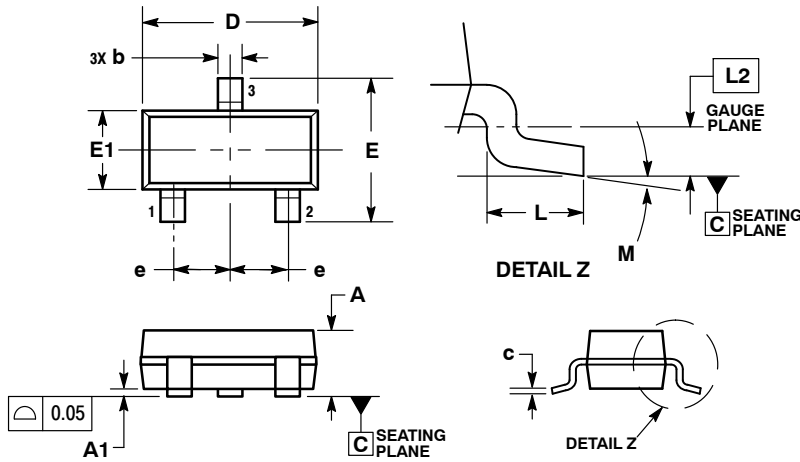


Figure 3. Application of Positive ESD Pulse between Input Channel and Ground

CM1215

PACKAGE DIMENSIONS

SOT-23 3-Lead (TO-236AA)
CASE 419AH-01
ISSUE O

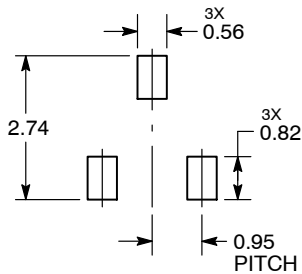


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS	
	MIN	MAX
A	0.75	1.17
A1	0.05	0.15
b	0.30	0.50
c	0.08	0.20
D	2.80	3.05
E	2.10	2.64
E1	1.20	1.40
e	0.95 BSC	
L	0.40	0.60
L2	0.25 BSC	
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



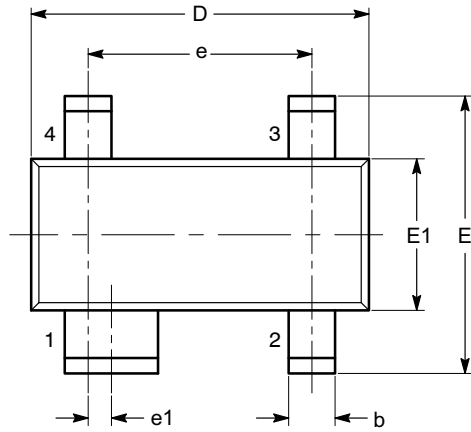
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

CM1215

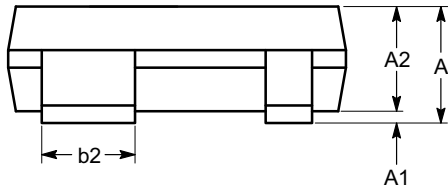
PACKAGE DIMENSIONS

SOT-143, 4 Lead
CASE 527AF-01
ISSUE A

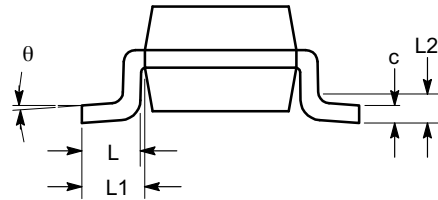


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.22
A1	0.05		0.15
A2	0.75	0.90	1.07
b	0.30		0.50
b2	0.76		0.89
c	0.08		0.20
D	2.80	2.90	3.04
E	2.10		2.64
E1	1.20	1.30	1.40
e	1.92 BSC		
e1	0.20 BSC		
L	0.40	0.50	0.60
L1	0.54 REF		
L2		0.25	
θ	0°		8°



SIDE VIEW



END VIEW

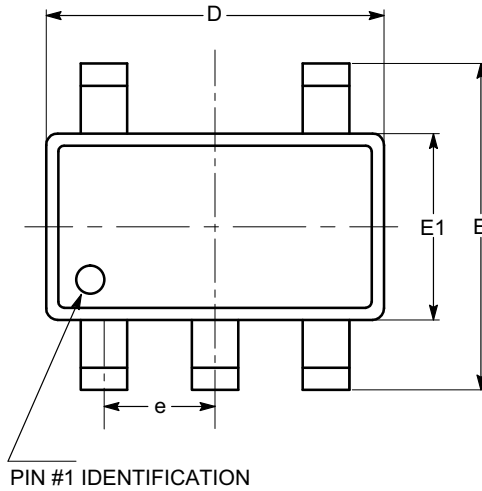
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC TO-253.

CM1215

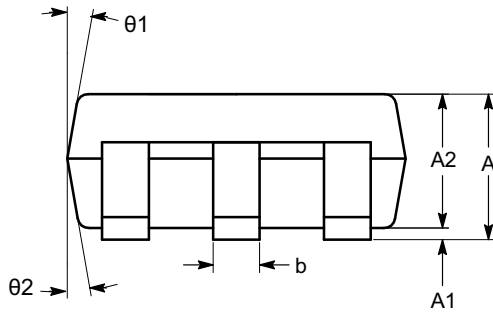
PACKAGE DIMENSIONS

SOT-23, 5 Lead
CASE 527AH-01
ISSUE O

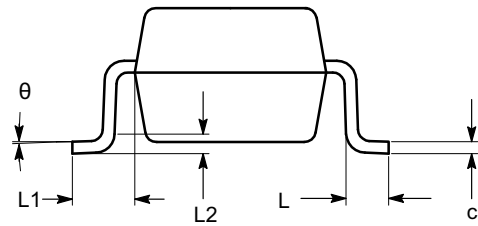


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.90		1.45
A1	0.00		0.15
A2	0.90	1.15	1.30
b	0.30		0.50
c	0.08		0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
$\theta 1$	5°	10°	15°
$\theta 2$	5°	10°	15°



SIDE VIEW



END VIEW

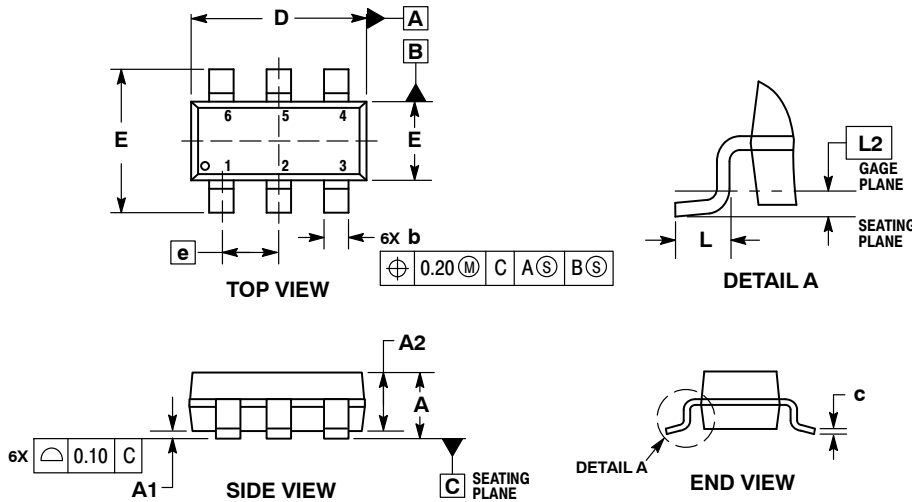
Notes:

- (1) All dimensions in millimeters. Angles in degrees.
- (2) Complies with JEDEC standard MO-178.

CM1215

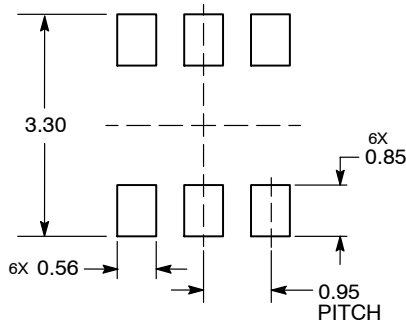
PACKAGE DIMENSIONS

SOT-23, 6 Lead
CASE 527AJ-01
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DATUM C IS THE SEATING PLANE.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

FireWire is a registered trademark of Apple Computer, Inc.
iLink is a trademark of S. J. Electro Systems, Inc.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative