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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74HC283

4-bit Binary Full Adder



ADE-205-485 (Z)

1st. Edition

Sep. 2000

Description

The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. This adder features full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation. The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- High Speed Operation: $t_{pd} = 19 \text{ ns typ (} C_L = 50 \text{ pF)}$
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2 \text{ to } 6 \text{ V}$
- Low Input Current: $1 \mu\text{A max}$
- Low Quiescent Supply Current: $I_{CC} \text{ (static)} = 4 \mu\text{A max (} T_a = 25^\circ\text{C)}$

Function Table

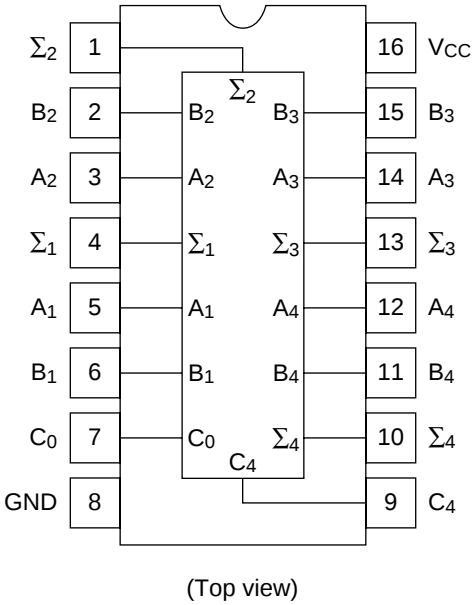
Inputs				Outputs					
				When C ₀ = L/When C ₂ = L			When C ₀ = H/When C ₂ = H		
A ₁ /A ₃	B ₁ /B ₃	A ₂ /A ₄	B ₂ /B ₄	Σ ₁ /Σ ₃	Σ ₂ /Σ ₄	C ₂ /C ₄	Σ ₁ /Σ ₃	Σ ₂ /Σ ₄	C ₂ /C ₄
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H : high level

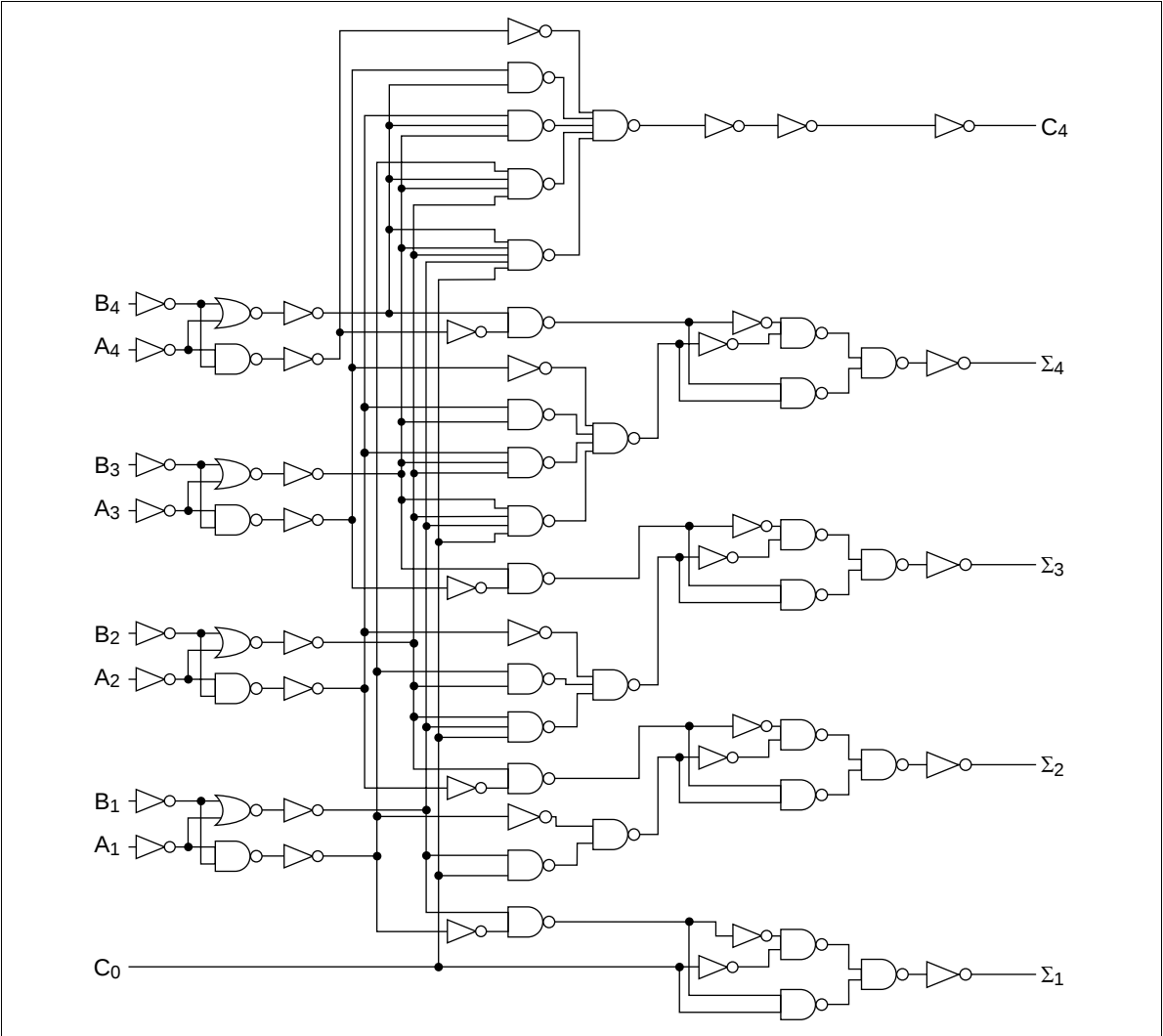
L : low level

Note: Input conditions at A₁, B₁, A₂, B₂, and C₀ are used to determine outputs Σ₁ and Σ₂ and the value of the internal carry C₂. The values at C₂, A₃, B₃, A₄ and B₄ are then used to determine outputs Σ₃, Σ₄ and C₄.

Pin Arrangement



Block Diagram



DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V _{IL}	2.0	—	—	0.5	—	0.5	V	
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		
		6.0	5.68	—	—	5.63	—		
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		
		6.0	—	—	0.26	—	0.33		
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA

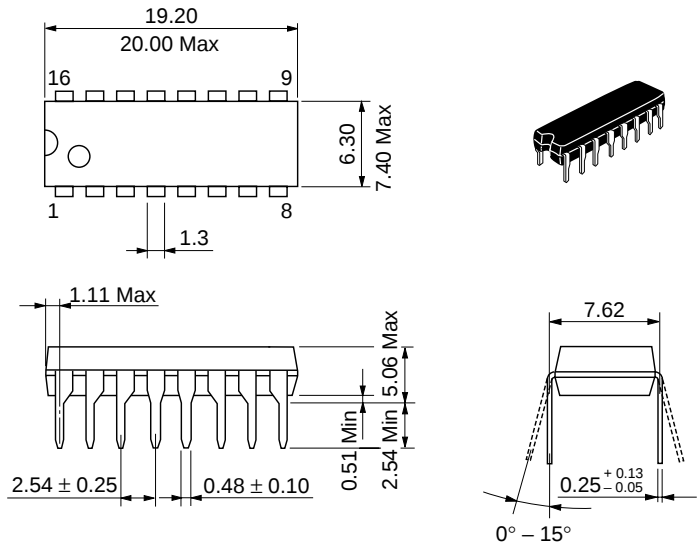
HD74HC283

AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	V _{cc} (V)	Ta = 25°C					Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	2.0	—	—	150	—	190	ns	C ₀ to Σ ₁		
	t _{PHL}	4.5	—	19	30	—	38				
		6.0	—	—	26	—	33				
	t _{PLH}	2.0	—	—	150	—	190	ns	A ₁ or B ₁ to Σ ₁		
	t _{PHL}	4.5	—	19	30	—	38				
		6.0	—	—	26	—	33				
	t _{PLH}	2.0	—	—	150	—	190	ns	C ₀ to C ₄		
	t _{PHL}	4.5	—	19	30	—	38				
		6.0	—	—	26	—	33				
	t _{PLH}	2.0	—	—	150	—	190	ns	A ₁ or B ₁ to C ₄		
	t _{PHL}	4.5	—	19	30	—	38				
		6.0	—	—	26	—	33				
Output rise/fall time	t _{TLH}	2.0	—	—	75	—	95	ns			
	t _{THL}	4.5	—	5	15	—	19				
		6.0	—	—	13	—	16				
Input capacitance	Cin	—	—	5	10	—	10	pF			

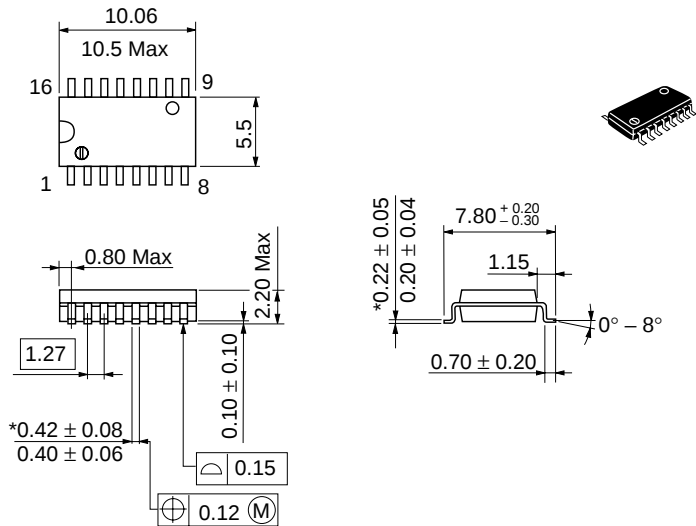
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

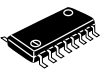
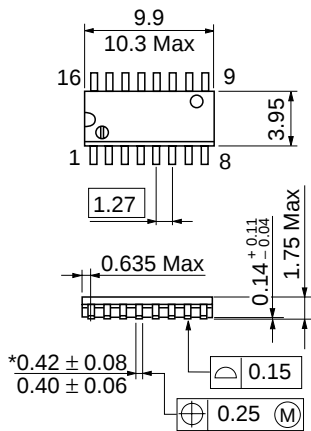
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.15 g

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