PRELIMINARY

CY2XF23

High Performance LVDS Oscillator with Frequency Margining - I²C Control

Features

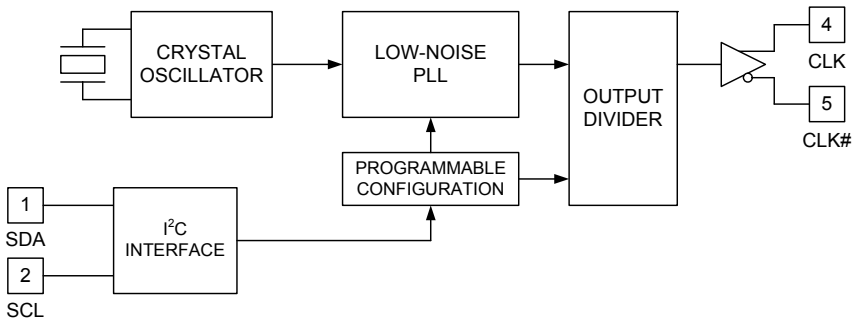
- Low Jitter Crystal Oscillator (XO)
- Less than 1ps Typical RMS Phase Jitter
- Differential LVDS Output
- Output Frequency from 50 MHz to 690 MHz
- Frequency Margining through I²C Bus
- Factory Configured or Field Programmable
- Integrated Phase-Locked Loop (PLL)
- Pb-Free Package: 5.0 x 3.2 mm LCC
- Supply Voltage: 3.3V or 2.5V
- Commercial and Industrial Temperature Ranges

Functional Description

The CY2XF23 is a high performance and high frequency Crystal Oscillator (XO). It uses a Cypress proprietary low noise PLL to synthesize the frequency from an integrated crystal. The output frequency can be changed using the I²C Bus serial interface, allowing easy frequency margin testing in applications.

The CY2XF23 is available as a factory configured device or as a field programmable device.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 6 Pin Ceramic LCC

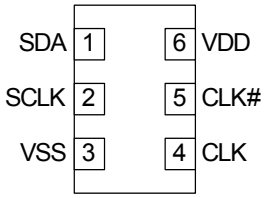


Table 1. Pin Definitions - 6 Pin Ceramic LCC

Pin	Name	I/O Type	Description
1	SDA	I/O	I²C Serial Data
2	SCLK	CMOS Input	I²C Serial Clock
4, 5	CLK, CLK#	LVDS Output	Differential Output Clock
6	VDD	Power	Supply Voltage: 2.5V or 3.3V
3	VSS	Power	Ground

Functional Description

The CY2XF23 is a phase locked loop (PLL) based high performance clock generator. It uses an internal crystal oscillator as a reference, and outputs one differential LVDS clock. It has an I^2C Bus serial interface[1], which is used to change the output frequency.

The CY2XF23 comes configured for four different frequencies. At power on, the four configurations are transparently loaded into an internal volatile memory which in turn controls the PLL. The user can switch between the four frequencies through the I^2C Bus. The user can also configure the CY2XF23 with new output frequencies by shifting new data into the internal memory.

Frequency margining is a common application for this feature. One frequency is used for the standard operating mode of the device, while additional frequencies are available for margin testing, either during product development or in system manufacturing test.

Note that all configuration changes made using I^2C are temporary and are lost when power is removed from the device. At power on, the device returns to its original state.

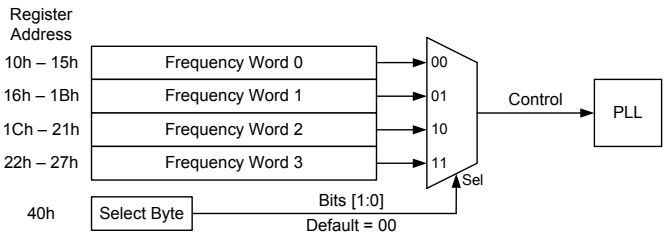
The configuration for a particular frequency is stored in a 6-byte block of memory, known as a word. The CY2XF23 has four such words, labeled Frequency Word 0 through Frequency Word 3. An additional register byte contains a 2-bit field, which selects one of the four frequency words. By writing to this Select Byte, the user can switch back and forth between the four programmed frequencies. The select byte is always defined to select Frequency Word 0 at power on.

When changing the output frequency, the frequency transition is not guaranteed to be smooth. There can be frequency excursions beyond the start frequency and the new frequency. Glitches and runt pulses are possible, and time must be allowed for the PLL to re-lock.

If more than four frequencies are needed, the I^2C Bus can be used to change any of the four frequency words. When writing frequency words via I^2C, users should not change the currently selected word. Instead, write one of the three unselected words before changing the select byte to select that new word.

Figure 2 shows how the frequency words are arranged and selected.

Figure 2. Frequency Words



Configuration Software

Cypress provides CyberClocks™ Online web-based software that enables users to create data values for shifting into the frequency words. This software is required because the algorithm is too complicated to describe here.

The software is located at www.cyberclocksonline.com.

The user specifies the output frequency. The software then calculates the bit stream. The bit stream is generic in the sense that it can be shifted into any of the four Frequency Words. This process is repeated for all frequencies of interest.

Programming Description

The CY2XF23 is a programmable device. Before being used in an application, it must be programmed with the output frequencies and other variables described in a later section. Two different device types are available, each with its own programming flow. They are described in the following sections.

Field Programmable CY2XF23F

Field programmable devices are shipped unprogrammed and must be programmed before being installed on a printed circuit board (PCB). Customers use CyberClocks Online Software to specify the device configuration and generate a JEDEC (extension .jed) programming file. Programming of samples and prototype quantities is available using a Cypress programmer. Third party vendors manufacture programmers for small to large volume applications. Cypress's value added distribution partners also provide programming services. Field programmable devices are designated with an "F" in the part number. They are intended for quick prototyping and inventory reduction. The CY2XF23 is one time programmable (OTP).

Factory Configured CY2XF23

For customers wanting ready-to-use devices, the CY2XF23 is available with no field programming required. All requests are submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, the user receives a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample requests and production orders.

Note
1. The serial interface is I^2C Bus compliant, with the following exceptions: SDA input leakage current, SDA input capacitance, SDA and SCLK are clamped to V_{DD}, setup time, and output hold time.

Programming Variables

Output Frequencies

The CY2XF23 is programmed with up to four independent output frequencies, which are then selected using the I^2C interface. The device can synthesize frequencies to a resolution of 1 part per million (ppm), but the actual accuracy of the output frequency is limited by the accuracy of the integrated reference crystal.

The CY2XF23 has an output frequency range of 50 MHz to 690 MHz, but the range is not continuous. The CY2XF23 cannot generate frequencies in the ranges of 521 MHz to 529 MHz, and 596 MHz to 617 MHz.

Industrial Versus Commercial Device Performance

Industrial and Commercial devices have different internal crystals. This has a potentially significant impact on performance levels for applications requiring the lowest possible phase noise. CyberClocks Online Software displays expected performance for both options.

Phase Noise Versus Jitter Performance

In most cases, the device configuration for optimal phase noise performance is different from the device configuration for optimal cycle to cycle or period jitter. CyberClocks Online Software includes algorithms to optimize performance for either parameter.

Table 2. Device Programming Variables

Variable
Output Frequency 0
Output Frequency 1
Output Frequency 2
Output Frequency 3
Optimization (phase noise or jitter)
Temperature range (Commercial or Industrial)

Memory Map

Five fields can be written via the I^2C Bus. Four frequency words define the output frequency. As shown in Table 3, each of these words is a 6-byte field. When writing to a frequency word, all 6 bytes should be written. They may be written either as individual byte writes, or as a block write. The currently selected frequency word should not be written to. All four words are symmetrical, meaning that a 6-byte value that is valid for one word is also valid for any of the other words, and produces the same frequency.

The fifth field is the select byte, located at byte address 40h. The value written into the two least significant bits determines the active frequency word. The other bits of the byte are reserved and should be written with the values indicated in the table. Users should never write to any address other than the 25 bytes described here.

Table 3. Frequency Words

Frequency Word	Byte Addresses (hex)	Word Select (Select Byte 40h)
0	10h to 15h	00
1	16h to 1Bh	01
2	1Ch to 21h	10
3	22h to 27h	11

Table 4. Register 40h: Select Byte

Bits	Default Value (binary)	Name	Description
7:2	000000	Reserved	Reserved. Always write this value.
1:0	00	Word Select	Selects the Frequency Word to determine the output frequency. 00 selects Word 0; 01 selects Word 1; 10 selects Word 2; 11 selects Word 3.

Serial Interface Protocol and Timing

The CY2XF23 uses pins SDA and SCLK for an I^2C Bus that operates up to 100 kbits/sec in Read or Write mode. The CY2XF23 is always a slave on this bus, meaning that it never initiates a bus transaction. The basic Write protocol is as follows:

Start Bit; 7-bit Device Address (DA); R/$\overline{W}$ Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; and so on, until STOP Bit. The basic serial format is illustrated in Figure 4 on page 5.

Device Address

The device address is a 7-bit value. The default serial interface address is 69H.

Data Valid

Data is valid when the clock is HIGH, and may only be transitioned when the clock is LOW as illustrated in Figure 5 on page 5.

Data Frame

Every new data frame is indicated by a start and stop sequence, as illustrated in Figure 6 on page 5.

START Sequence - Start Frame is indicated by SDA going LOW when SCLK is HIGH. Every time a start signal is given, the next 8-bit data must be the device address (seven bits) and a R/W bit, followed by register address (eight bits) and register data (eight bits).

STOP Sequence - Stop Frame is indicated by SDA going HIGH when SCLK is HIGH. A Stop Frame frees the bus for writing to another part on the same bus or writing to another random register address.

Acknowledge Pulse

During Write Mode, the CY2XF23 responds with an Acknowledge (ACK) pulse after every eight bits. This is accomplished by pulling the SDA line LOW during the N*9th clock cycle as illustrated in Figure 7 on page 6. (N = the number of bytes transmitted). After the data packet is sent during Read Mode, the master generates the acknowledge.

Write Operations

Writing Individual Bytes

A valid write operation must have a full 8-bit register address after the device address word from the master, which is followed by an acknowledge bit from the slave (SDA = 0/LOW). The next eight bits must contain the data word intended for storage. After the data word is received, the slave responds with another acknowledge bit (SDA = 0/LOW), and the master must end the write sequence with a STOP condition.

Writing Multiple Bytes

To write more than one byte at a time, the master does not end the write sequence with a stop condition. Instead, the master can send multiple contiguous bytes of data to be stored. After each byte, the slave responds with an acknowledge bit, just like after the first byte, and accept data until the acknowledge bit is responded to by the STOP condition. When receiving multiple bytes, the CY2XF23 internally increments the register address.

Read Operations

Read operations are initiated the same way as Write operations except that the R/W bit of the slave address is set to ‘1’ (HIGH). There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

The CY2XF23 has an onboard address counter that retains 1 more than the address of the last word access. If the last word written or read was word ‘n’, then a current address read operation would return the value stored in location ‘n+1’. When the CY2XF23 receives the slave address with the R/W bit set to a ‘1’, the CY2XF23 issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but does generate a STOP condition, which causes the CY2XF23 to stop transmission.

Random Read

Through random read operations, the master may access any memory location. To perform this type of read operation, first the word address must be set. This is accomplished by sending the address to the CY2XF23 as part of a write operation. After the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation before any data is stored in the address, but not before the internal address pointer is set. Next the master reissues the control byte with the R/W byte set to ‘1’. The CY2XF23 then issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but does generate a STOP condition which causes the CY2XF23 to stop transmission.

Sequential Read

Sequential read operations follow the same process as random reads except that the master issues an acknowledge instead of a STOP condition after transmission of the first 8-bit data word. This action results in an incrementing of the internal address pointer, and subsequently output of the next 8-bit data word. By continuing to issue acknowledges instead of STOP conditions, the master may serially read the entire contents of the slave device memory. When the internal address pointer points to the FFh register, after the next increment, the pointer will point to the 00h register.

Figure 3. Data Transfer Sequence on the Serial Bus

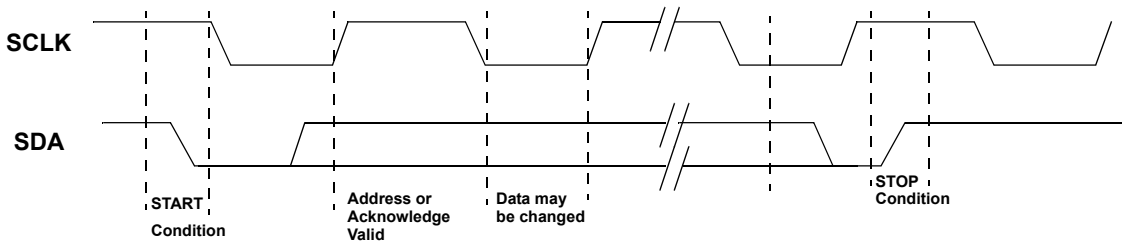


Figure 4. Data Frame Architecture

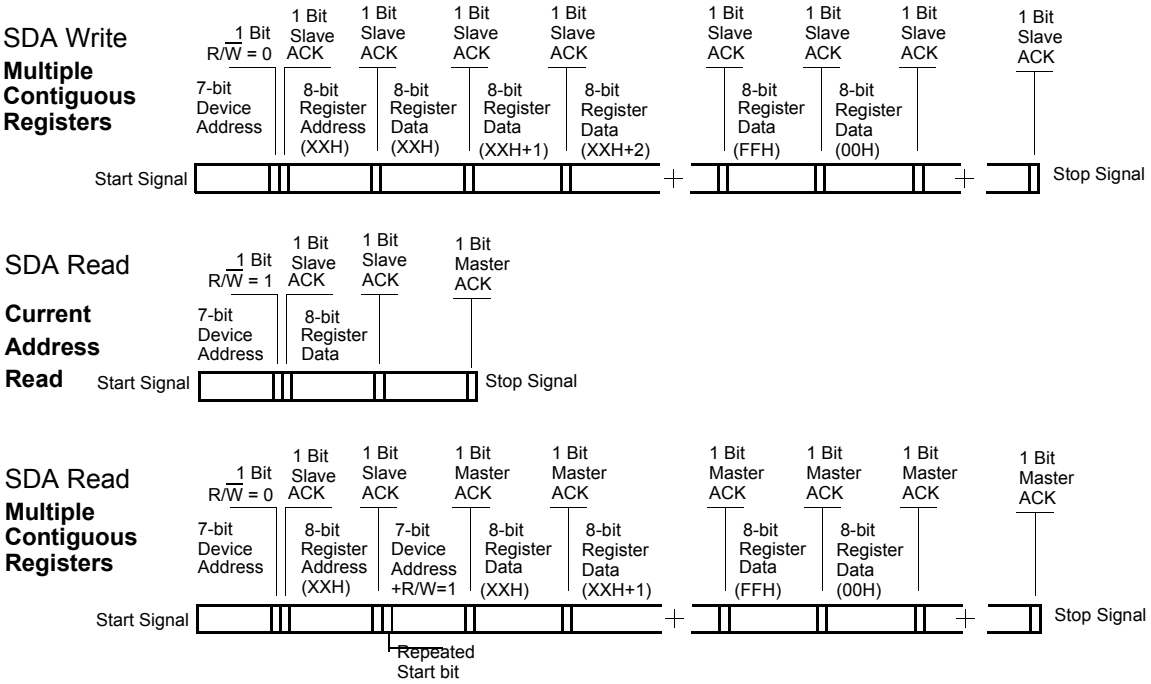


Figure 5. Data Valid and Data Transition Periods

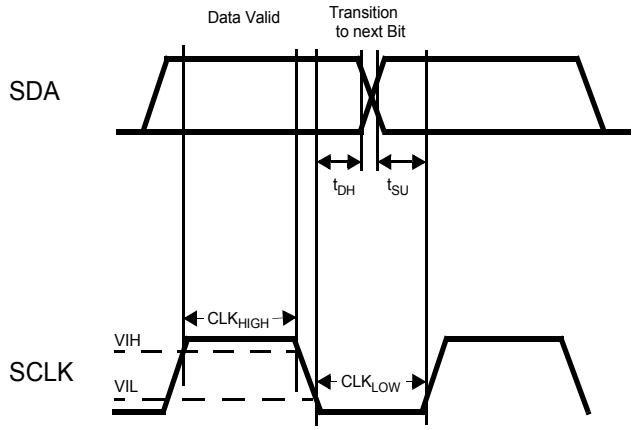


Figure 6. Start and Stop Frame

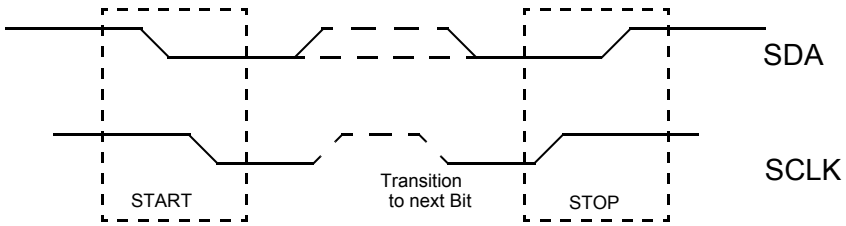
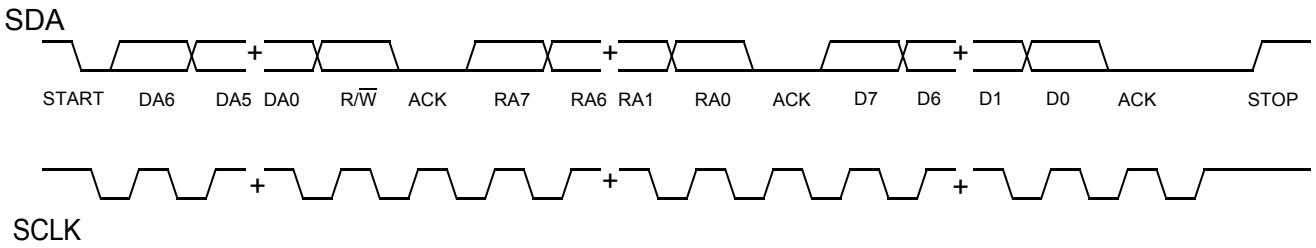


Figure 7. Frame Format (Device Address, R/$\overline{W}$, Register Address, Register Data)



Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	4.4	V
V_{IN}[2]	Input Voltage, DC	Relative to V_{SS}	–0.5	V_{DD}+0.5	V
T_S	Temperature, Storage	Non Operating	–55	135	□C
T_J	Temperature, Junction		–40	135	□C
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC STD 22-A114-B	2000	–	V
Θ_{JA}[3]	Thermal Resistance, Junction to Ambient	0 m/s airflow	64		□C/W

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	3.3V Supply Voltage Range	3.135	3.3	3.465	V
	2.5V Supply Voltage Range	2.375	2.5	2.625	V
T_{PU}	Power Up Time for V_{DD} to Reach Minimum Specified Voltage (Power Ramp is Monotonic)	0.05	–	500	ms
T_A	Ambient Temperature (Commercial)	0	–	70	□C
	Ambient Temperature (Industrial)	–40	–	85	□C

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{DD}[4]	Operating Supply Current	V_{DD} = 3.465V, CLK = 150 MHz, output terminated	–	–	120	mA
		V_{DD} = 2.625V, CLK = 150 MHz, output terminated	–	–	115	mA
V_{OD}	LVDS Differential Output Voltage	V_{DD} = 3.3V or 2.5V, defined in Figure 8 as terminated in Figure 13	247	–	454	mV
ΔV_{OD}	Change in V_{OD} between Complementary Output States	V_{DD} = 3.3V or 2.5V, defined in Figure 8 as terminated in Figure 13	–	–	50	mV
V_{OS}	LVDS Offset Output Voltage	V_{DD} = 3.3V or 2.5V, defined in Figure 9 as terminated in Figure 13	1.125	–	1.375	V
ΔV_{OS}	Change in V_{OS} between Complementary Output States	V_{DD} = 3.3V or 2.5V, R_{TERM} = 100Ω between CLK and CLK#	–	–	50	mV

Notes
2. The voltage on any input or I/O pin cannot exceed the power pin during power up.
3. Simulated. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.
4. I_{DD} includes ~4 mA of current that is dissipated externally in the output termination resistors.

DC Electrical Characteristics (continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OLS}	Output Low Voltage (SDA)	I_{OL} = 4 mA	–	–	0.1*V_{DD}	V
V_{IH}	Input High Voltage		0.7*V_{DD}	–	–	V
V_{IL}	Input Low Voltage		–	–	0.3*V_{DD}	V
I_{IH0}	Input High Current (SDA)	Input = V_{DD}	–	–	115	µA
I_{IH1}	Input High Current (SCLK)	Input = V_{DD}	–	–	10	µA
I_{IL0}	Input Low Current (SDA)	Input = V_{SS}	–50	–	–	µA
I_{IL1}	Input Low Current (SCLK)	Input = V_{SS}	–20	–	–	µA
C_{IN0}[5]	Input Capacitance (SDA)		–	15	–	pF
C_{IN1}[5]	Input Capacitance (SCLK)		–	4	–	pF

AC Electrical Characteristics[5]

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{OUT}	Output Frequency[7]		50	–	690	MHz
FSC	Frequency Stability, commercial devices[6]	V_{DD} = min to max, T_A = 0°C to 70°C	–	–	±35	ppm
FSI	Frequency Stability, industrial devices[6]	V_{DD} = min to max, T_A = –40° to 85°C	–	–	±55	ppm
AG	Aging, 10 years		–	–	±15	ppm
T_{DC}	Output Duty Cycle	F <= 450 MHz, measured at zero crossing	45	50	55	%
		F > 450 MHz, measured at zero crossing	40	50	60	%
T_R, T_F	Output Rise and Fall Time	20% and 80% of full output swing	–	0.35	1.0	ns
T_{LOCK}	Startup Time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD}(min.)	–	–	5	ms
T_{LSER}	Relock Time	Time for CLK to reach valid frequency from serial bus change to select bits in register 40h, measured from I^2C STOP	–	–	1	ms
$T_{Jitter(\phi)}$	RMS Phase Jitter (Random)	f_{OUT} = 106.25 MHz (12 kHz–20 MHz)	–	1	–	ps

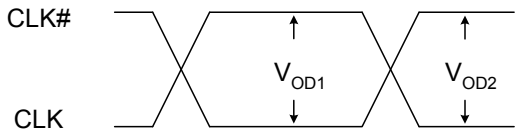
Notes
5. Not 100% tested, guaranteed by design and characterization.
6. Frequency stability is the maximum variation in frequency from F_0. It includes initial accuracy, plus variation from temperature and supply voltage.
7. This parameter is specified in CyberClocks Online software.

I²C Bus Timing Specifications[5]

Parameter	Description	Min	Max	Unit
f_{SCLK}	SCLK frequency	–	100	kHz
$t_{HD:STA}$	Start mode time from SDA LOW to SCLK LOW	4	–	µs
t_{LOW}	SCLK LOW period	4.7	–	µs
t_{HIGH}	SCLK HIGH period	4	–	µs
$t_{SU:DAT}$	Input data setup (SDA transition to SCLK rising edge)	1000	–	ns
$t_{HD:DAT}$	Input data hold (SCLK falling edge to SDA transition)	0	–	ns
$t_{HD:DO}$	Output data hold (SCLK falling edge to SDA transition)	200	–	ns
t_{SR}	Rise time of SCLK and SDA	–	300	ns
t_{SF}	Fall time of SCLK and SDA	–	300	ns
$t_{SU:STO}$	Stop mode time from SCLK HIGH to SDA HIGH	4	–	µs
t_{BUF}	Stop mode to Start mode	4.7	–	µs

Switching Waveforms

Figure 8. Output Voltage Swing



$$\Delta V_{OD} = V_{OD1} - V_{OD2}$$

Figure 9. Output Offset Voltage

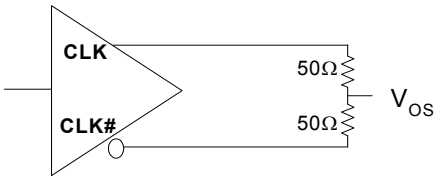
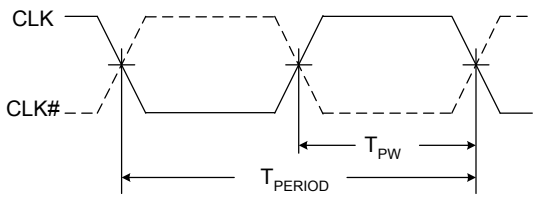


Figure 10. Duty Cycle Timing



$$T_{DC} = \frac{T_{PW}}{T_{PERIOD}}$$

Figure 11. Output Rise and Fall Time

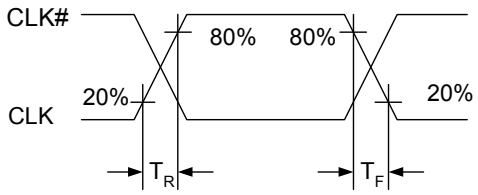
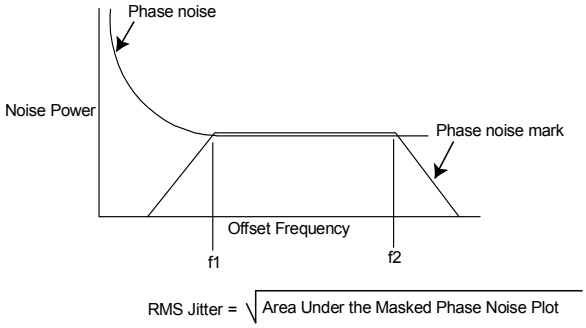
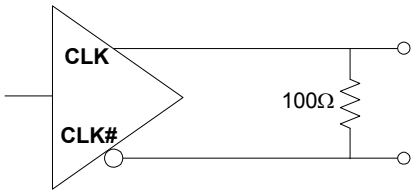


Figure 12. RMS Phase Jitter



Termination Circuits

Figure 13. LVDS Termination

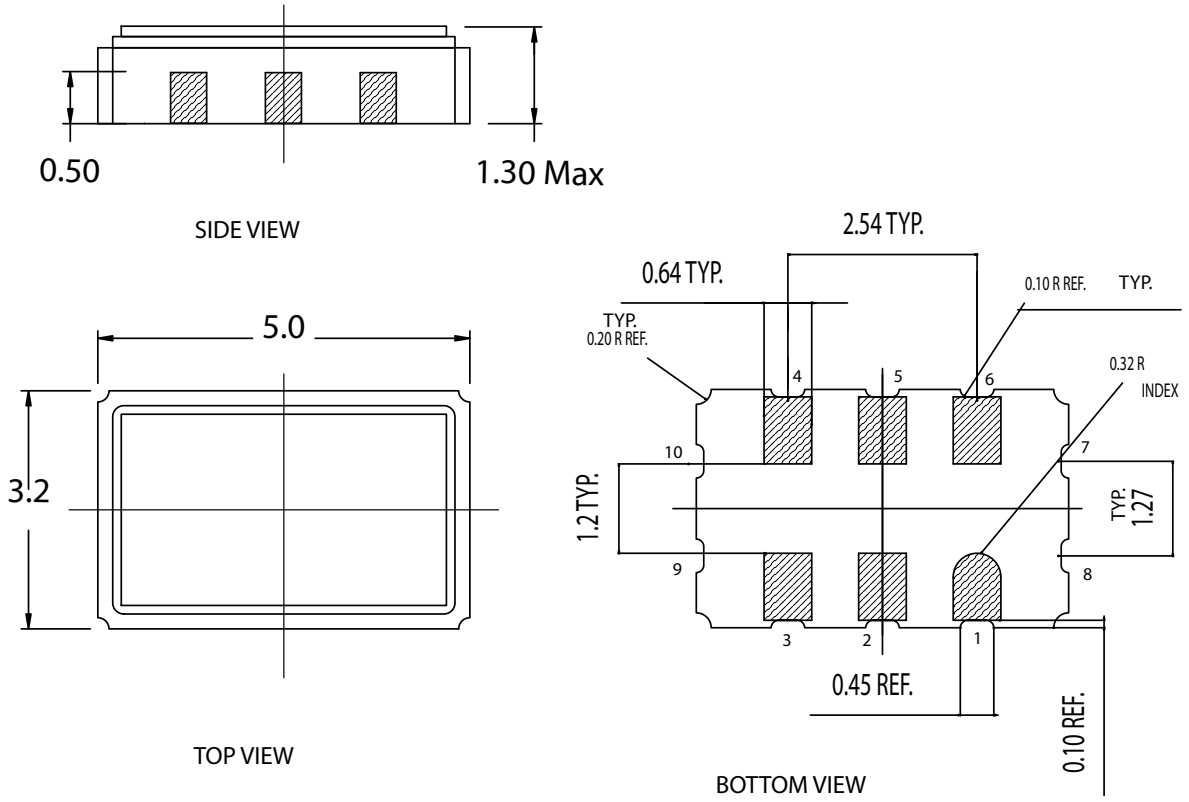


Ordering Information

Part Number[8]	Configuration	Package Description	Product Flow
Pb-Free			
CY2XF23FLXCT	Field Programmable	6-Pin Ceramic LCC SMD - Tape and Reel	Commercial, 0° to 70°C
CY2XF23FLXIT	Field Programmable	6-Pin Ceramic LCC SMD - Tape and Reel	Industrial, –40° to 85°C
CY2XF23LXCxxxT	Factory Configured	6-Pin Ceramic LCC SMD - Tape and Reel	Commercial, 0° to 70°C
CY2XF23LXIxxxT	Factory Configured	6-Pin Ceramic LCC SMD - Tape and Reel	Industrial, –40° to 85°C

Package Drawings and Dimensions

Figure 14. 6-Pin 3.2x5.0 mm Ceramic LCC LZ06A



Dimensions in mm
General Tolerance: ± 0.15MM
Kyocera dwg ref KD-VA6432-A
Package Weight ~ 0.12 grams

001-10044-**

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Note
8. "xxx" is a factory assigned code that identifies the programming option.

Document History Page

Document Title: CY2XF23 High Performance LVDS Oscillator with Frequency Margining - I2C Control Document Number: 001-53145				
REV.	**ECN NO.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2704379	KVM/PYRS	05/11/2009	New data sheet
*A	2718898	WWZ	06/15/09	Minor ECN to post data sheet to external web
*B	2764787	KVM	09/18/09	Change V_{OD} limits from 250/450 mV to 247/454 mV Add max limit for T_R, T_F: 1.0 ns Change T_{LOCK} max from 10 ms to 5 ms Change T_{LSER} max from 10 ms to 1 ms

Sales, Solutions, and Legal Information

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