TWL6041 8-Channel Low-Power Audio Codec for Portable Applications

1 Device Overview

1.1 Features

- Four Audio Digital-to-Analog Converter (DAC) Channels
- Stereo Capless Headphone Drivers
  - Up to 104-dB DR
  - Power Tune for Performance and Power Consumption Tradeoff
- Stereo 8 Ω, 1.5 W per Channel Speaker Drivers also with 4-Ω Support Capability
- Differential Earpiece Driver
- Stereo Line-Out
- Two Audio Analog-to-Digital Converter (ADC) Channels
  - 96-dBA SNR
- Four Audio Inputs:
  - Three Differential Microphone Inputs
  - Stereo Line-In and FM Input
- Two Vibrator and Haptics Feedback Channels
  - Differential H-bridge Drivers
- Two Low-Noise Analog Microphone Bias Outputs
- Two Digital Microphone Bias Outputs
- Analog Low-Power Loop from Line-in to Headphone and Speaker Outputs
- Dual Phase-Locked Loops (PLLs) for Flexible Clock Support:
  - 32-kHz Sleep Clock Input for System Low-Power Playback Mode
  - 12-, 19.2-, 26-, and 38.4-MHz System Clock Input
- Accessory Plug and Unplug Detection, Accessory Button Press Detection
- Integrated Power Supplies:
  - Negative Charge Pump for Capless Headphone Driver
  - Two Low Dropout Voltage Regulators (LDOs) for High Power Supply Rejection Ration (PSRR)
- I^2C Control
- Thermal Protection:
  - Host Interrupt
- Power Supplies:
  - Analog: 2.1 V
  - Digital I/O: 1.8 V
  - Battery: 2.3 V–5.5 V
- Package 3.8-mm × 3.8-mm 81-Pin WCSP

1.2 Applications

- Mobile and Smart Phones
- MP3 Players
- Handheld Devices

1.3 Description

The TWL6041 is an audio codec with a high level of integration providing analog audio codec functions for portable applications, as shown in Figure 1-1. The device contains multiple audio analog inputs and outputs, as well as microphone biases and accessory detection. The device is connected to the OMAP™ 4 host processor through a proprietary PDM interface for audio data communication enabling partitioning with optimized power consumption and performance. Multichannel audio data is multiplexed to a single wire for downlink (PDML) and uplink (PDMUL).

The OMAP4 device provides the TWL6041 device with five PDM audio-input channels (DL0–DL4). Channels DL0–DL3 are connected to four parallel DAC channels multiplexed to stereo headphone (HSL, HSR), stereo speaker (HFL, HFR), and earpiece (EAR) or stereo line outputs (AUXL, AUXR).

The stereo headphone path has a low-power (LP) mode operating from a 32-kHz sleep clock to enable more than 100 hours of MP3 playback time. Very-high dynamic range of 104 dBA is achieved when using the system clock input and DAC path high-performance (HP) mode. Class-AB headphone drivers provide a 1-Vrms output and are ground centered for capless connection to a headphone, thus enabling system size and cost reduction. The earpiece driver is a differential class-AB driver with 2-Vrms capability to a typical 32-Ω load or 1.4-Vrms to a typical 16-Ω load.

Stereo speaker path has filterless class-D outputs with 1.5-W capability per channel. Additionally, the 4-Ω load is supported. For output-power maximization, supply connection to an external boost is supported. Speaker drivers also support hearing aid coil loads.

For vibrator and haptic feedback support, the TWL6041 device has two PWM channels with independent input signals from DL4 or I^2C. Vibra drivers are differential H-bridge outputs, enabling fast acceleration and deceleration of vibra motor. An external driver for a hearing aid coil or a piezo speaker requiring high voltage can be connected to line outputs.

The TWL6041 supports three differential microphone inputs (MMIC, HMIC, and SMIC) and a stereo line-input (AFML, AFMR) multiplexed to two parallel ADCs. The PDM output from the ADCs is transmitted to the OMAP4 processor through UL0 and UL1. AFML, AFMR inputs can also be looped to analog outputs (LB0, LB1).

Two LDOs provide a voltage of 2.1 V to bias analog microphones (MBIAS and HBIAS). The maximum output current is 2 mA for each analog bias, allowing up to two microphones on one bias. Two LDOs provide a voltage of 1.8 V to 1.85 V to bias digital microphones (DBIAS1 and DBIAS2). One bias generator can bias several digital microphones at the same time, with a total maximum output current of 10 mA.

The TWL6041 device has an integrated negative charge pump and two LDOs (HS LDO and LS LDO) for high PSRR. The only external supply needed is 2.1 V, which is available from the 2.1-V DC-DC of TWL6030/6032 power-management IC (PMIC) in the OMAP4 system. By powering audio from low-noise 2.1-V DC-DC of low power consumption, high dynamic range and high output swing at the headset output are achieved. All other supply inputs can be directly connected to battery or system 1.8-V I/O.

Two integrated PLLs enable operation from a 12-, 19.2-, 26-, and 38.4-MHz system clock (MCLK) or, in LP playback mode, from a 32-kHz sleep clock (CLK32K). The frequency plan is based on a 48-kS/s audio data rate for all channels, and the host processor uses sample-rate converters to interface with different sample rates (for example, 44.1 kHz). In the specific case of low-power audio playback, the TWL6041 supports the 44.1-kS/s and 48-kS/s rates. Transitions between sample rates or input clocks are seamless.

Accessory plug and unplug detections are supported (PLUGDET). Some headsets have a manual switch for submitting send/end signal to the terminal through the microphone input pin. This feature is supported by a periodic accessory button press detection to minimize current consumption in sleep mode. Detection cycle properties can be programmed according to system requirements.

The TWL6041BSRS, when connected to OMAP4 and OMAP5 platform, includes SRS Audio Effects, SRS pre-processing solutions and SRS TruMedia as standard feature for Android™ ICS.

Table 1-1. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TWL6041B	YFF (81)	3.56 mm × 3.56 mm

(1) For more information, see Section 3, *Mechanical Packaging and Orderable Information*.

1.4 Functional Block Diagram

Figure 1-1 shows a simplified block diagram of the device.

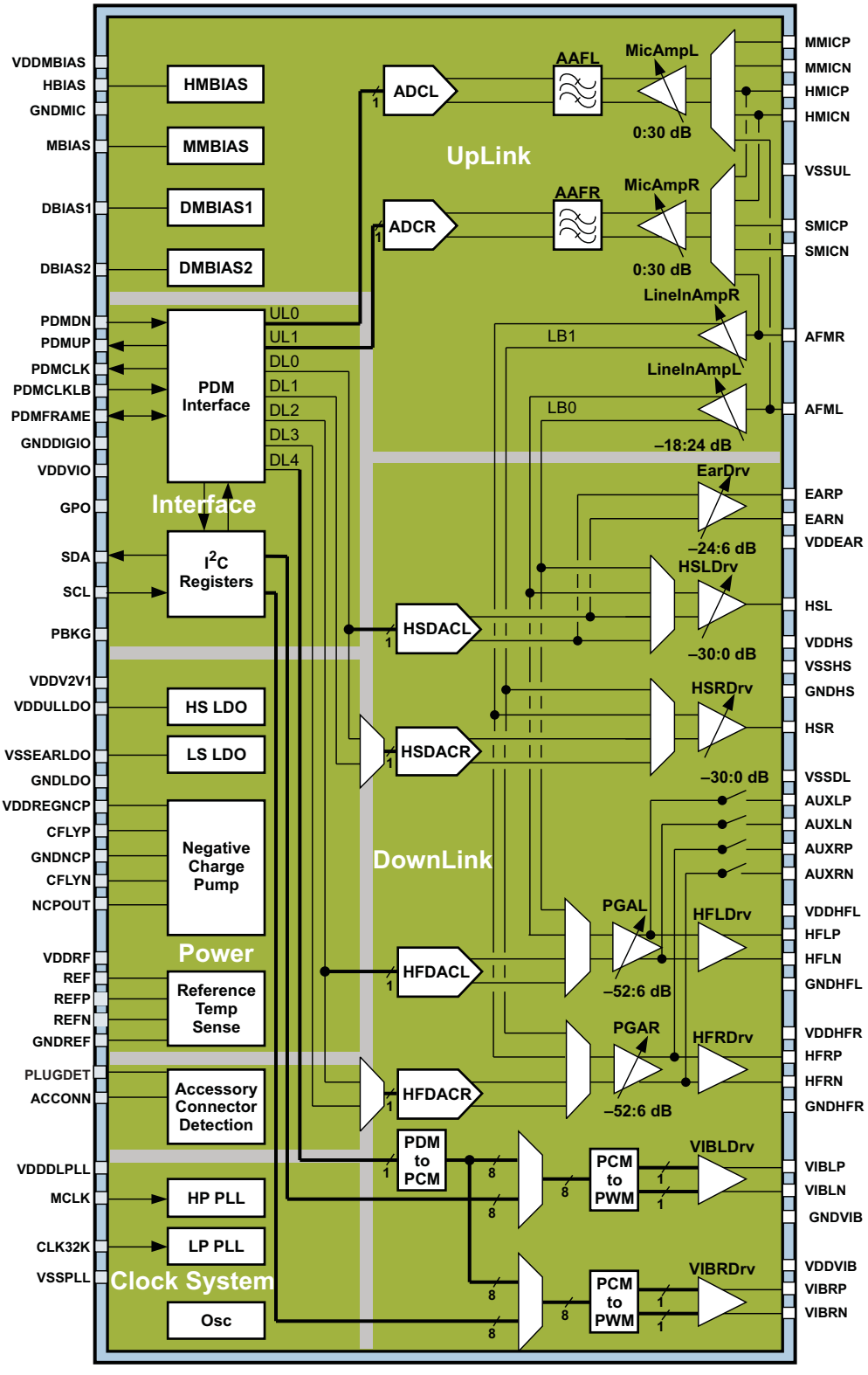


Figure 1-1. Simplified Block Diagram

For the complete TWL60xx data sheet (SWCS056), contact your TI sales representative.

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2012) to Revision D	Page
• Changed document to standard TI format	1

3 Mechanical Packaging and Orderable Information

3.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TWL6041BYFFR	Active	Production	DSBGA (YFF) | 81	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TWL6041B
TWL6041BYFFR.A	Active	Production	DSBGA (YFF) | 81	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TWL6041B
TWL6041BYFFT	Active	Production	DSBGA (YFF) | 81	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TWL6041B
TWL6041BYFFT.A	Active	Production	DSBGA (YFF) | 81	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TWL6041B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

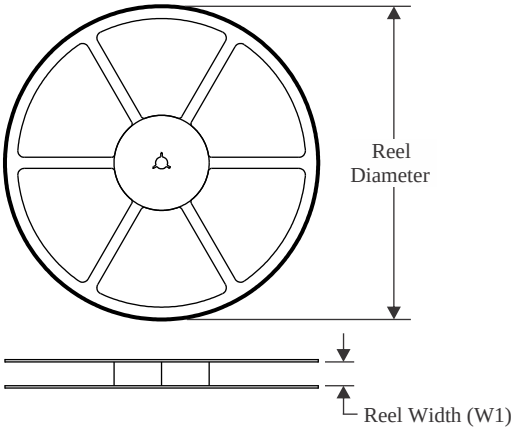
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

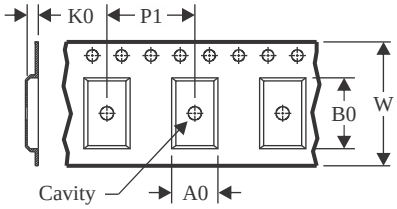
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

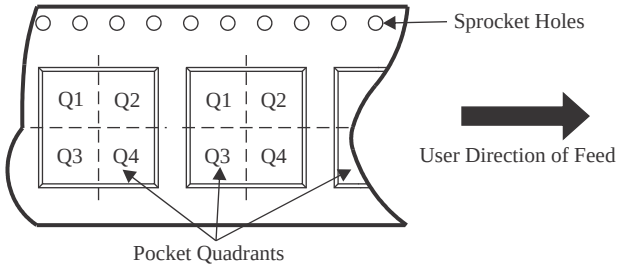


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

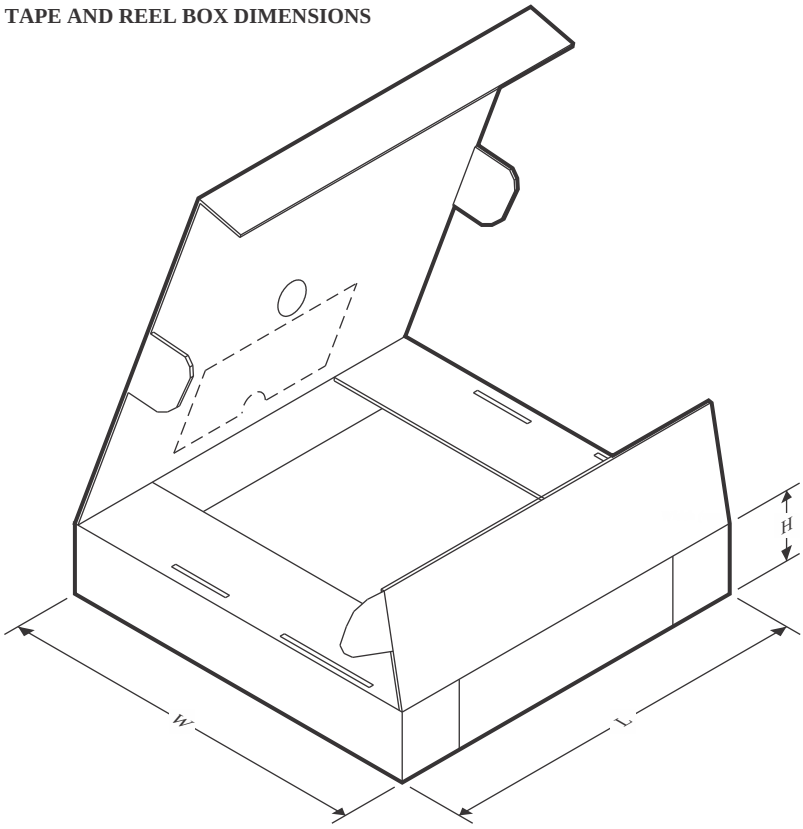
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TWL6041BYFFR	DSBGA	YFF	81	3000	330.0	12.4	3.86	3.86	0.69	8.0	12.0	Q1
TWL6041BYFFT	DSBGA	YFF	81	250	180.0	12.4	3.86	3.86	0.69	8.0	12.0	Q1

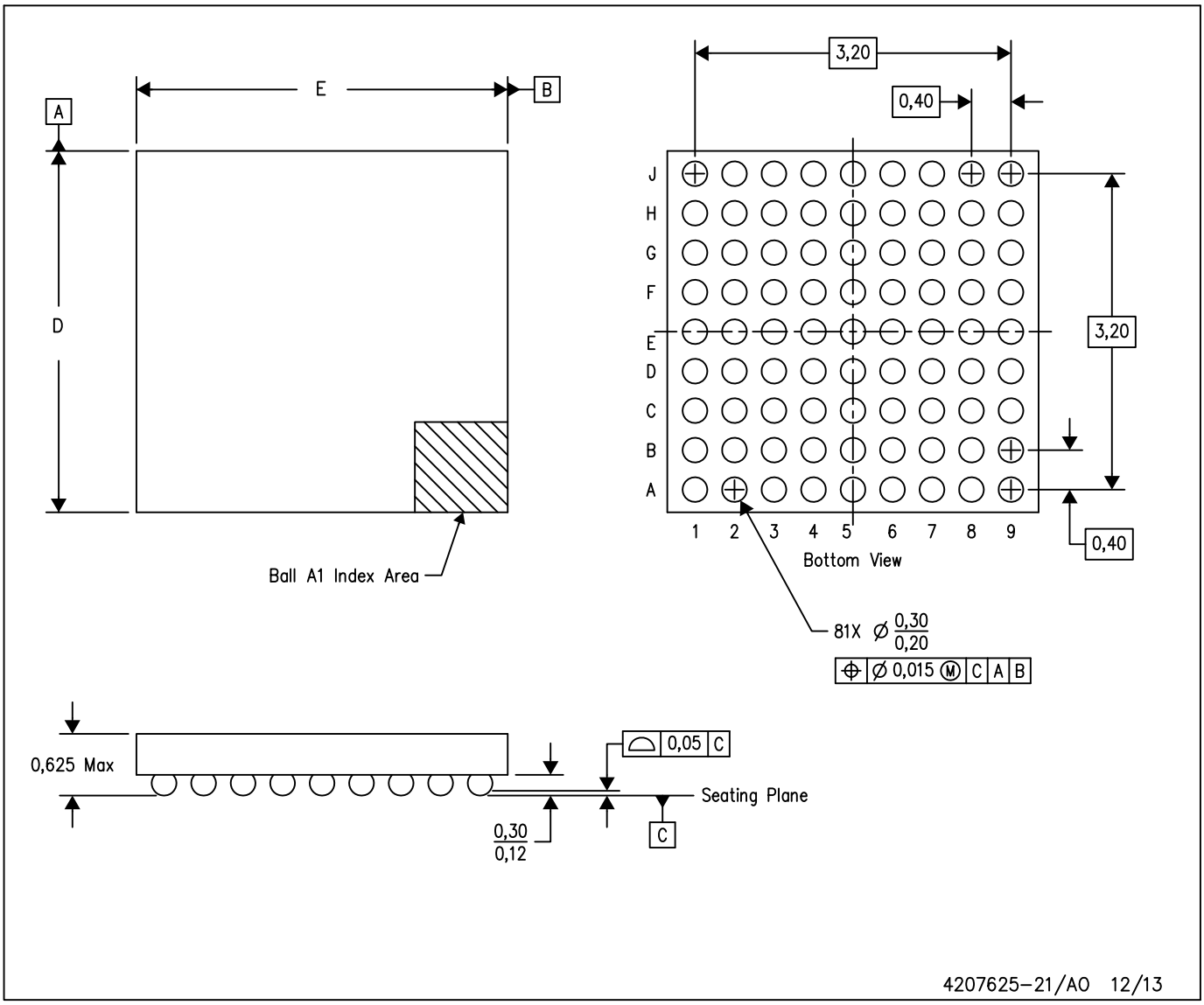
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TWL6041BYFFR	DSBGA	YFF	81	3000	335.0	335.0	25.0
TWL6041BYFFT	DSBGA	YFF	81	250	182.0	182.0	20.0

YFF (R–XBGA–N81) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265