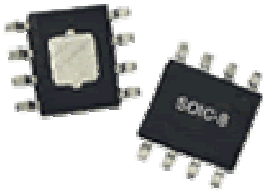
AH115

1/2 Watt, High Linearity InGaP HBT Amplifier

Applications

- Final stage amplifiers for Repeaters
- Mobile Infrastructure

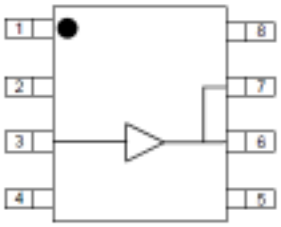


SOIC-8 Package

Product Features

- 1800 – 2300 MHz
- 14 dB Gain @ 1960 MHz
- 28.5 dBm P1dB
- +44 dBm Output IP3
- +5V Single Positive Supply
- Lead-free/green/RoHS-compliant SOIC-8 SMT Pkg

Functional Block Diagram



General Description

The AH115 is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve high performance for various narrow-band tuned application circuits with up to +44 dBm OIP3 and +28.5 dBm of compressed 1-dB power. All devices are 100% RF and DC tested. The AH115 is available in lead-free/green/RoHS-compliant SOIC-8 package.

The product is targeted for use as driver amplifiers for wireless infrastructure where high linearity and medium power is required. The internal active bias allows the AH115 to maintain high linearity over temperature and operate directly off a +5 V supply. This combination makes the device an excellent fit for transceiver line cards and power amplifiers in current and next generation multi-carrier 3G base stations.

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Pin Configuration

Pin #	Symbol
1	Vref
3	Input
6, 7	Output
8	Vbias
Backside Paddle	GND
2, 4, 5	N/C or GND

Ordering Information

Part No.	Description
AH115-S8G	½ Watt, High IP3 InGaP HBT Amp
AH115-S8PCB1960	1960 MHz Evaluation Board
AH115-S8PCB2140	2140 MHz Evaluation Board

Standard T/R size = 500 pieces on a 7” reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150 °C
RF Input Power, CW, 50Ω,T = 25ºC	+22 dBm
Device Voltage	+8 V
Device Power	2 W
Device Current	400 mA

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{cc}		+5		V
I_{cc}	200	250	300	mA
T_J (for >10^6 hours MTTF)			+200	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

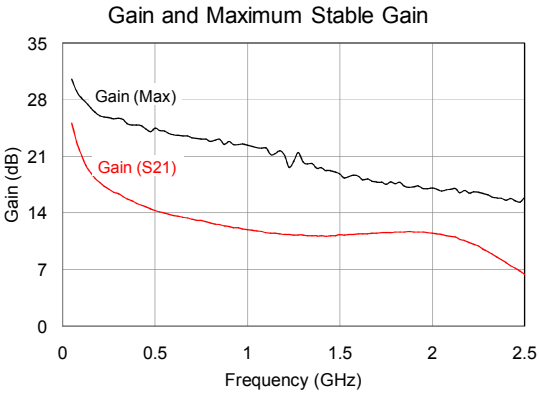
Test conditions unless otherwise noted: T_{LEAD}=25ºC, Vcc=+5V, in tuned application circuit.

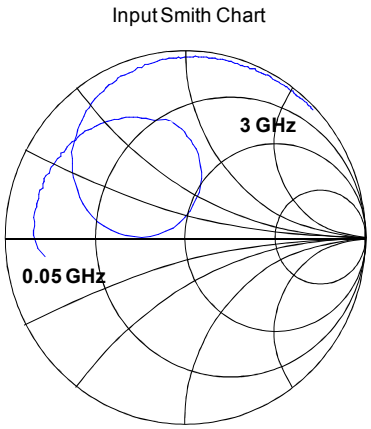
Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		1800		2300	MHz
Test Frequency			2140		MHz
Gain		12.5	14.4		dB
Input Return Loss			23		dB
Output Return Loss			8		dB
Output P1dB		+26.5	+28.5		dBm
Output IP3	See Note 1.	+41	+42		dBm
WCDMA Channel Power @ -45 dBc ACLR	See Note 2.		+20		dBm
Noise Figure			5.3		dB
Device Voltage, Vcc			+5		V
Quiescent Current, Icq		200	250	300	mA
Thermal Resistance, R_{TH}				62	°C/W

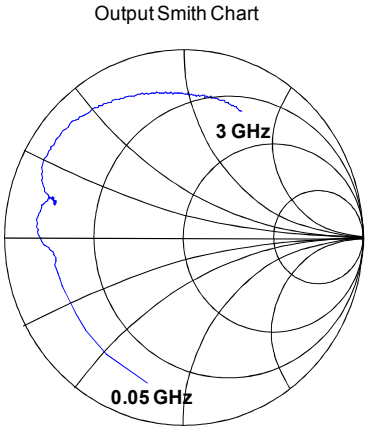
Notes:
1. 3OIP measured with two tones at an output power of +11 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.
2. 3GPP WCDMA, TM1+64DPCH, ±5 MHz Offset, no clipping, PAR = 10.2 dB @ 0.01% Probability.

Device Characterization Data

V_{CC} = +5 V, I_{CQ} = 250 mA, T_{LEAD} = 25 °C, unmatched 50 ohm system







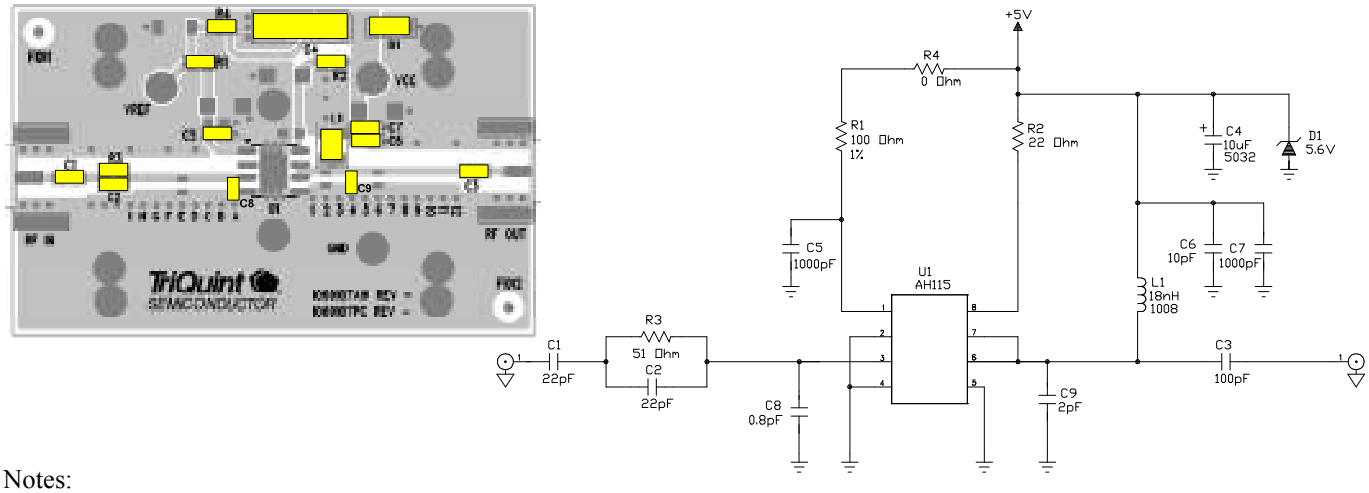
Notes:
The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the dashed red line. The impedance plots are shown from 0.5 – 3 GHz, with markers placed at 0.5 GHz and 3 GHz.

S-Parameter Data

V_{CC} = +5 V, I_{CQ} = 250 mA, T_{LEAD} = 25 °C, unmatched 50 ohm system, calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (angle)	S22 (dB)	S22 (ang)
50	-2.11	-172.90	25.10	133.84	-36.03	31.44	-2.06	-105.55
100	-1.59	-178.94	21.15	126.67	-35.22	15.04	-2.73	-138.75
200	-1.51	173.71	17.75	124.19	-34.29	7.30	-2.80	-160.44
400	-1.45	163.84	15.23	111.50	-34.45	-2.16	-2.73	-174.00
600	-1.58	153.68	13.69	98.94	-33.58	-2.99	-1.96	-179.13
800	-1.78	144.31	12.77	84.57	-32.84	-12.80	-1.68	172.00
1000	-1.96	134.21	11.94	69.70	-32.77	-18.76	-1.85	166.98
1200	-2.46	123.44	11.36	55.57	-31.79	-30.73	-2.14	164.05
1400	-3.30	111.21	11.17	40.93	-31.12	-45.14	-2.30	163.07
1600	-4.70	92.57	11.39	22.80	-30.30	-61.92	-2.52	164.84
1800	-8.15	78.58	11.64	1.64	-29.47	-83.99	-2.43	164.25
2000	-19.01	93.29	11.51	-25.24	-29.31	-112.79	-1.84	162.38
2200	-9.59	177.56	10.35	-55.97	-30.51	-150.45	-1.22	155.68
2400	-4.09	159.30	7.87	-83.78	-32.59	177.62	-1.06	147.58
2600	-1.99	141.65	4.95	-105.90	-33.96	137.14	-1.07	139.74
2800	-1.12	127.57	1.97	-122.86	-34.68	109.27	-1.19	132.15
3000	-0.72	116.11	-0.88	-136.93	-35.64	81.83	-1.44	125.05

1960 MHz Application Circuit (AH115-S8PCB1960)



Notes:

1. 0 Ω jumpers may be replaced with copper traces in the target application layout.
2. C8 is placed at 1.8 deg @ 1.96 GHz from C8 centerline to end of U1 pin 3.
3. C9 is placed at 20 deg @ 1.96 GHz from C9 centerline to end of U1 pin 6 and 7.

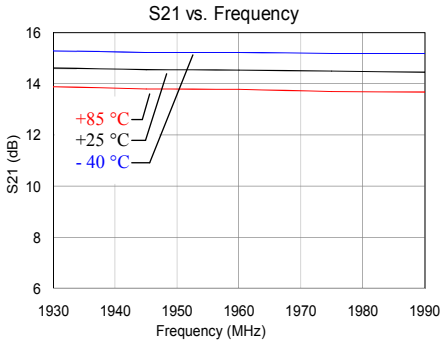
Bill of Material

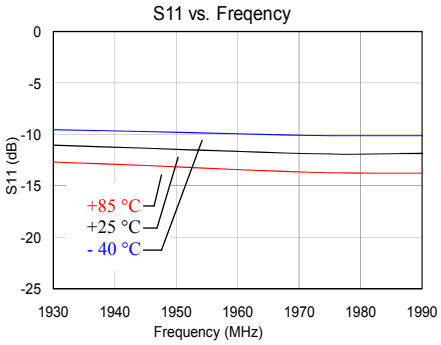
Ref Des	Value	Description	Manufacturer	Part Number
U1		High Linearity Amplifier	TriQuint	AH115-S8G
C1, C2	22 pF	Cap, Chip, 0603, 50V, 5%, NPO/COG	various	
C3	100 pF	Cap, Chip, 0603, 50 V, 5%, NPO/COG	various	
C4	10 uF	Cap, Chip, 6032, 25 V, 20%, TANT	various	
C5, C7	1000 pF	Cap, Chip, 0603, 50 V, 5%, X7R	various	
C6	10 pF	Cap, Chip, 0603, 50V, 5%, NPO/COG	various	
C8	0.8 pF	Cap, Chip, 0603, 50 V, ±0.05 pF	various	
C9	2.0 pF	Cap, Chip, 0603, 50 V, ±0.05 pF	various	
L1	18 nH	Coil, Wire Wound, 1008, 5%	various	
R1	100 Ω	Cap, Chip, 0603, 50 V, 1%, 1/16W	various	
R2	22 Ω	Res, Chip, 0603, 5%, 1/16W	various	
R3	51 Ω	Res, Chip, 0603, 5%, 1/16W	various	
R4	0 Ω	Res, Chip, 0603, 5%, 1/16W	various	
D1		Zener Diode, 5.6V	various	

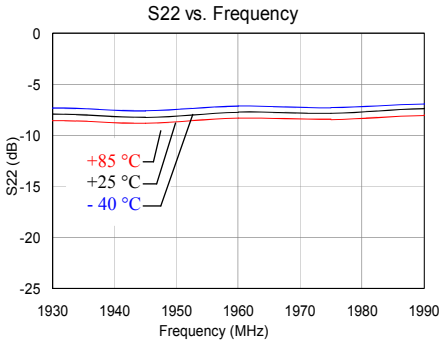
Typical Performance 1930 - 1990 MHz (AH115-S8PCB1960)

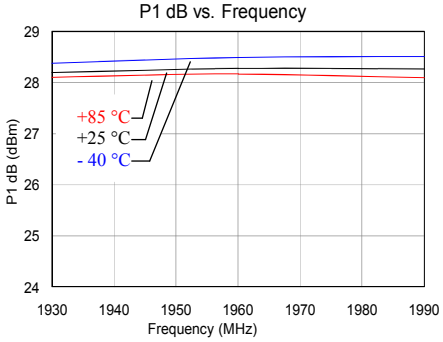
Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CQ} = 250 mA, T_{LEAD} = 25 °C

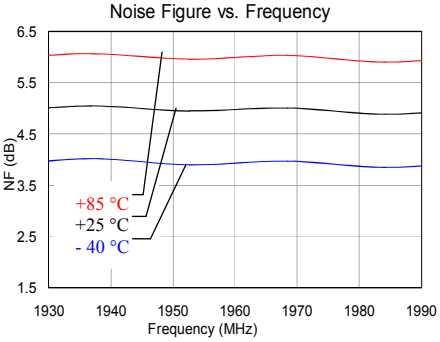
Frequency	MHz	1930	1960	1990
Gain	dB	14.3	14.3	14.3
Input Return Loss	dB	11	12	13
Output Return Loss	dB	8	8	8
OIP3 @ Pout = 11 dBm/tone, 1 MHz spacing	dBm	+43.7	+44	+44
Channel Power @-45 dBc ACPR, IS-95 9 channels fwd	dBm	+22.5	+22.5	+22.5
Noise Figure	dB	5	5	5
Output P1dB	dBm	+28.1	+28.3	+28.3
Device / Supply Voltage	V	+5		
Quiescent Current	mA	250		

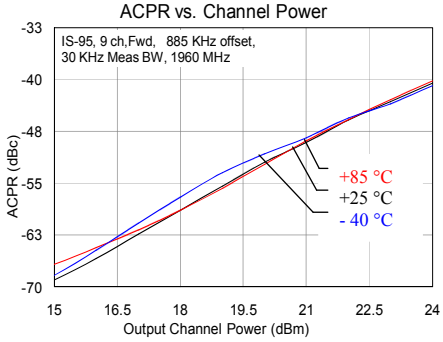


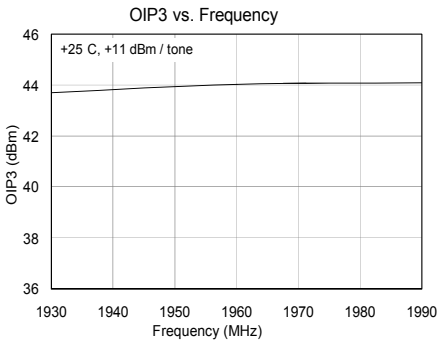


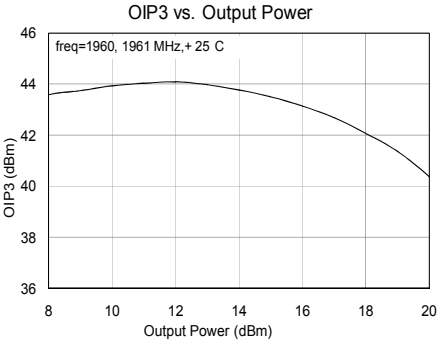


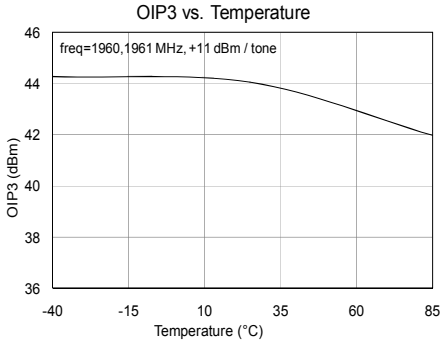




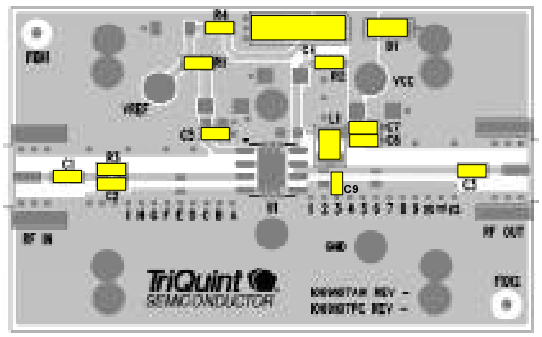


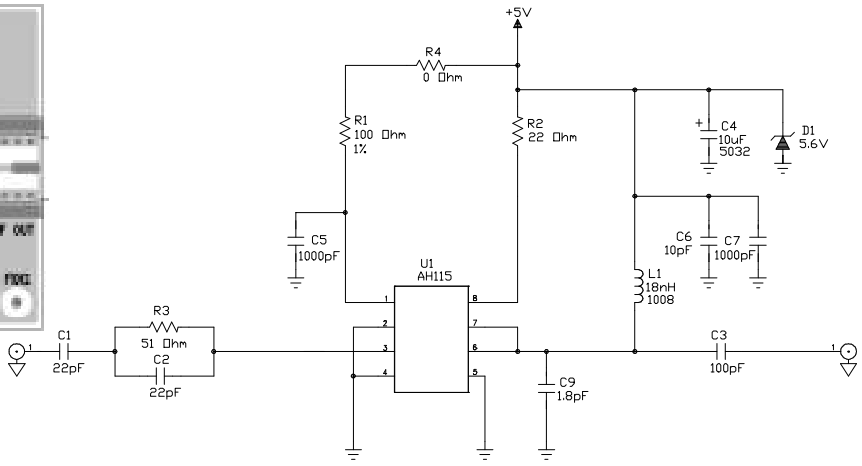






2140 MHz Application Circuit (AH115-S8PCB2140)





Notes:

1. 0 Ω jumpers may be replaced with copper traces in the target application layout.
2. C9 is placed at 13 deg @ 2.14 GHz from C9 centerline to end of U1 pin 6 and 7.

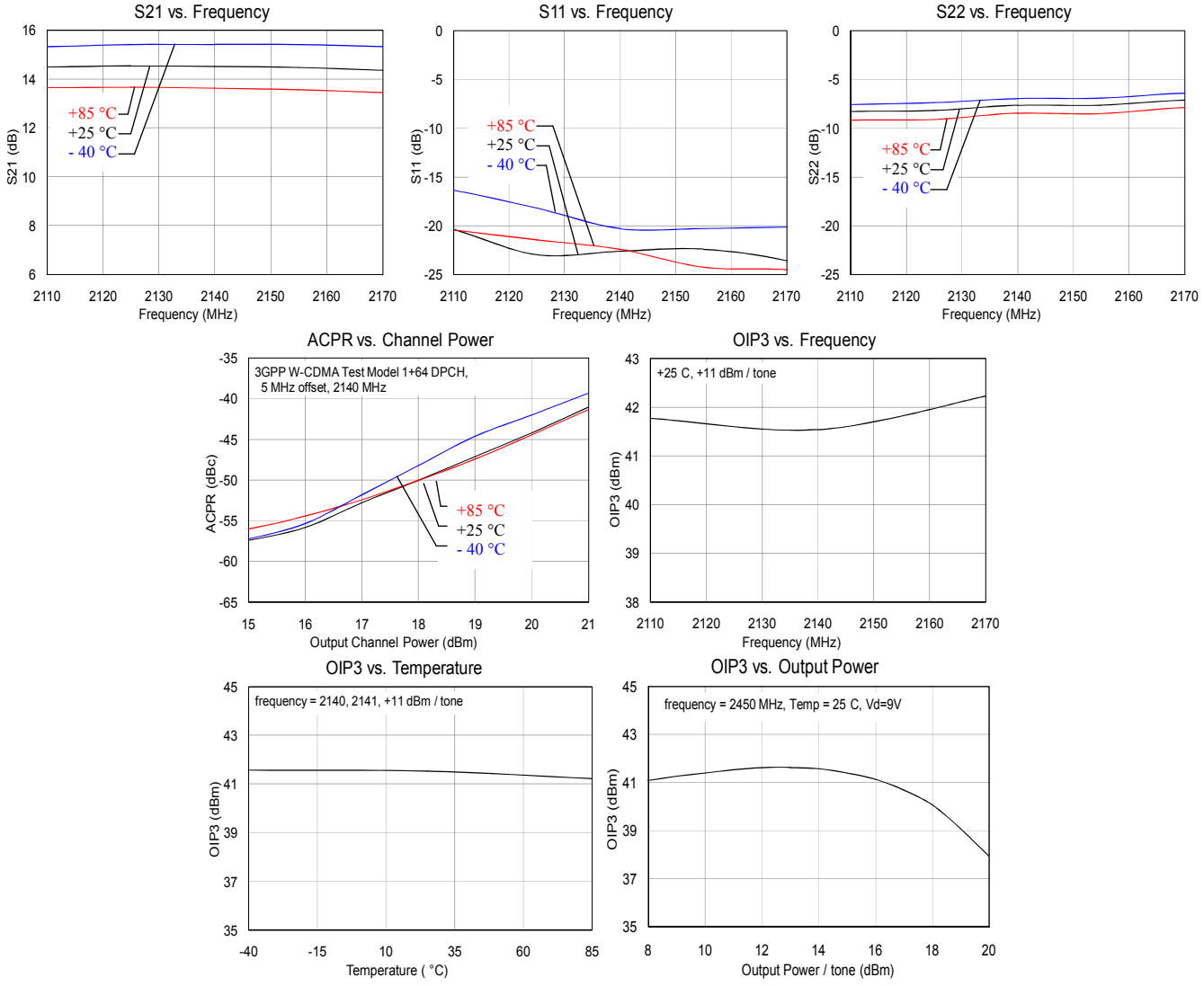
Bill of Material

Ref Des	Value	Description	Manufacturer	Part Number
U1		High Linearity Amplifier	TriQuint	AH115-S8G
C1, C2	22 pF	Cap, Chip, 0603, 50V, 5%, NPO/COG	various	
C3	100 pF	Cap, Chip, 0603, 50 V, 5%, NPO/COG	various	
C4	10 uF	Cap, Chip, 6032, 25 V, 20%, TANT	various	
C5, C7	1000 pF	Cap, Chip, 0603, 50 V, 5%, X7R	various	
C6	10 pF	Cap, Chip, 0603, 50V, 5%, NPO/COG	various	
C9	1.8 pF	Cap, Chip, 0603, 50V, ±0.05 pF	various	
L1	18 nH	Coil, Wire Wound, 1008, 5%	various	
R1	100 Ω	Cap, Chip, 0603, 50 V, 1%, 1/16W	various	
R2	22 Ω	Res, Chip, 0603, 5%, 1/16W	various	
R3	51 Ω	Res, Chip, 0603, 5%, 1/16W	various	
R4	0 Ω	Res, Chip, 0603, 5%, 1/16W	various	
D1		Zener Diode, 5.6V	various	

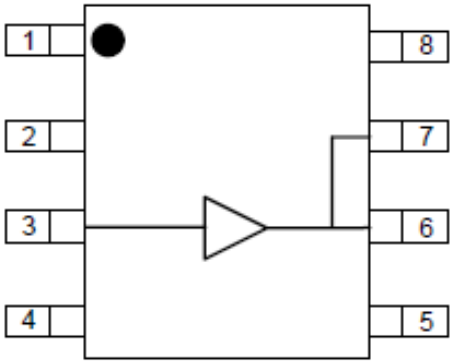
Typical Performance 2110 - 2170 MHz (AH115-S8PCB2140)

Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CQ} = 250 mA, T_{LEAD} = 25 °C

Frequency	MHz	2110	2140	2170
Gain	dB	14.4	14.4	14.3
Input Return Loss	dB	20	23	24
Output Return Loss	dB	9	8	7
OIP3 @ Pout = 11 dBm/tone, 1 MHz spacing	dBm	+41.8	+41.5	+42.3
Channel Power @-45 dBc ACPR, WCDMA, 3GPP, ±5 MHz offset	dBm	+20	+20	+20
Noise Figure	dB	5.3		
Output P1dB	dBm	+28.5		
Device / Supply Voltage	V	+5		
Quiescent Current	mA	250		



Pin Description



Pin	Symbol	Description
1	Vref	Set reference current
2, 4, 5	N/C or GND	No electrical connection. Provide an isolated or grounded solder pad for mounting integrity.
3	RF Input	RF Input. Requires matching circuit to 50 Ω. See application circuits.
6, 7	RF Output	RF Output. Requires matching circuit to 50 Ω. See application circuits.
8	Vbias	Set operating current.
Backside Paddle	GND	Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see page 9 for suggested footprint.

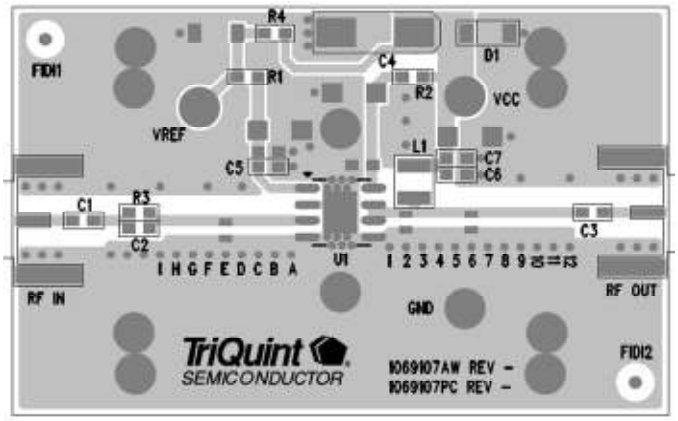
Applications Information

PC Board Layout

Circuit Board Material: .014" Getek, 4 - layer, 1 oz copper, Microstrip line details: width = .026", spacing = .026"

The silk screen markers 'A', 'B', 'C', etc. and '1', '2', '3', etc. are used as placemarkers for the input and output tuning shunt capacitors – C8 and C9. The markers and vias are spaced in .050" increments.

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.



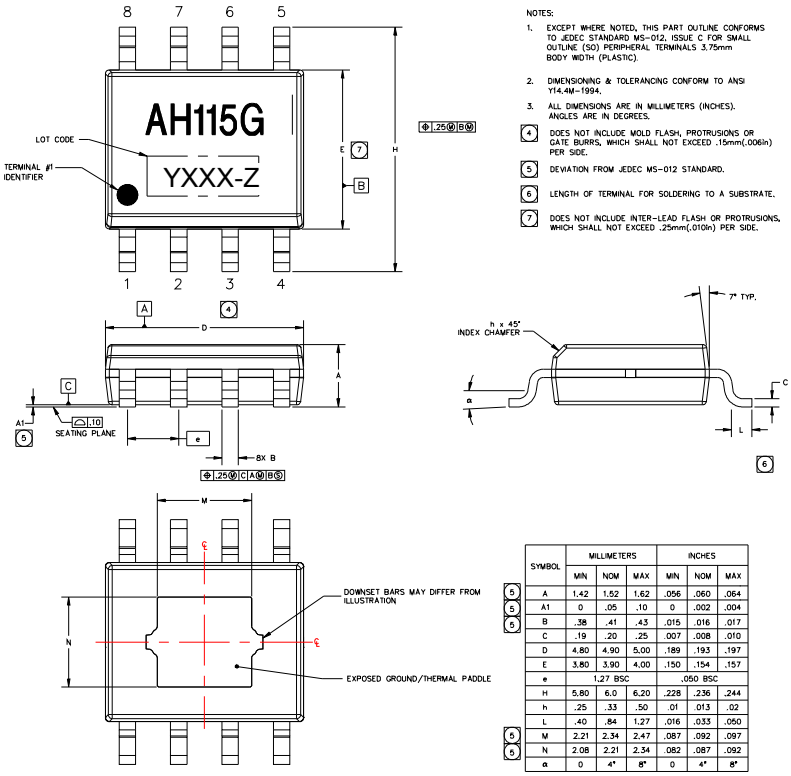
For further technical information, Refer to
http://www.triquint.com/prodserv/more_info/default.aspx?prod_id=AH115

Mechanical Information

Package Information and Dimensions

This package is lead-free/Green/RoHS-compliant. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes. The plating material on the leads is NiPdAu.

The component will be marked with an "AH115G" designator with an alphanumeric lot code on the top surface of the package.

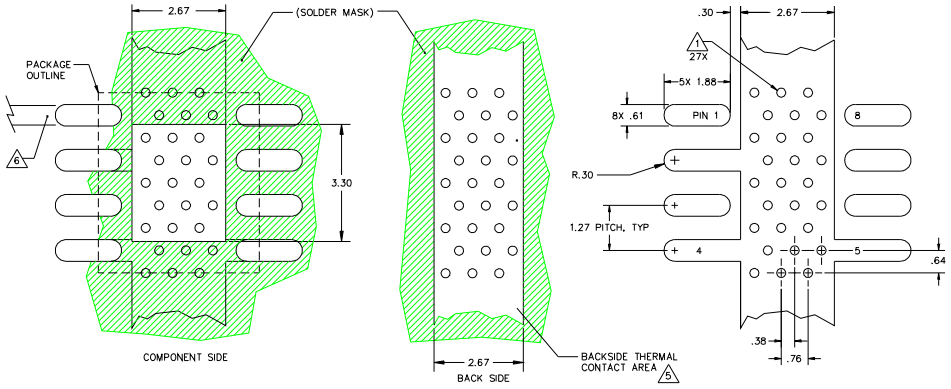


NOTES:
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MS-012, ISSUE C FOR SMALL OUTLINE (SO) PERIPHERAL TERMINALS 3.75mm BODY WIDTH (PLASTIC).
2. DIMENSIONING & TOLERANCING CONFORM TO ANSI Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES). ANGLES ARE IN DEGREES.
4. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, WHICH SHALL NOT EXCEED .15mm(.006in) PER SIDE.
5. DEVIATION FROM JEDEC MS-012 STANDARD.
6. LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS, WHICH SHALL NOT EXCEED .25mm(.010in) PER SIDE.

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.42	1.52	1.62	.056	.060	.064
A1	0	.05	.10	0	.002	.004
B	.38	.41	.43	.015	.016	.017
C	.19	.20	.25	.007	.008	.010
D	4.80	4.90	5.00	.189	.193	.197
E	3.80	3.90	4.00	.150	.154	.157
e	1.27 BSC			.050 BSC		
H	5.80	6.0	6.20	.228	.236	.244
h	.25	.33	.50	.01	.013	.02
L	.40	.84	1.27	.016	.033	.050
M	2.21	2.34	2.47	.087	.092	.097
N	2.08	2.21	2.34	.082	.087	.092
α	0	4°	8°	0	4°	8°

Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:
1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz. Copper minimum.
7. All dimensions are in millimeters (inches). Angles are in degrees.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating: Class 1B
Value: Passes between 500V and 1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

MSL Rating

Level 2 at +260 °C convection reflow
JEDEC standard J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email: info-sales@tqs.com **Fax:** +1.503.615.8902

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Email: sjcapplications.engineering@tqs.com

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