

Quad intelligent power low side switch

- Four low-side output driver with protection diagnostics designed as a conventional switch
 - 2 channels with 5 A output current capability and $r_{ON} = 0.2 \Omega$ typ.
 - 2 channels with 3 A output current capability and $r_{ON} = 0.3 \Omega$ typ.
- Integrated 60 V Zener diodes output clamping structure
- Output slope control
- Short circuit protection
- Open load detection in ON and OFF condition
- Load bypass detection
- Overload disable
- Signal and power ground loss shutdown
- Selective overtemperature shutdown
- Electrostatic discharge (ESD) protection

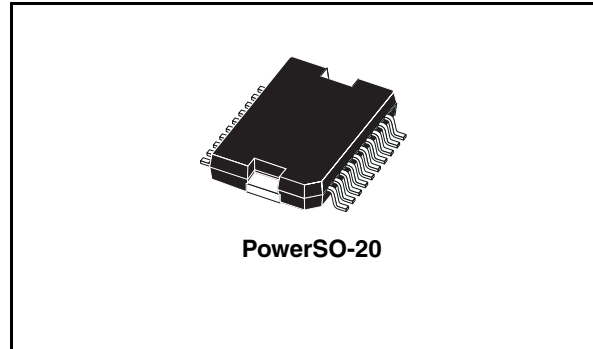
Description

The L9349 is a monolithic IC designed to drive inductive loads in low side configurations like hydraulic valves used in ABS systems.

Particular care has been taken to protect the device against failures, to avoid electromagnetic interferences and to offer extensive real time diagnostics.

The internal pull down current source at the ENable and INput pins assures, that the device is switched off, in case of open input conditions.

An output voltage slope limitation is implemented to reduce the EMI.



The device is equipped with an integrated Zener diodes clamp for fast inductive load current recirculation. This structure limits the output voltage during the recirculation phase to 50V.

The device is self-protected against short circuit at the outputs and overtemperature.

For the real time error diagnosis, the voltage and the current of the outputs are compared with internally fixed thresholds to recognize open load in OFF and ON conditions.

The output voltages are also compared with each other in OFF condition with a fixed offset, in order to recognize load bypasses.

If the over load current threshold is exceeded, the output current will be limited internally during the diagnostic overload delay switch-off time.

All four channels are monitored with a status output. The diagnostic output level in connection with different enable and input conditions allows it to recognize the different fail states.

Table 1. Device summary

Order code	Package ⁽¹⁾	Packing
L9349-LF	PowerSO-20	Tray
L9349TR-LF	PowerSO-20	Tape and reel

1. ECOPACK® package (see [Section 4: Package information](#))

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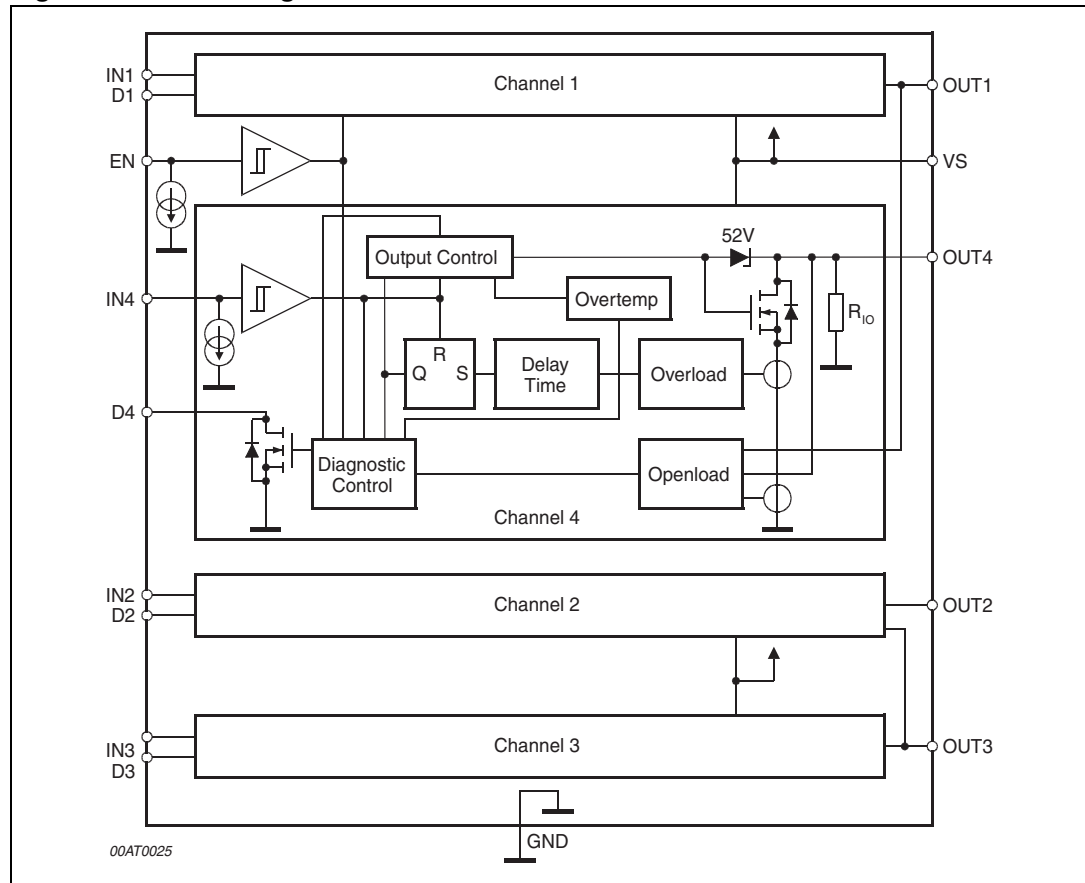
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1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. Pins connection (top view)

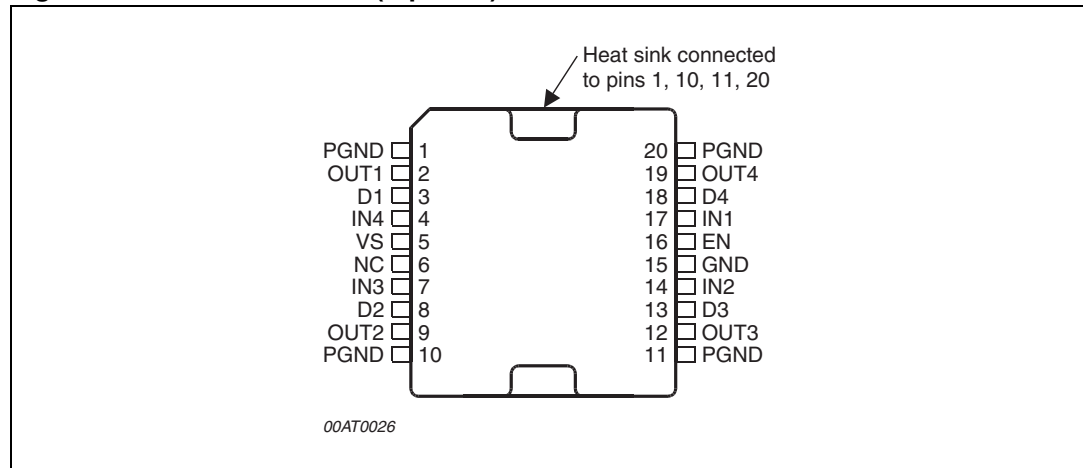


Table 2. Pins description

N°	Pin	Function
1	PGND	Power Ground
2	Out1	Output 1 (5A)
3	D1	Diagnostic 1
4	IN4	Input 4
5	VS	Supply Voltage
6	NC	Not Connected
7	IN3	Input 3
8	D2	Diagnostic 2
9	Out2	Output 2 (5A)
10	PGND	Power Ground
11	PGND	Power Ground
12	Out3	Output 3 (3A)
13	D3	Diagnostic 3
14	IN2	Input 2
15	GND	Signal Ground
16	EN	Common Enable
17	IN1	Input 1
18	D4	Diagnostic 4
19	Out4	Output 4 (3A)
20	PGND	Power Ground

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Conditions	Value	Unit
V_S	DC supply voltage		-0.3 to 32	V
V_{SP}	Supply voltage pulse (duration <200ms)		-0.3 to 45	V
$ dV_S/dt $	Supply voltage slope		10	V/ μ s
$V_{IN, EN}$	Input voltage	$ I 10mA$	-1.5 to 6	V
V_D	Diagnostic DC output voltage	$ I 50mA$	-0.3 to 16	V
V_{ODC}	DC output voltage		-0.3 to 45	V
$I_{O1, 2}$	DC output current out 1, 2		>5 (Min.) internal limited (Max.)	A
$I_{O3, 4}$	DC output current out 3, 4		>3 (Min.) internal limited (Max.)	A
$I_{OR1, 2}$	Reverse output current		-5	A
$I_{OR3, 4}$	Reverse output current		-3	A
$E_{O1, 2}$	Switch-off energy for inductive loads	$t_{EO} = 250\mu s, ^{(1)}$	50	mJ
$E_{O3, 4}$		$T = 5ms$	30	mJ
ΔV_{GND}	GND potential difference	$T_j = -40 \text{ to } 150^\circ C$	± 0.3	V
T_{jEO}	Junction temperature during switch-off	$\Sigma t \leq 30 \text{ min}$	175	$^\circ C$
		$\Sigma t \leq 15 \text{ min}$	190	$^\circ C$
T_j	Junction temperature		-40 to T_{jDIS}	$^\circ C$
T_{stg}	Storage temperature		-55 to 150	$^\circ C$
T_{jDIS}	Thermal disable junction temperature threshold		180 to 210	$^\circ C$
ESD	Electrostatical discharging	MIL883C	+2	kV
ESD	OUT1 - 4	vs. Common-GND (PGNDs + GND)	+4	kV

1. t_{EO} is the clamping time (see [Figure 3](#))

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{Th j-case}$	Thermal resistance junction to case	3	$^\circ C/W$

3.3 Electrical characteristics (operating range)

The electrical characteristics are valid within the below defined operating range, unless otherwise specified.

Table 5. Electrical characteristics (operating range)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Board supply voltage		4.5	12	32	V
T_{j1}	Junction temperature		-40		150	°C
T_{j2}		$\Sigma t \leq 15\text{min}^{(1)}$ over life time	150		T_{jDIS}	°C

1. Parameters guaranteed by correlation

3.4 Electrical characteristics

Table 6. Electrical characteristics

($V_S = 4.5$ to 32V ; $-40^\circ\text{C} \leq T_{j1} \leq 150^\circ\text{C} < T_{j2} \leq T_{jDIS}$, unless otherwise specified.)

Symbol	Parameter	Test conditions	Values T _{j1}			Values T _{j2}		Unit
			Min.	Typ.	Max.	Min.	Max.	
Supply								
I _{VS OFF}	DC supply current Off	EN = 1.0V		5	10			mA
I _{VS ON}	DC supply current On	V _s ≤ 14V; V _{IN} , V _{EN} = 2V		8				mA
Diagnostic outputs D1 - D4								
V _{DL}	Diagnostic output low voltage	I _D ≤ 3mA		0.65	1.0		1.5	V
I _{DLE}	Diagnostic output leakage current	V _D = 14V ⁽¹⁾		0.1	2		20	μA
Outputs Out 1 - Out 4								
R _{DS ON 1, 2}	Output On resistance	T _j = 25°C T _j = 150°C V _S > 9.5V I _{O1,2} = 2A		200	300 500			mΩ
R _{DS ON 3, 4}		T _j = 25°C T _j = 150°C V _S > 9.5V I _{O3,4} = 1.3A		300	450 750			mΩ
V _Z	Z-diode clamping voltage	I _{OCL} ≥ 200mA	45		60			V
R _O	Output pull down resistor	VS > 9.5V EN = 0V	10		40		50	kΩ
V _{OUV 1-4}	Open load voltage threshold	V _{IN} = 1V	0.525 x V _S	0.55 x V _S	0.575 x V _S			V

Table 6. Electrical characteristics (continued)(V_S = 4.5 to 32V; -40°C ≤ T_{j1} ≤ 150°C < T_{j2} ≤ T_{jDIS}, unless otherwise specified.)

Symbol	Parameter	Test conditions	Values T _{j1}			Values T _{j2}		Unit
			Min.	Typ.	Max.	Min.	Max.	
V _{OUV hys 1-4}	Hysteresis			0.003 x V _S				V
ΔV _{OUV 1-4, 2-3, 4-1, 3-2}	Open load difference voltage threshold	V _{IN1,4/2,3} = 1V V _S ≤ 16V V _{OC} ≥ 4.5V V _{OC} = output voltage of other channel	V _{OC} - 1.0V	V _{OC} - 1.25V	V _{OC} - 1.5V			V
ΔV _{OUV hys 1-4, 2-3, 4-1, 3-2}	Open load hysteresis			40				mV
I _{OUC 1, 2, 3, 4}	Open load current threshold	V _{EN} =V _{IN} =2V; V _S =6.5 - 16V	160	320	480			mA
I _{OOC 1, 2}	Over load current threshold	V _S > 6.5V; V _{OUT} = 32V	5	10				A
I _{OOC 3, 4}			3	6				A
T _{SD}	Thermal shut down		180	195	210			°C
T _{SD-hys}	Thermal shut down hysteresis			20				°C
I _{OUT-LE}	OUT leakage current	V _{OUT} = 20V V _S = 0V			5			μA
Inputs IN1-4, EN								
V _{IN,EN L}	Logic input/enable low voltage		-0.3		1			V
V _{IN,EN H}	Logic input/enable high voltage	IN, EN	2.0		6			V
V _{EN,IN hys}	Logic input hysteresis		50	100				mV
I _{IN}	Input sink current	2V < V _{IN} , V _{EN} < 6V ⁽²⁾	10	20	40			μA
I _{EN}	Enable sink current	V _{IN} , V _{EN} < V _S	10	20	40			μA
Timing								
t _{ON}	Output delay ON time	I _O = 1A V _S = 12V (3) Figure 4		4	25			μs
t _{f,r}	Output fall and rise time	I _O = 1A V _S = 12V Figure 4	3	10	30			μs
t _{OFF}	Output delay OFF time	I _O = 1A V _S = 12V (3) Figure 4	5	15	30			μs

Table 6. Electrical characteristics (continued)(V_S = 4.5 to 32V; -40°C ≤ T_{j1} ≤ 150°C < T_{j2} ≤ T_{jDIS}, unless otherwise specified.)

Symbol	Parameter	Test conditions	Values T _{j1}			Values T _{j2}		Unit
			Min.	Typ.	Max.	Min.	Max.	
t _{DH-L, Diag}	Diag. delay output OFF time	(3) <i>Figure 4</i>	8		65		90	μs
t _{D IOU}	Diagnostic open load delay time	9V < V _S < 16V, <i>Figure 5</i>		8	50			μs
t _{DOL}	Diagnostic overload delay switch-OFF time	9V < V _S < 16V, <i>Figure 5</i>	6		65			μs
t _{filt}	Filter time		4		24			μs
PGND								
PGND _{loss,h}	Power GND loss threshold high			3				V
PGND _{loss,l}	Power GND loss threshold low			2				V

1. The diagnostic output is short circuit protected up to V_D = 16V
2. Open pins (EN, IN) are detected as low
3. V_S = 9 to 16V ∧ I_{OUC} ≤ I_O ≤ I_{OOC}

3.5 Diagnostic

Table 7. Diagnostic

Conditions		EN	IN	OUT	DIAG.
Normal function		L	X	off	L
		H	L	off	L
		H	H	on	H
GND short	V _{Otyp} < 0.55V _S	L	X	off	H
Load bypass	ΔV _{O1-4/2-3} ≥ 1.25V	H	L	off	H
Open load	I _{O1,2,3,4typ} < 320mA	H	H	on	L
T _{jtyp} ≥ 190°C Overtemperature		X	X	off	L
Over load	I _{Omin 1,2} > 5A I _{Omin 3,4} > 3A	H	H	off	L
SGND or PGND loss	channel off	X	L	off	H
SGND or PGND loss	channel on	H	H	off	L

3.6 Circuit description

The L9349 is a quad low side driver for inductive loads like valves in automotive environment. The internal pull down current sources at the ENable and INput pins assure in case of open input conditions that the device is switched off. An output voltage slope limitation for du/dt is implemented to reduce the EMI. An integrated active flyback voltage limitation clamps the output voltage during the flyback phase to 50 V.

Each driver is protected against short circuit at $V_{OUT} < 32V$ and thermal overload. In short circuit condition the output will be disabled after a short delay time t_{DOL} . The thermal disable for $T_J > 180^{\circ}C$ of the output will be reset if the junction temperature decreases about $20^{\circ}C$ below the disable threshold temperature.

The overtemperature, overload and groundloss information is stored until IN is low.

For the real time error diagnosis the voltage and the current of the outputs are compared with internal fixed values V_{OUV} for OFF and I_{OUC} for ON conditions to recognize open load ($R_L \geq 20K\Omega$, $R_L > 38\Omega$) in OFF and ON conditions.

Also the output voltages V_{O1-4} are compared to each other output in OFF condition with a fixed offset of ΔV_{OUV} to recognize load bypasses. The ΔV_{OUV} diagnoses is suppressed during the flyback phases of the compared output. The outputs 1 and 4 are compared for ΔV_{OUV} and also outputs 2 and 3 are compared.

The diagnostic output level in connection with different ENable and INput conditions allows to recognize different fail states, like overtemp, short to V_S , short to GND, bypass to GND and disconnected load (see [Table 7: Diagnostic](#)).

The diagnostic output is protected against short circuit. Exceeding the over load current threshold I_{OOC} , the output current will be limited internally during the diagnostic overload delay switch-off time t_{DOL} .

The device complies the I_{SO} pulses imposed to the supply voltage of the valves without any failures of the functionality. Therefore some diagnostic functions are internal filtered. The following table shows the corresponding filter time for each detected signal.

Table 8. Corresponding filter time for each detected signal

	ON State EN and IN = HIGH	OFF State EN or IN, = LOW	min. Filter time	Reset done by
Overloading of output (also shorted load to supply)	X		4 μ s	INx = "LOW"
Open load (under voltage detection)		X	-	
Open load (under current detection)	X		-	
Overtemperature	X		4 μ s	INx = "LOW"
Power-signal GND-loss	X		4 μ s	INx = "LOW"
Power-signal GND-loss		X	4 μ s	
Openload difference		X	4 μ s	

Figure 3. t_{EO} clamping time

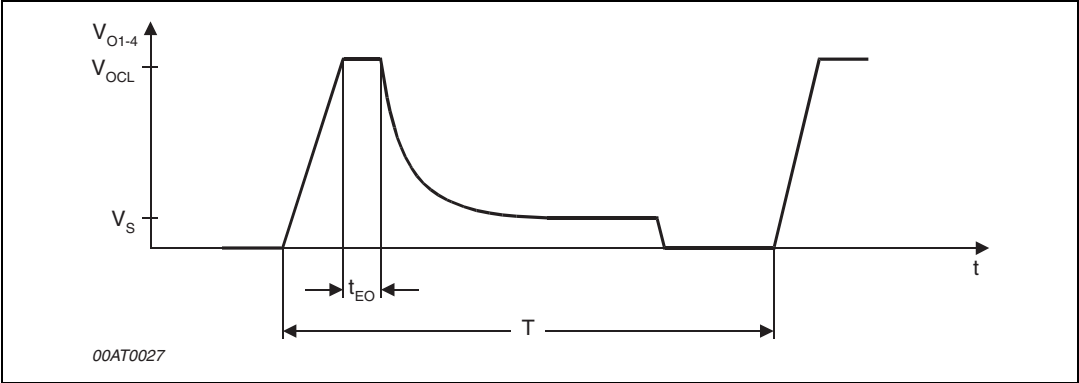


Figure 4. Output slope (resistive load for testing)

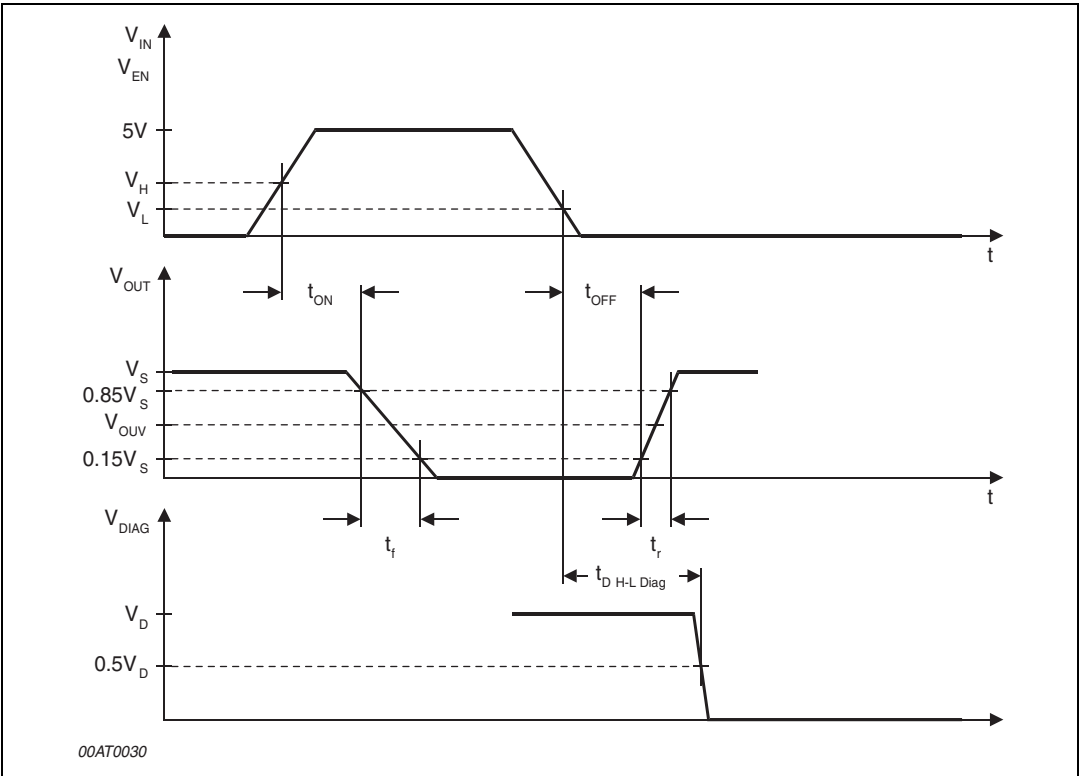


Figure 5. Timing (t_{DOL} , t_{DIOU})

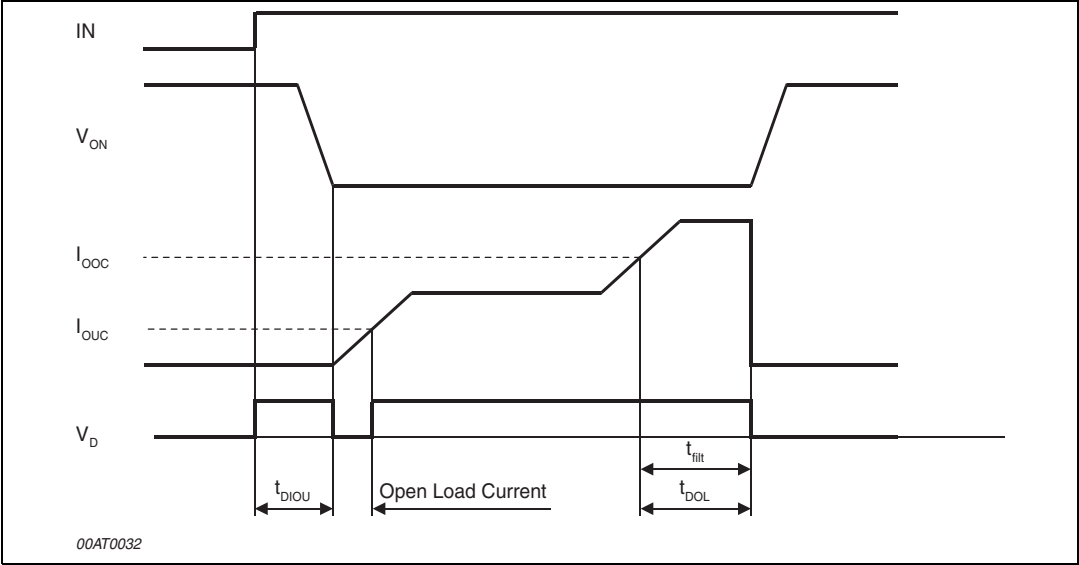


Figure 6. Block diagram - Open load voltage detection

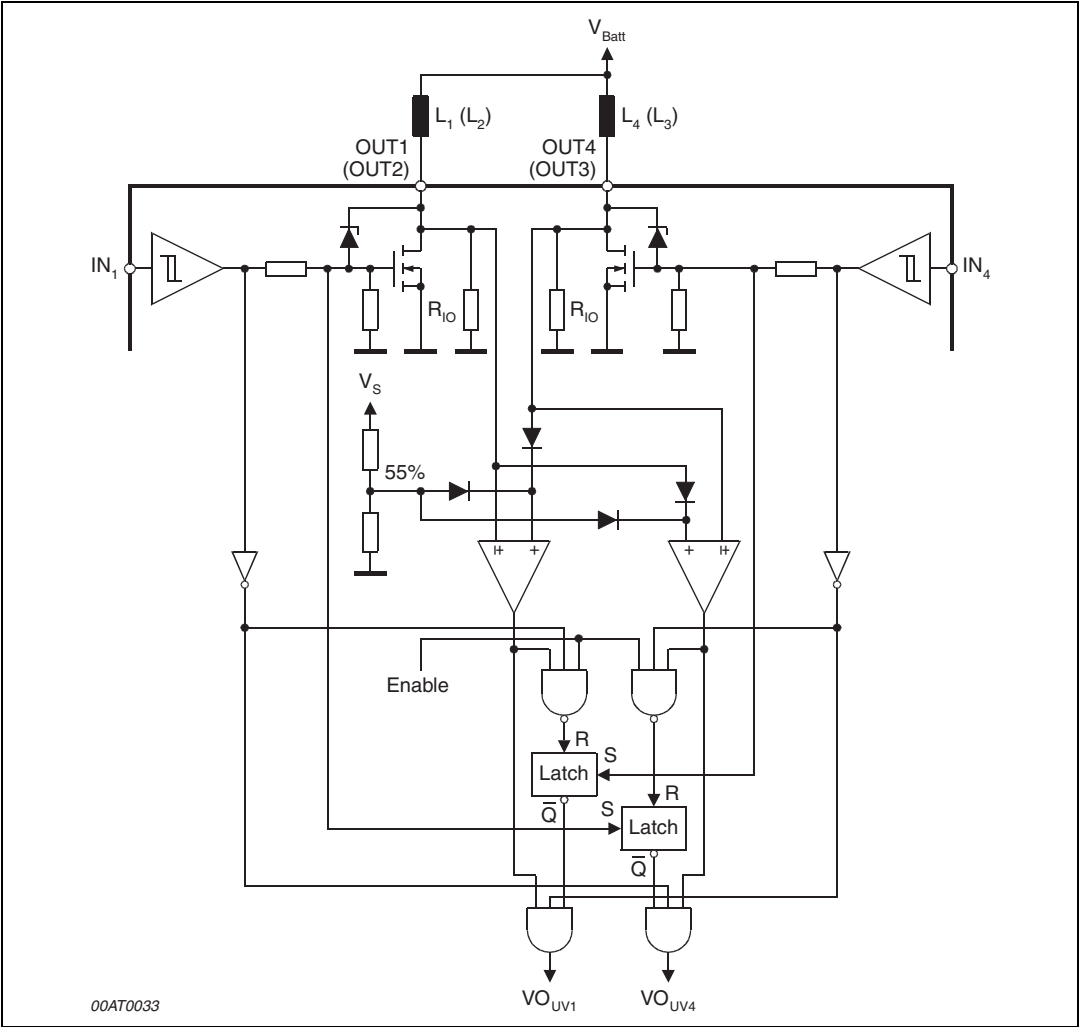


Figure 7. Logic diagram

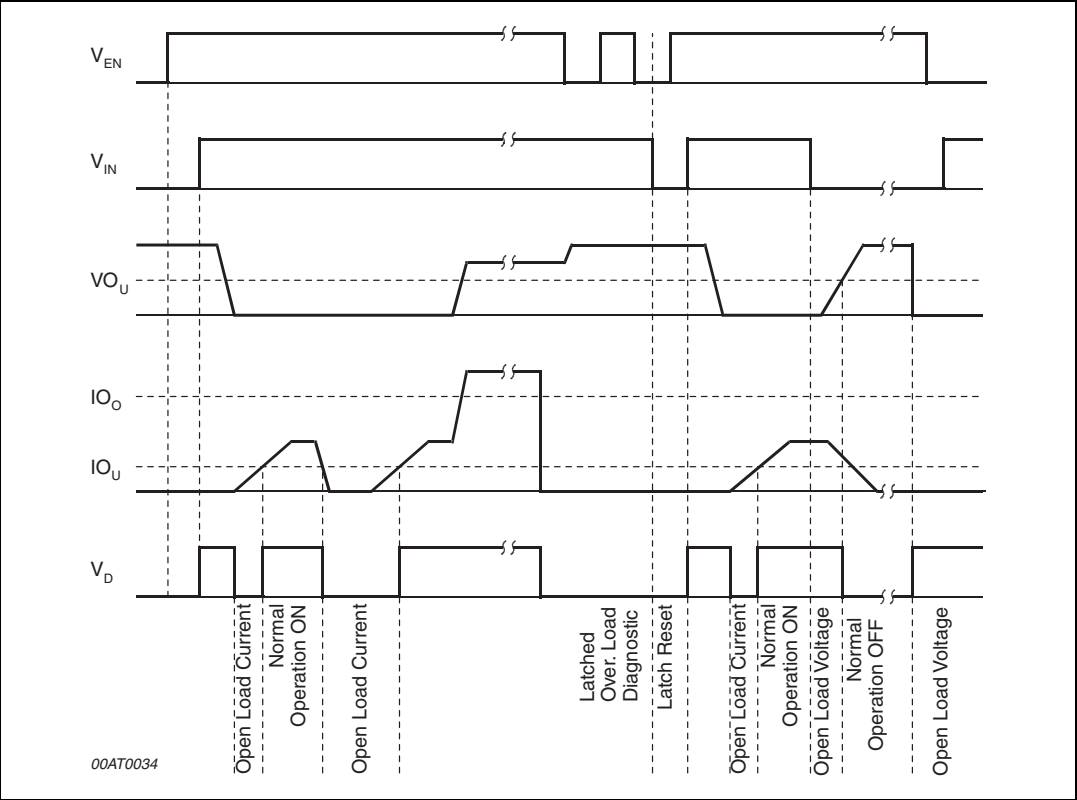
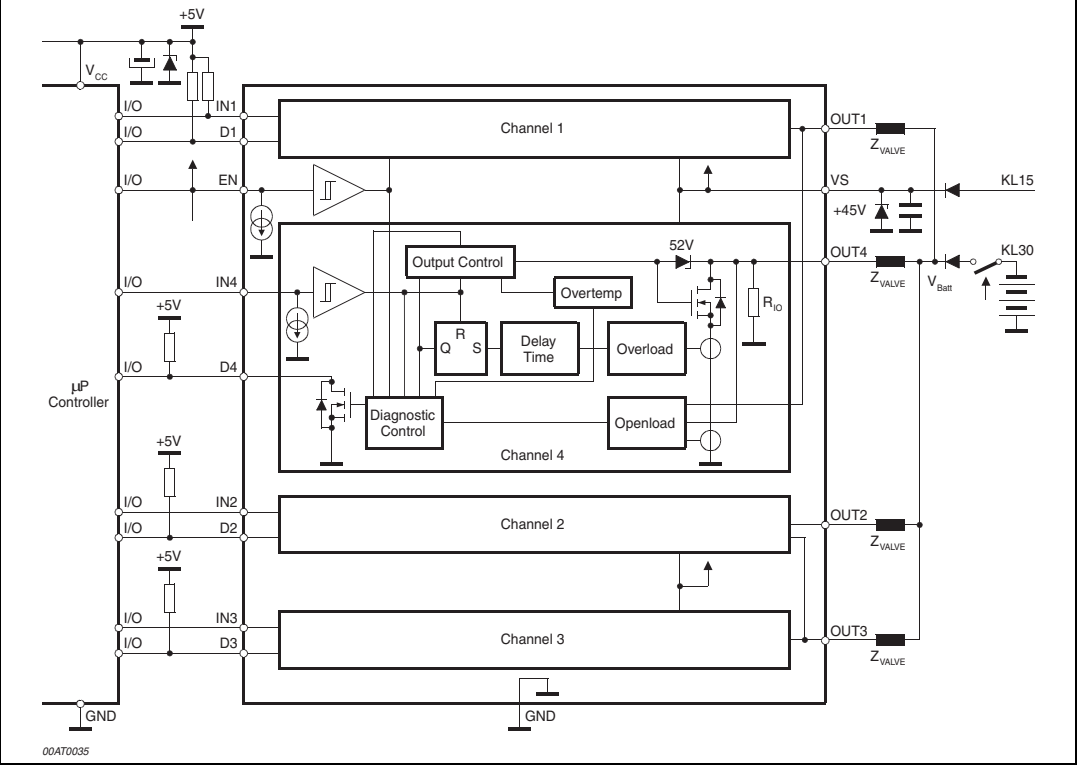


Figure 8. Application circuit diagram

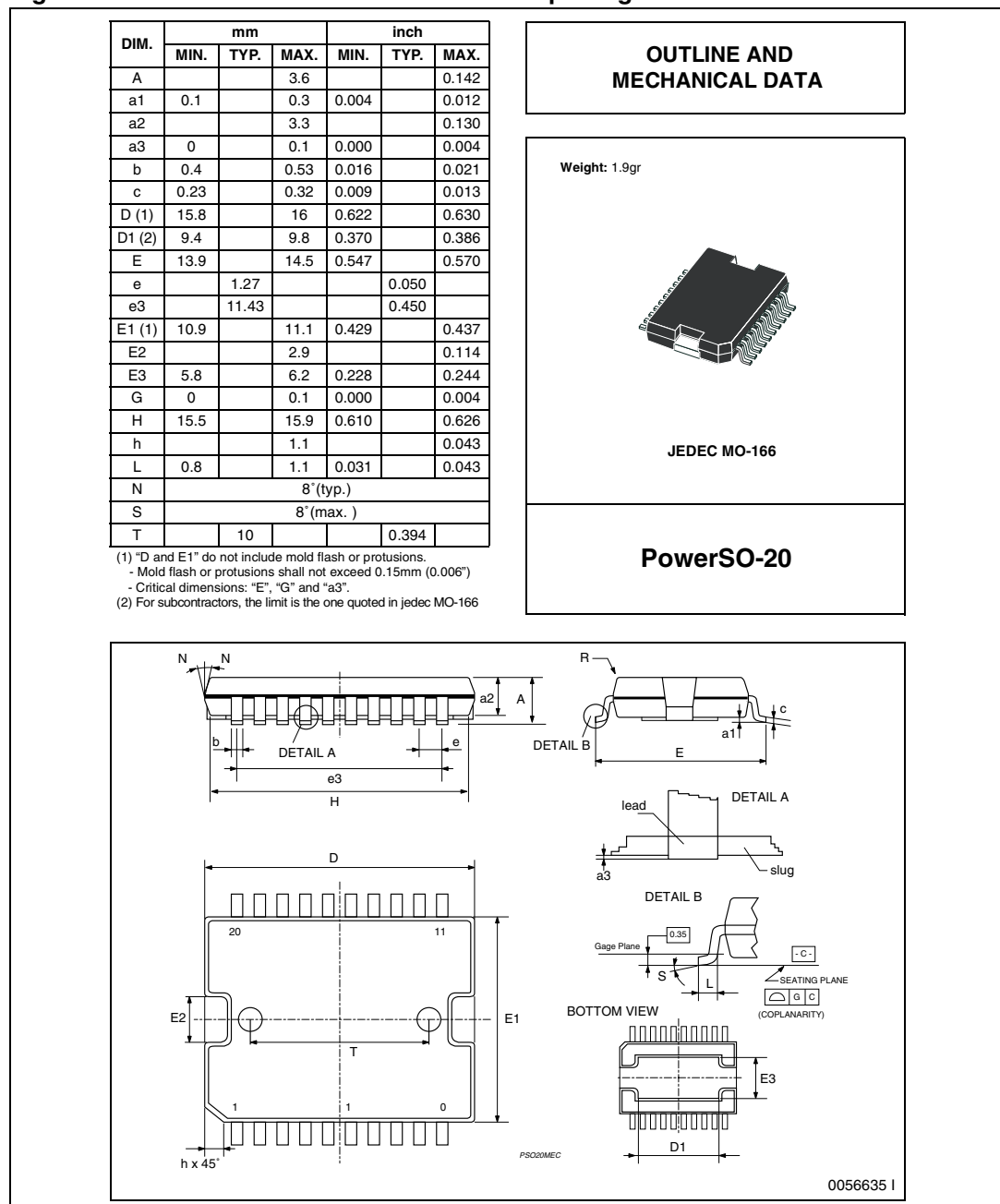


4 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK[®] packages. ECOPACK[®] packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 9. PowerSO-20 mechanical data and package dimensions



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
20-Sep-2002	4	Initial release.
09-Sep-2008	5	Document reformatted. Updated feature and description on page 1. Added Table 1: Device summary on page 1 . Updated Table 3: Absolute maximum ratings on page 7 .
20-Sep-2013	6	Updated disclaimer.

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