

| REVISIONS |                                                                                                                                                                                                                    |                 |            |
|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|------------|
| LTR       | DESCRIPTION                                                                                                                                                                                                        | DATE (YR-MO-DA) | APPROVED   |
| G         | Add case outline 2. Electrical changes in table I, 1.3, and 1.4. Editorial changes throughout. Change vendor CAGE 34371 vendor PINs and add vendor CAGE 24355. Delete vendor CAGE 32293 and add vendor CAGE 1ES66. | 94-03-24        | M. A. Frye |
| H         | Changes in accordance with NOR 5962-R135-95.                                                                                                                                                                       | 95-05-09        | M. A. Frye |
| J         | Drawing updated to reflect current requirements. Editorial changes throughout. – drw                                                                                                                               | 00-08-23        | R. Monnin  |
| K         | Drawing updated to current requirements. Editorial changes throughout. – drw                                                                                                                                       | 03-02-04        | R. Monnin  |
| L         | Make correction to Marking paragraph 3.5. - ro                                                                                                                                                                     | 05-04-05        | R. Monnin  |

**CURRENT CAGE CODE 67268**

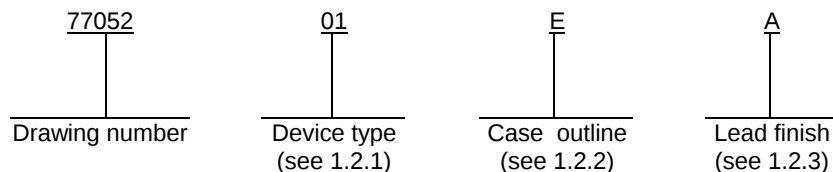
THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

|                                                                                                                                                            |    |    |  |                                   |  |   |   |   |                                                                                                                                            |                           |   |              |   |   |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |  |
|------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|--|-----------------------------------|--|---|---|---|--------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|---|--------------|---|---|----|----|----|----|----|--|--|--|--|--|--|--|--|--|--|--|
| REV                                                                                                                                                        |    |    |  |                                   |  |   |   |   |                                                                                                                                            |                           |   |              |   |   |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |  |
| SHEET                                                                                                                                                      |    |    |  |                                   |  |   |   |   |                                                                                                                                            |                           |   |              |   |   |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |  |
| REV                                                                                                                                                        | L  | L  |  |                                   |  |   |   |   |                                                                                                                                            |                           |   |              |   |   |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |  |
| SHEET                                                                                                                                                      | 15 | 16 |  |                                   |  |   |   |   |                                                                                                                                            |                           |   |              |   |   |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |  |
| REV STATUS                                                                                                                                                 |    |    |  | REV                               |  | L | L | L | L                                                                                                                                          | L                         | L | L            | L | L | L  | L  | L  | L  | L  |  |  |  |  |  |  |  |  |  |  |  |
| OF SHEETS                                                                                                                                                  |    |    |  | SHEET                             |  | 1 | 2 | 3 | 4                                                                                                                                          | 5                         | 6 | 7            | 8 | 9 | 10 | 11 | 12 | 13 | 14 |  |  |  |  |  |  |  |  |  |  |  |
| PMIC N/A                                                                                                                                                   |    |    |  | PREPARED BY<br>A. J. Foley        |  |   |   |   | <b>DEFENSE SUPPLY CENTER COLUMBUS</b><br><b>COLUMBUS, OHIO 43218-3990</b><br><a href="http://www.dscc.dla.mil">http://www.dscc.dla.mil</a> |                           |   |              |   |   |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |  |
| <b>STANDARD MICROCIRCUIT DRAWING</b><br><br>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE<br><br>AMSC N/A |    |    |  | CHECKED BY<br>C. R. Jackson       |  |   |   |   |                                                                                                                                            |                           |   |              |   |   |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |  |
|                                                                                                                                                            |    |    |  | APPROVED BY<br>N. A. Hauck        |  |   |   |   |                                                                                                                                            |                           |   |              |   |   |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |  |
|                                                                                                                                                            |    |    |  | DRAWING APPROVAL DATE<br>77-10-26 |  |   |   |   |                                                                                                                                            |                           |   |              |   |   |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |  |
|                                                                                                                                                            |    |    |  | REVISION LEVEL<br>L               |  |   |   |   | SIZE<br>A                                                                                                                                  | CAGE CODE<br><b>14933</b> |   | <b>77052</b> |   |   |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |  |
|                                                                                                                                                            |    |    |  |                                   |  |   |   |   |                                                                                                                                            | SHEET 1 OF 16             |   |              |   |   |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |  |

## 1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

| <u>Device type</u> | <u>Generic number</u>   | <u>Circuit function</u>                                                      |
|--------------------|-------------------------|------------------------------------------------------------------------------|
| 01                 | DG508A, HI-508, ADG508A | CMOS, positive logic, 8-channel analog MUX/DEMUX                             |
| 02                 | HI-508A, HI-548         | CMOS, positive logic, 8-channel analog MUX/DEMUX with overvoltage protection |
| 03                 | MAX358                  | CMOS, positive logic, 8-channel analog MUX/DEMUX with overvoltage protection |

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| <u>Outline letter</u> | <u>Descriptive designator</u> | <u>Terminals</u> | <u>Package style</u>         |
|-----------------------|-------------------------------|------------------|------------------------------|
| 2                     | CQCC1-N20                     | 20               | Square leadless chip carrier |
| E                     | GDIP1-T16 or CDIP2-T16        | 16               | Dual-in-line                 |
| F                     | GDFP2-F16 or CDFP3-F16        | 16               | Flat pack                    |
| X                     | CDFP4-F16                     | 16               | Flat pack                    |

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

## 1.3 Absolute maximum ratings.

Supply voltage between V+ and V-:

Device type 01 ..... +44 V dc

Device types 02 and 03 ..... +40 V dc

V+ to ground:

Device type 01 ..... +22 V dc

Device types 02 and 03 ..... +20 V dc

V- to ground:

Device type 01 ..... -22 V dc

Device types 02 and 03 ..... -20 V dc

Digital input overvoltage range:

Device types 02 and 03 ..... (V-) - 4.0 V dc to (V+) + 4.0 V dc

Analog input overvoltage range:

Device type 01 ..... (V-) - 3.0 V dc to (V+)

Analog input voltage (V<sub>S</sub>):

Device type 01 ..... (V-) - 2 V dc to (V+) + 2 V dc

Device types 02 and 03 ..... (V-) - 20 V dc to (V+) + 20 V dc

**STANDARD  
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DEFENSE SUPPLY CENTER COLUMBUS  
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### 1.3 Absolute maximum ratings – continued.

|                                                               |                                         |
|---------------------------------------------------------------|-----------------------------------------|
| Storage temperature range .....                               | -65°C to +150°C                         |
| Power dissipation (P <sub>D</sub> ):                          |                                         |
| Case 2 .....                                                  | 1.23 W at T <sub>A</sub> = +75°C        |
| Case E .....                                                  | 470 mW at T <sub>A</sub> = +75°C        |
| Case F and X .....                                            | 725 mW at T <sub>A</sub> = +75°C        |
| Derating factor:                                              |                                         |
| Case 2 .....                                                  | 12.3 mW/°C above T <sub>A</sub> = +75°C |
| Case E .....                                                  | 12.0 mW/°C above T <sub>A</sub> = +75°C |
| Case F and X .....                                            | 8.0 mW/°C above T <sub>A</sub> = +25°C  |
| Thermal resistance, junction-to-case (θ <sub>JC</sub> ) ..... | See MIL-STD-1835                        |
| Lead temperature (soldering, 10 seconds) .....                | +300°C                                  |
| Junction temperature (T <sub>J</sub> ) .....                  | +175°C                                  |

### 1.4 Recommended operating conditions.

|                                                                |                                          |
|----------------------------------------------------------------|------------------------------------------|
| Positive supply voltage (V <sub>+</sub> ) .....                | +15 V dc                                 |
| Negative supply voltage (V <sub>-</sub> ) .....                | -15 V dc                                 |
| Logic low level address input voltage (V <sub>IL</sub> ) ..... | 0 V dc to 0.8 V dc                       |
| Logic high level address input voltage (V <sub>IH</sub> ):     |                                          |
| Device types 01 and 03 .....                                   | 2.4 V dc to (V <sub>+</sub> ) - 0.7 V dc |
| Device type 02 .....                                           | 4.0 V dc to V <sub>+</sub>               |
| Enable voltage (V <sub>EN</sub> ):                             |                                          |
| Device type 01 .....                                           | 4.5 V dc to (V <sub>+</sub> ) - 0.7 V dc |
| Device type 02 .....                                           | 4.0 V dc to (V <sub>+</sub> ) - 0.7 V dc |
| Device type 03 .....                                           | 2.4 V dc to (V <sub>+</sub> ) - 0.7 V dc |
| Ambient operating temperature range (T <sub>A</sub> ) .....    | -55°C to +125°C                          |

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

|                                                                                                 |           |                     |            |
|-------------------------------------------------------------------------------------------------|-----------|---------------------|------------|
| STANDARD<br>MICROCIRCUIT DRAWING<br>DEFENSE SUPPLY CENTER COLUMBUS<br>COLUMBUS, OHIO 43218-3990 | SIZE<br>A |                     | 77052      |
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2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

|                                                                                                 |           |                     |            |
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TABLE I. Electrical performance characteristics.

| Test                                                        | Symbol               | Conditions <u>1/</u><br>V- = -15 V, V+ = +15 V,<br>V <sub>EN</sub> = 4.5 V<br><br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br>unless otherwise specified | Group A<br>subgroups | Device<br>type | Limits |      | Unit |
|-------------------------------------------------------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------|--------|------|------|
|                                                             |                      |                                                                                                                                                 |                      |                | Min    | Max  |      |
| Input leakage current <u>2/</u>                             | I <sub>IH</sub>      | Measure address inputs sequentially, connect all                                                                                                | 1,2                  | 01             |        | +0.8 | μA   |
|                                                             | I <sub>IL</sub>      | unused address inputs to 5.0 V                                                                                                                  |                      |                |        | -0.8 |      |
| Leakage current into the source terminal of an "OFF" switch | +I <sub>S(OFF)</sub> | V <sub>S</sub> = +10 V, V <sub>EN</sub> = 0.8 V, all unused inputs = -10 V                                                                      | 1,2,3                | 01             | -50    | +50  | nA   |
|                                                             | -I <sub>S(OFF)</sub> | V <sub>S</sub> = -10 V, V <sub>EN</sub> = 0.8 V, all unused inputs = +10 V                                                                      |                      |                |        |      |      |
| Leakage current into the drain terminal of an "OFF" switch  | +I <sub>D(OFF)</sub> | V <sub>D</sub> = +10 V, V <sub>EN</sub> = 0.8 V, all unused inputs = -10 V                                                                      | 1,2,3                | 01             | -250   | +250 | nA   |
|                                                             | -I <sub>D(OFF)</sub> | V <sub>D</sub> = -10 V, V <sub>EN</sub> = 0.8 V, all unused inputs = +10 V                                                                      |                      |                |        |      |      |
| Leakage current from an "ON" driver into the switch (drain) | +I <sub>D(ON)</sub>  | V <sub>D</sub> = +10 V, V <sub>S</sub> = -10 V, all unused inputs = -10 V                                                                       | 1,2,3                | 01             | -250   | +250 | nA   |
|                                                             | -I <sub>D(ON)</sub>  | V <sub>D</sub> = -10 V, V <sub>S</sub> = +10 V, all unused inputs = +10 V                                                                       |                      |                |        |      |      |
| Positive supply current                                     | I(+)                 | V <sub>A</sub> = 0 V, V <sub>EN</sub> = 5 V                                                                                                     | 1,2,3                | 01             |        | +12  | mA   |
| Negative supply current                                     | I(-)                 | V <sub>A</sub> = 0 V, V <sub>EN</sub> = 5 V                                                                                                     | 1,2,3                | 01             | -12    |      | mA   |
| Standby positive supply current                             | +I <sub>SBY</sub>    | V <sub>A</sub> = 0 V, V <sub>EN</sub> = 0 V                                                                                                     | 1, 2, 3              | 01             |        | +3.5 | mA   |
| Standby negative supply current                             | -I <sub>SBY</sub>    | V <sub>A</sub> = 0 V, V <sub>EN</sub> = 0 V                                                                                                     | 1, 2, 3              | 01             | -3.5   |      | mA   |
| Switch "ON" resistance                                      | R <sub>DS1</sub>     | V <sub>S</sub> = +10 V, I <sub>D</sub> = +1 mA                                                                                                  | 1, 3                 | 01             |        | 400  | Ω    |
|                                                             |                      |                                                                                                                                                 | 2                    |                |        | 500  |      |
|                                                             |                      | V <sub>S</sub> = -10 V, I <sub>D</sub> = -1 mA                                                                                                  | 1, 3                 |                |        | 400  |      |
|                                                             |                      |                                                                                                                                                 | 2                    |                |        | 500  |      |
| Switch "ON" resistance                                      | R <sub>DS2</sub>     | V+ = +10 V, V- = -10 V, V <sub>S</sub> = +7.5 V, I <sub>D</sub> = -1 mA                                                                         | 1, 2, 3              | 01             |        | 1000 | Ω    |
|                                                             |                      | V+ = +10 V, V- = +10 V, V <sub>S</sub> = -7.5 V, I <sub>D</sub> = -1 mA                                                                         |                      |                |        | 1000 |      |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

| Test                                                          | Symbol               | Conditions <u>1/</u><br>V- = -15 V, V+ = +15 V,<br>V <sub>EN</sub> = 4.5 V<br><br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br>unless otherwise specified | Group A<br>subgroups | Device<br>type | Limits |      | Unit |
|---------------------------------------------------------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------|--------|------|------|
|                                                               |                      |                                                                                                                                                 |                      |                | Min    | Max  |      |
| Capacitance: Address                                          | C <sub>A</sub>       | V+ = V- = 0 V, <u>3/</u><br>f = 1 MHz, T <sub>A</sub> = +25°C                                                                                   | 4                    | 01             |        | 10   | pF   |
| Capacitance: output switch                                    | C <sub>OS</sub>      | V+ = V- = 0 V, <u>3/</u><br>f = 1 MHz, T <sub>A</sub> = +25°C                                                                                   | 4                    | 01             |        | 45   | pF   |
| Capacitance: input switch                                     | C <sub>IS</sub>      | V+ = V- = 0 V, <u>3/</u><br>f = 1 MHz, T <sub>A</sub> = +25°C                                                                                   | 4                    | 01             |        | 10   | pF   |
| Charge transfer error                                         | V <sub>CTE</sub>     | V <sub>S</sub> = GND, <u>3/</u><br>V <sub>GEN</sub> = 0 V to 5 V,<br>f = 500 kHz, C <sub>L</sub> = 100 pF,<br>T <sub>A</sub> = +25°C            | 4                    | 01             |        | 10   | mV   |
| Single channel isolation                                      | V <sub>ISO</sub>     | V <sub>GEN</sub> = 1 V <sub>P-P</sub> , <u>3/</u><br>f = 200 kHz, T <sub>A</sub> = +25°C                                                        | 4                    | 01             | 50     |      | dB   |
| Crosstalk between<br>channels                                 | V <sub>CT</sub>      | V <sub>GEN</sub> = 1 V <sub>P-P</sub> , <u>3/</u><br>f = 200 kHz, T <sub>A</sub> = +25°C                                                        | 4                    | 01             | 50     |      | dB   |
| Break-before-make time<br>delay                               | t <sub>D</sub>       | T <sub>A</sub> = +25°C, see figure 3                                                                                                            | 9                    | 01             | 5      |      | ns   |
| Propagation delay times:<br>Address inputs to<br>I/O channels | t <sub>ON(A)</sub>   | R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 100 pF,<br>see figure 4                                                                                 | 9, 11                | 01             |        | 1000 | ns   |
|                                                               | t <sub>OFF(A)</sub>  |                                                                                                                                                 | 10                   |                |        | 1500 |      |
| Enable to I/O                                                 | t <sub>ON(EN)</sub>  | R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 100 pF,<br>see figure 5                                                                                 | 9, 11                | 01             |        | 1000 | ns   |
|                                                               | t <sub>OFF(EN)</sub> |                                                                                                                                                 | 10                   |                |        | 1500 |      |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

| Test                                                                              | Symbol                            | Conditions <u>1/</u><br>V- = -15 V, V+ = +15 V,<br>V <sub>EN</sub> = 4.0 V<br><br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br>unless otherwise specified | Group A<br>subgroups | Device<br>type | Limits |      | Unit |
|-----------------------------------------------------------------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------|--------|------|------|
|                                                                                   |                                   |                                                                                                                                                 |                      |                | Min    | Max  |      |
| Positive input clamping voltage                                                   | V <sub>IC(POS)</sub>              | I <sub>IN</sub> = 1 mA, <u>3/</u><br>V+ = V- = 0 V, T <sub>A</sub> = +25°C                                                                      | 1                    | 02             |        | +1.5 | V    |
| Negative input clamping voltage                                                   | V <sub>IC(NEG)</sub>              | I <sub>IN</sub> = -1 mA, <u>3/</u><br>V+ = V- = 0 V, T <sub>A</sub> = +25°C                                                                     | 1                    | 02             | -1.5   |      | V    |
| Input leakage current <u>2/</u>                                                   | I <sub>IH</sub>                   | Measure inputs sequentially, connect all unused inputs to GND                                                                                   | 1,2                  | 02             | -1.0   | +1.0 | μA   |
|                                                                                   | I <sub>IL</sub>                   |                                                                                                                                                 |                      |                | +1.0   | -1.0 |      |
| Leakage current into the source terminal of an "OFF" switch                       | +I <sub>S(OFF)</sub>              | V <sub>S</sub> = +10 V, V <sub>EN</sub> = 0.8 V,<br>V <sub>D</sub> = -10 V,<br>all unused inputs = -10 V                                        | 1,2                  | 02             | -50    | +50  | nA   |
|                                                                                   | -I <sub>S(OFF)</sub>              | V <sub>S</sub> = -10 V, V <sub>EN</sub> = 0.8 V,<br>V <sub>D</sub> = +10 V,<br>all unused inputs = +10 V                                        |                      |                |        |      |      |
| Leakage current into the drain terminal of an "OFF" switch                        | +I <sub>D(OFF)</sub>              | V <sub>D</sub> = +10 V, V <sub>EN</sub> = 0.8 V,<br>all unused inputs = -10 V                                                                   | 1,2                  | 02             | -250   | +250 | nA   |
|                                                                                   | -I <sub>D(OFF)</sub>              | V <sub>D</sub> = -10 V, V <sub>EN</sub> = 0.8 V,<br>all unused inputs = +10 V                                                                   |                      |                |        |      |      |
| Leakage current from an "ON" driver into the switch (drain)                       | +I <sub>D(ON)</sub>               | V <sub>D</sub> = +10 V, V <sub>S</sub> = +10 V,<br>all unused inputs = -10 V                                                                    | 1,2,3                | 02             | -250   | +250 | nA   |
|                                                                                   | -I <sub>D(ON)</sub>               | V <sub>D</sub> = -10 V, V <sub>S</sub> = -10 V,<br>all unused inputs = +10 V                                                                    |                      |                |        |      |      |
| Overvoltage protected, leakage current into the drain terminal of an "OFF" switch | +I <sub>D(OFF)</sub> over-voltage | V <sub>S</sub> = +33 V, V <sub>D</sub> = 0 V,<br>V <sub>EN</sub> = 0.8 V                                                                        | 1,2,3                | 02             | -2.0   | +2.0 | μA   |
|                                                                                   | -I <sub>D(OFF)</sub> over-voltage | V <sub>S</sub> = -33 V, V <sub>D</sub> = 0 V,<br>V <sub>EN</sub> = 0.8 V                                                                        |                      |                |        |      |      |
| Positive supply current                                                           | I(+)                              | V <sub>A</sub> = 0 V, V <sub>EN</sub> = 4 V                                                                                                     | 1,2,3                | 02             |        | +2.0 | mA   |
| Negative supply current                                                           | I(-)                              | V <sub>A</sub> = 0 V, V <sub>EN</sub> = 4 V                                                                                                     | 1,2,3                | 02             | -1.0   |      | mA   |
| Standby positive supply current                                                   | +I <sub>SBY</sub>                 | V <sub>A</sub> = 0 V, V <sub>EN</sub> = 0 V                                                                                                     | 1, 2, 3              | 02             |        | +2.0 | mA   |
| Standby negative supply current                                                   | -I <sub>SBY</sub>                 | V <sub>A</sub> = 0 V, V <sub>EN</sub> = 0 V                                                                                                     | 1, 2, 3              | 02             | -1.0   |      | mA   |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

| Test                                                          | Symbol               | Conditions <u>1/</u><br>V- = -15 V, V+ = +15 V,<br>V <sub>EN</sub> = 4.0 V<br><br>-55°C ≤ T <sub>A</sub> ≤ +125°C unless<br>otherwise specified                           | Group A<br>subgroups | Device<br>type | Limits |      | Unit |
|---------------------------------------------------------------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------|--------|------|------|
|                                                               |                      |                                                                                                                                                                           |                      |                | Min    | Max  |      |
| Switch “ON” resistance                                        | +R <sub>DS1</sub>    | V <sub>S</sub> = +10 V, I <sub>D</sub> = -100 μA                                                                                                                          | 1                    | 02             |        | 1500 | Ω    |
|                                                               |                      |                                                                                                                                                                           | 2,3                  |                |        | 1800 |      |
|                                                               | -R <sub>DS1</sub>    | V <sub>S</sub> = -10 V, I <sub>D</sub> = -100 μA                                                                                                                          | 1                    |                |        | 1500 | Ω    |
|                                                               |                      |                                                                                                                                                                           | 2,3                  |                |        | 1800 |      |
| Difference in switch “ON”<br>resistance between<br>channels   | +ΔR <sub>DS1</sub>   | (+R <sub>DS1</sub> max) – (+R <sub>DS1</sub> min) x<br>100 / +R <sub>DS1</sub> AVE,<br>T <sub>A</sub> = +25°C                                                             | 1                    | 02             |        | 7    | %    |
|                                                               | -ΔR <sub>DS1</sub>   | (-R <sub>DS1</sub> max) – (-R <sub>DS1</sub> min) x<br>100 / -R <sub>DS1</sub> AVE,<br>T <sub>A</sub> = +25°C                                                             | 1                    |                |        | 7    |      |
| Capacitance: Address                                          | C <sub>A</sub>       | V+ = V- = 0 V, <u>3/</u><br>f = 1 MHz, T <sub>A</sub> = +25°C                                                                                                             | 4                    | 02             |        | 10   | pF   |
| Capacitance: output<br>switch                                 | C <sub>OS</sub>      | V+ = V- = 0 V, <u>3/</u><br>f = 1 MHz, T <sub>A</sub> = +25°C                                                                                                             | 4                    | 02             |        | 45   | pF   |
| Capacitance: input<br>switch                                  | C <sub>IS</sub>      | V+ = V- = 0 V, <u>3/</u><br>f = 1 MHz, T <sub>A</sub> = +25°C                                                                                                             | 4                    | 02             |        | 15   | pF   |
| Charge transfer error                                         | V <sub>CTE</sub>     | V <sub>S</sub> = GND, <u>3/</u><br>V <sub>GEN</sub> = 0 V to 5 V,<br>T <sub>A</sub> = +25°C                                                                               | 4                    | 02             |        | 10   | mV   |
| Off isolation                                                 | V <sub>ISO</sub>     | V <sub>GEN</sub> = 0.8 V <sub>P-P</sub> , <u>3/</u><br>f = 100 kHz, V <sub>S</sub> = 7 V rms,<br>R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 15 pF,<br>T <sub>A</sub> = +25°C | 4                    | 02             | 50     |      | dB   |
| Break-before-make time<br>delay                               | t <sub>D</sub>       | R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 12.5 pF, <u>3/</u><br>T <sub>A</sub> = +25°C, see figure 3                                                                        | 9                    | 02             | 5      |      | ns   |
| Propagation delay times:<br>Address inputs to<br>I/O channels | t <sub>ON(A)</sub>   | R <sub>L</sub> = 1 MΩ, C <sub>L</sub> = 14 pF,<br>see figure 4                                                                                                            | 9                    | 02             |        | 500  | ns   |
|                                                               | t <sub>OFF(A)</sub>  |                                                                                                                                                                           | 10,11                |                |        | 1000 |      |
| Enable to I/O                                                 | t <sub>ON(EN)</sub>  | R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 12.5 pF,<br>see figure 5                                                                                                          | 9                    | 02             |        | 500  | ns   |
|                                                               | t <sub>OFF(EN)</sub> |                                                                                                                                                                           | 10,11                |                |        | 1000 |      |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

| Test                                                                              | Symbol                           | Conditions <u>1/</u><br>V- = -15 V, V+ = +15 V,<br>V <sub>EN</sub> = 2.4 V<br><br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br>unless otherwise specified | Group A<br>subgroups | Device<br>type | Limits |      | Unit |
|-----------------------------------------------------------------------------------|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------|--------|------|------|
|                                                                                   |                                  |                                                                                                                                                 |                      |                | Min    | Max  |      |
| Input leakage current <u>2/</u>                                                   | I <sub>IH</sub>                  | Measure inputs sequentially, connect all unused inputs to ground                                                                                | 1                    | 03             | -1.0   | 1.0  | μA   |
|                                                                                   |                                  |                                                                                                                                                 | 2                    |                |        | 10   |      |
|                                                                                   | I <sub>IL</sub>                  |                                                                                                                                                 | 1                    |                | -1.0   | 1.0  |      |
|                                                                                   |                                  |                                                                                                                                                 | 2                    |                |        | 10   |      |
| Leakage current into the source terminal of an “OFF” switch                       | I <sub>S(OFF)</sub>              | V <sub>S</sub> = +10 V, V <sub>EN</sub> = 0.8 V,<br>V <sub>D</sub> = -10 V, all unused inputs = -10 V                                           | 1,2,3                | 03             | -50    | +50  | nA   |
|                                                                                   |                                  | V <sub>S</sub> = -10 V, V <sub>EN</sub> = 0.8 V,<br>V <sub>D</sub> = +10 V, all unused inputs = +10 V                                           |                      |                |        |      |      |
| Leakage current into the drain terminal of an “OFF” switch                        | +I <sub>D(OFF)</sub>             | V <sub>D</sub> = +10 V, V <sub>EN</sub> = 0.8 V, all unused inputs = -10 V                                                                      | 1,2,3                | 03             | -250   | +250 | nA   |
|                                                                                   | -I <sub>D(OFF)</sub>             | V <sub>D</sub> = -10 V, V <sub>EN</sub> = 0.8 V, all unused inputs = +10 V                                                                      |                      |                |        |      |      |
| Leakage current from an “ON” driver into the switch (drain)                       | I <sub>D(ON)</sub>               | V <sub>D</sub> = +10 V, V <sub>S</sub> = +10 V, all unused inputs = -10 V                                                                       | 1,2,3                | 03             | -250   | +250 | nA   |
|                                                                                   |                                  | V <sub>D</sub> = -10 V, V <sub>S</sub> = -10 V, all unused inputs = +10 V                                                                       |                      |                |        |      |      |
| Overvoltage protected, leakage current into the drain terminal of an “OFF” switch | I <sub>D(OFF)</sub> over-voltage | V <sub>S</sub> = +25 V, V <sub>D</sub> = 0 V, V <sub>EN</sub> = 0.8 V                                                                           | 1,3                  | 03             | -2.0   | 2.0  | μA   |
|                                                                                   |                                  |                                                                                                                                                 | 2                    |                | -5.0   | 5.0  |      |
|                                                                                   |                                  | V <sub>S</sub> = -25 V, V <sub>D</sub> = 0 V, V <sub>EN</sub> = 0.8 V                                                                           | 1,3                  |                | -2.0   | 2.0  |      |
|                                                                                   |                                  |                                                                                                                                                 | 2                    |                | -5.0   | 5.0  |      |
| Positive supply current                                                           | I(+)                             | V <sub>A</sub> = 5.0 V                                                                                                                          | 1,2,3                | 03             |        | +2.0 | mA   |
| Negative supply current                                                           | I(-)                             | V <sub>A</sub> = 5.0 V                                                                                                                          | 1,2,3                | 03             |        | -1.4 | mA   |
| Standby positive supply current                                                   | +I <sub>SBY</sub>                | V <sub>A</sub> = 0 V, V <sub>EN</sub> = 0.8 V                                                                                                   | 1, 2, 3              | 03             |        | +2.0 | mA   |
| Standby negative supply current                                                   | -I <sub>SBY</sub>                | V <sub>A</sub> = 0 V, V <sub>EN</sub> = 0.8 V                                                                                                   | 1, 2, 3              | 03             |        | -1.0 | mA   |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – continued.

| Test                                                          | Symbol               | Conditions <u>1/</u><br>V- = -15 V, V+ = +15 V,<br>V <sub>EN</sub> = 2.4 V<br><br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br>unless otherwise specified | Group A<br>subgroups | Device<br>type | Limits |      | Unit |
|---------------------------------------------------------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------|--------|------|------|
|                                                               |                      |                                                                                                                                                 |                      |                | Min    | Max  |      |
| Switch "ON" resistance                                        | R <sub>DS1</sub>     | V <sub>S</sub> = +10 V, I <sub>D</sub> = +100 μA                                                                                                | 1,3                  | 03             |        | 1500 | Ω    |
|                                                               |                      |                                                                                                                                                 | 2                    |                |        | 1800 |      |
|                                                               |                      | V <sub>S</sub> = -10 V, I <sub>D</sub> = -100 μA                                                                                                | 1,3                  |                |        | 1500 | Ω    |
|                                                               |                      |                                                                                                                                                 | 2                    |                |        | 1800 |      |
| Switch "ON" resistance                                        | R <sub>DS2</sub>     | V+ = +10 V, V- = -10 V,<br>V <sub>S</sub> = +5 V, I <sub>D</sub> = +100 μA                                                                      | 1,2,3                | 03             |        | 2200 | Ω    |
|                                                               |                      | V+ = +10 V, V- = +10 V,<br>V <sub>S</sub> = -5 V, I <sub>D</sub> = -100 μA                                                                      |                      |                |        | 2200 |      |
| Capacitance: Address                                          | C <sub>A</sub>       | V+ = V- = 0 V, <u>3/</u><br>f = 1 MHz, T <sub>A</sub> = +25°C                                                                                   | 4                    | 03             |        | 10   | pF   |
| Capacitance: output<br>switch                                 | C <sub>OS</sub>      | V+ = V- = 0 V, <u>3/</u><br>f = 1 MHz, T <sub>A</sub> = +25°C                                                                                   | 4                    | 03             |        | 45   | pF   |
| Capacitance: input<br>switch                                  | C <sub>IS</sub>      | V+ = V- = 0 V, <u>3/</u><br>f = 1 MHz, T <sub>A</sub> = +25°C                                                                                   | 4                    | 03             |        | 10   | pF   |
| Charge transfer error                                         | V <sub>CTE</sub>     | V <sub>S</sub> = GND, <u>3/</u><br>V <sub>GEN</sub> = 0 V to 5 V,<br>T <sub>A</sub> = +25°C                                                     | 4                    | 03             |        | 10   | mV   |
| Single channel isolation                                      | V <sub>ISO</sub>     | V <sub>GEN</sub> = 1 V <sub>P-P</sub> , <u>3/</u><br>f = 200 kHz, T <sub>A</sub> = +25°C                                                        | 4                    | 03             | 50     |      | dB   |
| Crosstalk between<br>channels                                 | V <sub>CT</sub>      | V <sub>GEN</sub> = 1 V <sub>P-P</sub> , <u>3/</u><br>f = 200 kHz, T <sub>A</sub> = +25°C                                                        | 4                    | 03             | 50     |      | dB   |
| Break-before-make time<br>delay                               | t <sub>D</sub>       | T <sub>A</sub> = +25°C, see figure 3 <u>3/</u>                                                                                                  | 9                    | 03             | 5      |      | ns   |
| Propagation delay times:<br>Address inputs to<br>I/O channels | t <sub>ON(A)</sub>   | R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF, <u>3/</u><br>see figure 4                                                                      | 9                    | 03             |        | 1000 | ns   |
|                                                               | t <sub>OFF(A)</sub>  |                                                                                                                                                 | 10,11                |                |        | 1500 |      |
| Enable to I/O                                                 | t <sub>ON(EN)</sub>  | R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 100 pF, <u>3/</u><br>see figure 5                                                                       | 9                    | 03             |        | 1000 | ns   |
|                                                               | t <sub>OFF(EN)</sub> |                                                                                                                                                 | 10,11                |                |        | 1500 |      |

1/ Unless otherwise specified, V+ = +15 V and V- = -15 V.2/ Input current of one input node.3/ Guaranteed, if not tested, to the limits specified.

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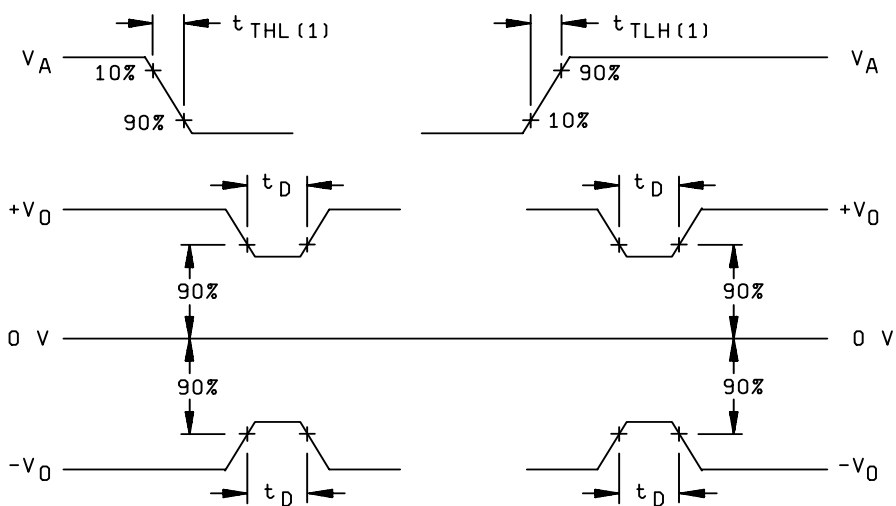
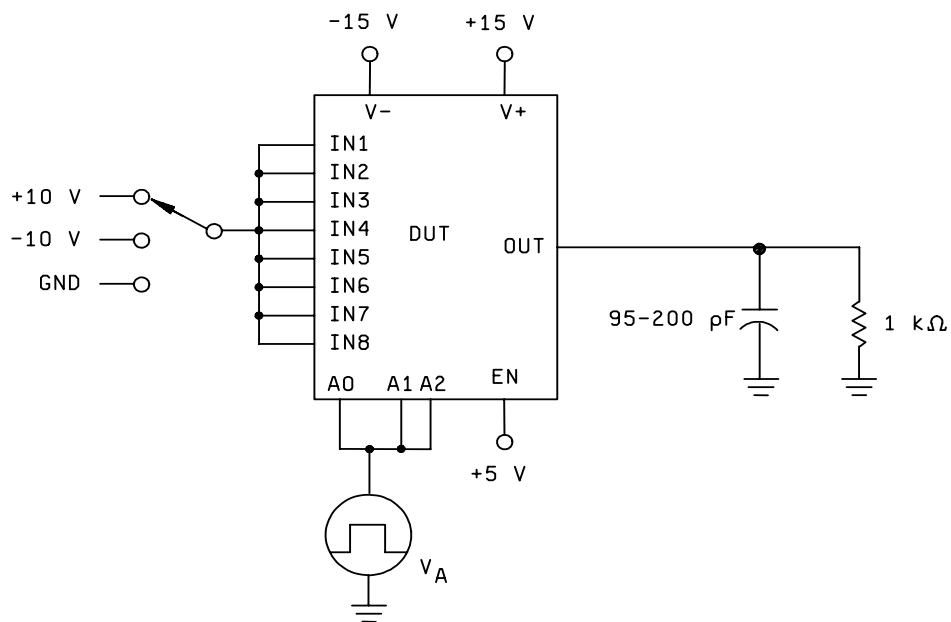
|                 |                 |         |          |
|-----------------|-----------------|---------|----------|
| Case outlines   | E               | F and X | 2        |
| Device types    | 01,02,03        | 01      | 01,02,03 |
| Terminal number | Terminal symbol |         |          |
| 1               | A0              | A0      | NC       |
| 2               | ENABLE          | ENABLE  | A0       |
| 3               | V-              | V-      | ENABLE   |
| 4               | IN 1            | IN 1    | V-       |
| 5               | IN 2            | IN 2    | IN 1     |
| 6               | IN 3            | IN 3    | NC       |
| 7               | IN 4            | IN 4    | IN 2     |
| 8               | OUT             | OUT     | IN 3     |
| 9               | IN 8            | IN 8    | IN 4     |
| 10              | IN 7            | IN 7    | OUT      |
| 11              | IN 6            | IN 6    | NC       |
| 12              | IN 5            | IN 5    | IN 8     |
| 13              | V+              | V+      | IN 7     |
| 14              | GND             | GND     | IN 6     |
| 15              | A2              | A2      | IN 5     |
| 16              | A1              | A1      | NC       |
| 17              | ---             | ---     | V+       |
| 18              | ---             | ---     | GND      |
| 19              | ---             | ---     | A2       |
| 20              | ---             | ---     | A1       |

FIGURE 1. Terminal connections.

| A2 | A1 | A0 | EN | Channel selected |
|----|----|----|----|------------------|
| X  | X  | X  | L  | None             |
| L  | L  | L  | H  | 1                |
| L  | L  | H  | H  | 2                |
| L  | H  | L  | H  | 3                |
| L  | H  | H  | H  | 4                |
| H  | L  | L  | H  | 5                |
| H  | L  | H  | H  | 6                |
| H  | H  | L  | H  | 7                |
| H  | H  | H  | H  | 8                |

FIGURE 2. Truth table.

|                                                                                                         |                  |                            |                    |
|---------------------------------------------------------------------------------------------------------|------------------|----------------------------|--------------------|
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|                                                                                                         |                  | REVISION LEVEL<br><b>L</b> | SHEET<br><b>11</b> |

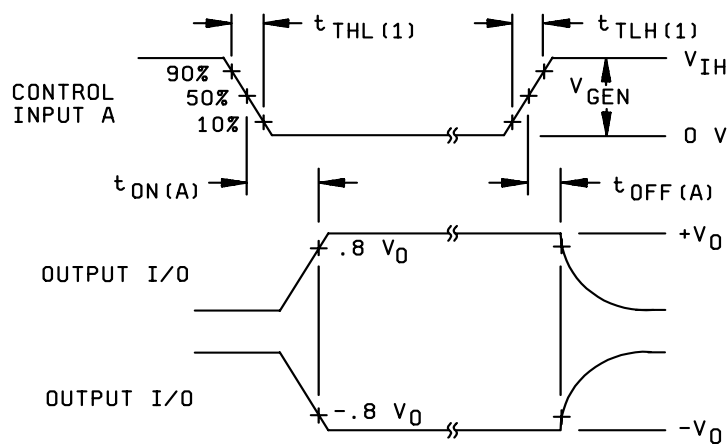
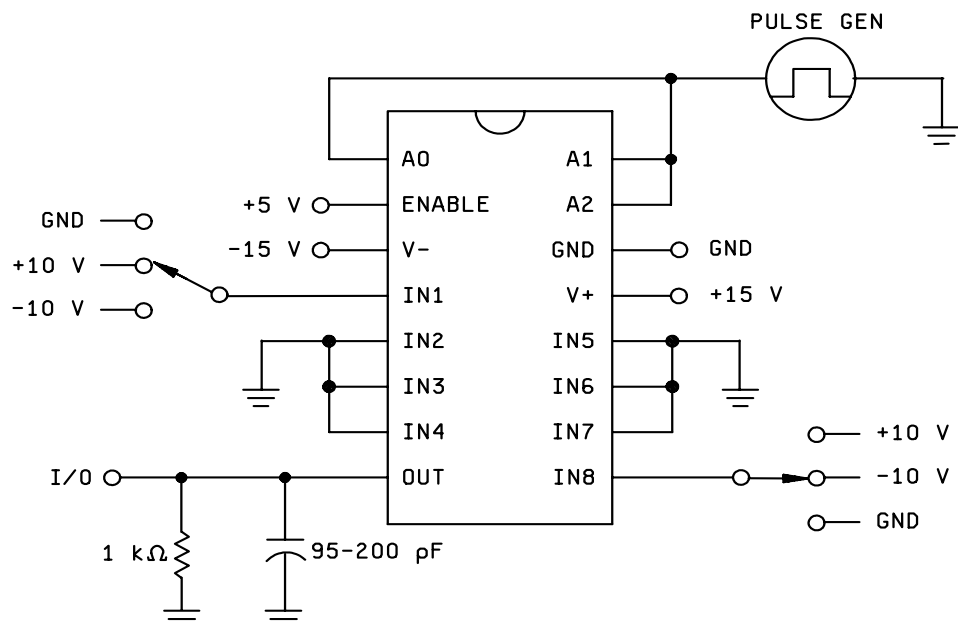


NOTE:

Input pulse requirements:  $V_{GEN} = 4\text{ V}$ ,  $t_{THL(1)} = t_{TLH(1)} \leq 20\text{ ns}$ .

FIGURE 3. Break before make test circuit and waveforms.

|                                                                                                               |                  |                            |                    |
|---------------------------------------------------------------------------------------------------------------|------------------|----------------------------|--------------------|
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|                                                                                                               |                  | REVISION LEVEL<br><b>L</b> | SHEET<br><b>12</b> |

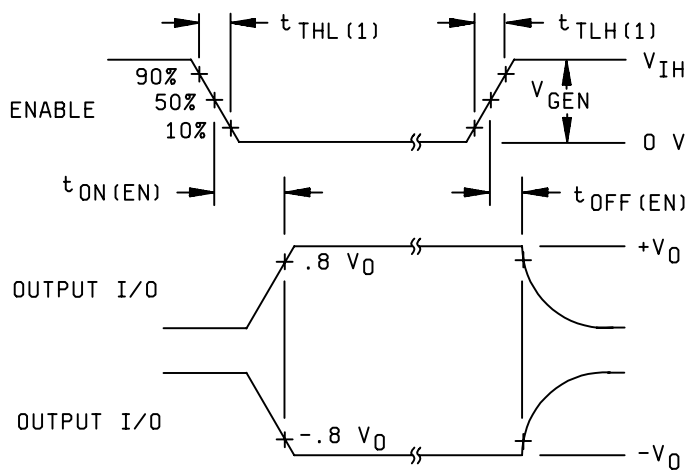
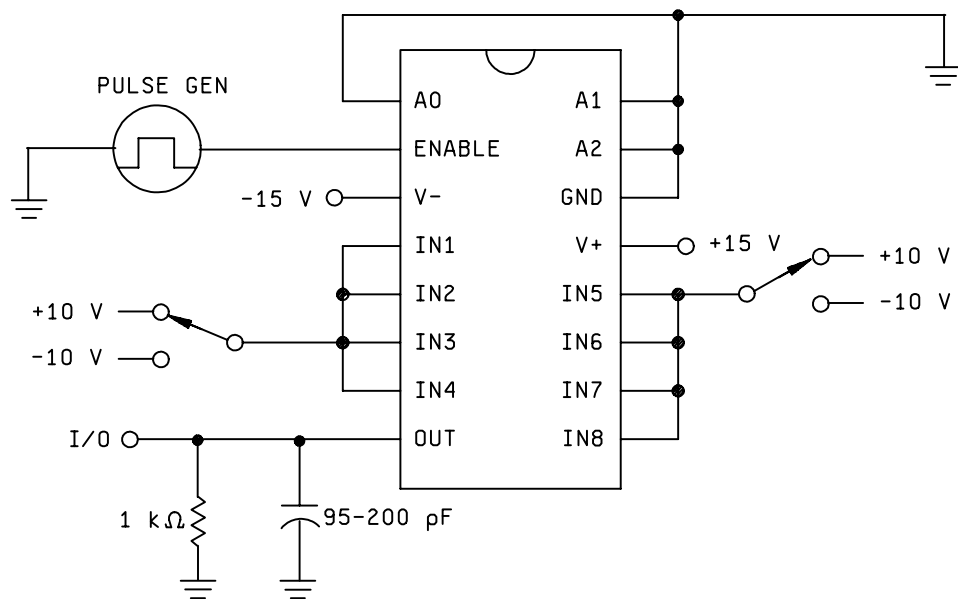


NOTE:

Input pulse requirements:  $V_{GEN} = 4\text{ V}$ ,  $t_{THL(1)} = t_{TLH(1)} \leq 20\text{ ns}$ .

FIGURE 4. Timing test circuit and waveforms. (Address inputs to I/O)

|                                                                                                               |                  |                            |                    |
|---------------------------------------------------------------------------------------------------------------|------------------|----------------------------|--------------------|
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|                                                                                                               |                  | REVISION LEVEL<br><b>L</b> | SHEET<br><b>13</b> |



NOTE:

Input pulse requirements:  $V_{GEN} = 4 \text{ V}$ ,  $t_{THL(1)} = t_{TLH(1)} \leq 20 \text{ ns}$ .

FIGURE 5. Timing test circuit and waveforms. (Enable to I/O)

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#### 4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2)  $T_A = +125^{\circ}\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

##### 4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (capacitance measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

##### 4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2)  $T_A = +125^{\circ}\text{C}$ , minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

|                                                                                                 |           |                     |             |
|-------------------------------------------------------------------------------------------------|-----------|---------------------|-------------|
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TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements                                      | Subgroups<br>(in accordance with<br>MIL-STD-883, method 5005,<br>table I) |
|--------------------------------------------------------------------|---------------------------------------------------------------------------|
| Interim electrical parameters<br>(method 5004)                     | 1                                                                         |
| Final electrical test parameters<br>(method 5004)                  | 1*,2,3,4,9                                                                |
| Group A test requirements<br>(method 5005)                         | 1,2,3,4,9,10**,11**                                                       |
| Groups C and D end-point<br>electrical parameters<br>(method 5005) | 1                                                                         |

\* PDA applies to subgroup 1.

\*\* Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

|                                                                                                         |                  |                            |                    |
|---------------------------------------------------------------------------------------------------------|------------------|----------------------------|--------------------|
| <b>STANDARD<br/>MICROCIRCUIT DRAWING</b><br>DEFENSE SUPPLY CENTER COLUMBUS<br>COLUMBUS, OHIO 43218-3990 | SIZE<br><b>A</b> |                            | <b>77052</b>       |
|                                                                                                         |                  | REVISION LEVEL<br><b>L</b> | SHEET<br><b>16</b> |

## STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-04-05

Approved sources of supply for SMD 77052 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

| Standard microcircuit drawing PIN <u>1/</u> | Vendor CAGE number | Vendor similar PIN <u>2/</u> | Reference military specification part number |
|---------------------------------------------|--------------------|------------------------------|----------------------------------------------|
| 77052012A                                   | 24355              | ADG508ATE/883B               |                                              |
|                                             | 34371              | HI4-508/883                  |                                              |
|                                             | <u>3/</u>          | DG508AAZ/883                 |                                              |
| 77052012C                                   | 1ES66              | DG508AAZ/883B                |                                              |
| 7705201EA                                   | 1ES66              | DG508AAK/883B                | M38510/19007BEA                              |
|                                             | 24355              | ADG508ATQ/883B               |                                              |
|                                             | <u>3/</u>          | HI1-508/883                  |                                              |
|                                             | <u>3/</u>          | DG508AAP/883                 |                                              |
| 7705201FA                                   | <u>3/</u>          | DG508AAL/883                 |                                              |
| 7705201XA                                   | <u>3/</u>          | DG508AAL/883                 |                                              |
| 7705201XC                                   | 1ES66              | DG508AAL/883B                |                                              |
| 77052022A                                   | 34371              | HI4-548/883                  |                                              |
| 7705202EA                                   | 34371              | HI1-548/883                  | M38510/19005BEA                              |
| 77052032C                                   | 1ES66              | MAX358MLP/883B               |                                              |
| 7705203EA                                   | 1ES66              | MAX358MJE/883B               | M38510/19005BEA                              |

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

STANDARD MICROCIRCUIT DRAWING BULLETIN – CONTINUED.

| <u>Vendor CAGE<br/>number</u> | <u>Vendor name<br/>and address</u>                                                                                                                         |
|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1ES66                         | Maxim Integrated Products<br>120 San Gabriel Dr.<br>Sunnyvale, CA 94086-5125                                                                               |
| 24533                         | Analog Devices<br>Rt 1 Industrial Park<br>PO Box 9106<br>Norwood, MA 02062<br>Point of contact: (35361)495999<br>Raheen Business Park<br>Limerick, Ireland |
| 34371                         | Intersil Corporation<br>2401 Palm Bay Blvd<br>PO Box 883<br>Melbourne, FL 32902-0883                                                                       |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.