EMB1428Q Switch Matrix Gate Driver

Check for Samples: EMB1428Q

FEATURES

- **60V Maximum Stack Operating Voltage**
- **Twelve (12) Floating Gate Drivers**
- **SPI Bus Interface (for Charge/discharge Commands and Fault Reporting)**
- **Low Power *Sleep* Mode**
- **EMB1428Q is an Automotive Grade Product that is AEC-Q100 Grade 1 Qualified (-40°C to +125°C Operating Junction Temperature)**

APPLICATIONS

- **Li-Ion Battery Management Systems**
- **Electrical/Hybrid Vehicles**
- **Grid-Power Storage**

DESCRIPTION

The EMB1428 Switch Matrix Gate Driver IC is designed to work in conjunction with EMB1499 DC/DC Controller IC to support TI's switch matrix based active cell balancing scheme in a battery management system. The EMB1428 provides 12 floating MOSFET gate drivers necessary for balancing up to 7 battery cells connected in a series stack. Multiple EMB1428 ICs may be used together to balance a stack of more than seven battery cells.

The EMB1428 integrated circuit interfaces with the EMB1499 DC/DC controller to control and enable charging and discharging modes. The EMB1428 uses an SPI bus to accept commands from the main controller (CPU/MCU) on which battery cell should be charged or discharged and to report back any faults to the main controller (CPU/MCU).

Typical Application

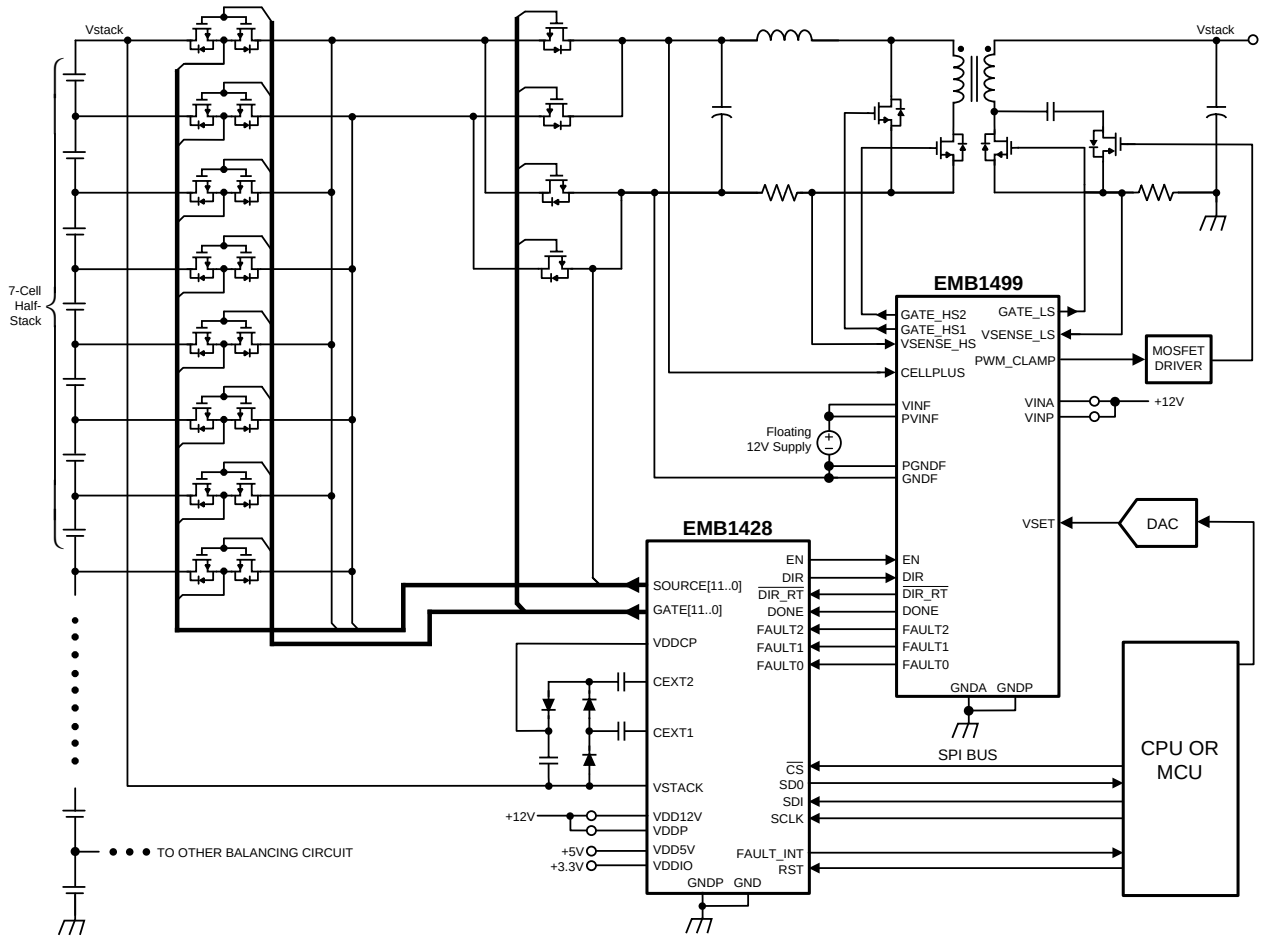
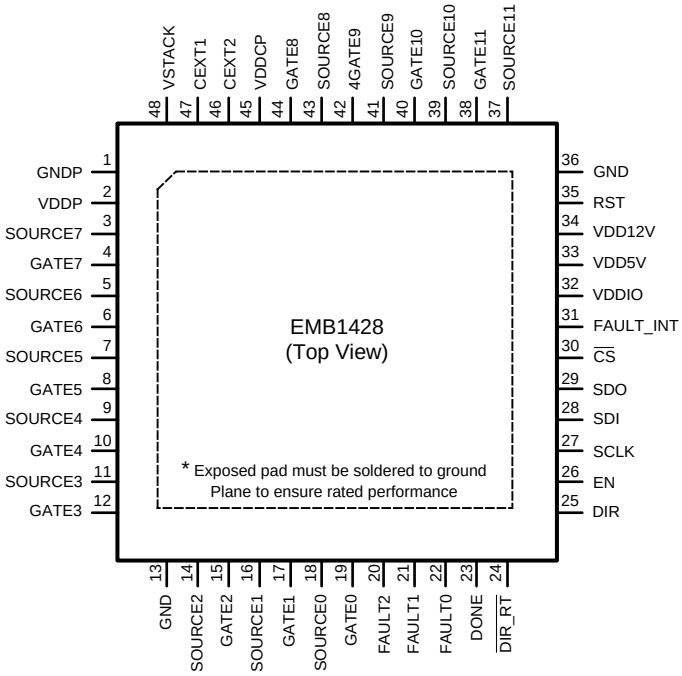


Figure 1. Typical Application

Connection Diagram



48-Pin WQFN
See RHS Package

Table 1. ORDERING INFORMATION

Order number	Package Type	Package Drawing	Supplied As	Features
EMB1428QSQ	WQFN	RHS	1000 Units in Tape and Reel	AECQ100 Grade qualified. Automotive EMB1428QSQE 250 Units in Tape and Reel Grade Production Flow(1)
EMB1428QSQE			250 Units in Tape and Reel	
EMB1428QSQX			2500 Units in Tape and Reel	

(1) Automotive Grade (Q) product incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC-Q100 standard. Automotive grade products are identified with the letter Q. For more information go to http://www.ti.com/automotive.

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	GNDP	Ground for charge pump circuitry	Connect to stack ground at board level.
2	VDDP	12V supply for charge pump circuitry	Connect to 12V supply at board level with 0.1µF bypass cap to GNDP.
3, 5, 7, 9, 11, 14, 16, 18, 37, 39, 41, 43	SOURCE0 to SOURCE11	Floating driver references	Connect to FET switch sources.
4, 6, 8, 10, 12, 15, 17, 19, 38, 40, 42, 44	GATE0 to GATE11	Floating driver outputs	Connect to FET switch gates.
13, 36	GND	Ground	Internal reference for all analog and digital circuitry except the charge pump.
20, 21, 22	FAULT[2, 1, 0]	Inputs, three-bit digital fault code from EMB1499	Fault code is reported to CPU through the SPI bus. 5V Schmitt-trigger inputs, 12V signal tolerant.
23	DONE	Input from EMB1499, indicates end of charge cycle	5V Schmitt-trigger input, 12V signal tolerant.

PIN DESCRIPTIONS (continued)

Pin	Name	Description	Application Information
24	$\overline{\text{DIR\_RT}}$	Input from EMB1499, handshake signal, inverted version of DIR	5V Schmitt-trigger input, 12V signal tolerant.
25	DIR	Output to EMB1499, indicates direction of charging current	'High' indicates charge mode, 'Low' indicates discharge mode. 5V CMOS output levels.
26	EN	Output to EMB1499, enable signal for charge/discharge cycle	'High' signals EMB1499 to begin charge or discharge cycle, 'Low' signals EMB1499 to ramp down current and finish present cycle. 5V CMOS levels.
27	SCLK	SPI clock input	1MHz SPI interface, I/O levels are referenced to the VDDIO supply.
28	SDI	SPI data input	
29	SDO	SPI data output	
30	$\overline{\text{CS}}$	SPI chip select input	
31	FAULT_INT	Fault interrupt output to CPU	Referenced to the VDDIO supply.
32	VDDIO	IO supply for SPI interface circuitry	Connect to CPU supply to match I/O levels.
33	VDD5V	5V supply for digital core and EMB1499 interface circuitry	
34	VDD12V	12V supply for analog core circuitry	
35	RST	RESET pin	
45	VDDCP	Floating supply input from external charge pump circuit	Connected to external charge pump circuit that provides a floating supply referenced to the top of the battery module (VSTACK).
46, 47	CEXT1, CEXT2	Charge pump driver outputs	Buffered, differential 1MHz clock signals for driving external charge pump circuit.
48	VSTACK	Supply from the highest voltage in the battery module	

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

Any SOURCE pin to GND	-0.5V to 70V
VSTACK to GND	-0.5V to 70V
VDDCP to VSTACK	-0.5V to 25V
VDDCP to GND	-0.5V to 90V
VDD12V to GND	-0.5V to 16V
VDDP to GNDP	-0.5V to 16V
GNDP to GND	-0.5V to 0.5V
FAULTx, DONE, $\overline{\text{DIR\_RT}}$ to GND	-0.5V to 16V
VDD5V, VDDIO to GND	-0.5V to 7.5V
All other inputs to GND	-0.5V to 7.5V
ESD Rating(2)	±2 kV
Soldering Information	
Junction Temperature	150°C
Storage Temperature	-65°C to 150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the recommended Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and should not be operated beyond such conditions.
(2) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD22–A114.

OPERATING RATINGS

VSTACK to GND	15V to 60V
VDD12V to GND	10.8V to 13.2V
VDDP to GNDP	10.8V to 13.2V
VDD5V, to GND	4.5V to 5.5V
VDDIO to GND	2.5V to 5.5V
VDDCP to VSTACK	18V to 24V
Junction Temperature (T_J)	-40°C to 125°C

ELECTRICAL CHARACTERISTICS

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of −40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°, and are provided for reference purposes only. VSTACK = 60V, SOURCEX = 0V, VDD12V = VDDP = 12V, VDD5V = 5V, VDDIO = 3.3V unless otherwise indicated in the conditions column.

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
System Parameters						
I_{STACK}	Stack supply current	System connected to Cell 1,		1.57	**2.4**	mA
I_{VDDP}	Charge pump driver supply current	EN high		4	**6**	mA
I_{VDD12V}	12V supply current	VSTACK = 60V		100	**125**	µA
I_{VDD5V}	5V supply current	SOURCEx = 60V		135	**180**	µA
I_{VDDIO}	IO supply current			0.2	**1.8**	µA
I_{STACK_SD}	Stack supply current, shutdown	Shutdown (FETs disconnected)		1.4	**2.3**	µA
I_{VDDP_SD}	Charge pump driver supply current, shutdown	VSTACK = 60V			**0.4**	µA
I_{VDD12V_SD}	12V supply current, shutdown	SOURCEx = 60V			**0.2**	µA
I_{VDD5V_SD}	5V supply current, shutdown			8.7	**11**	µA
I_{VDDIO_SD}	IO supply current, shutdown				**0.1**	µA
I_{STACK_RST}	Stack supply current, reset	RESET		0.28	**2.3**	µA
I_{VDDP_RST}	Charge pump driver supply current, reset	VSTACK = 60V			**0.8**	µA
I_{VDD12V_RST}	12V supply current, reset	SOURCEx = 60V			**1.2**	µA
I_{VDD5V_RST}	5V supply current, reset			20	**28**	µA
I_{VDDIO_RST}	IO supply current, reset				**0.5**	µA
FET Driver Parameters						
t_{EN}	Driver setup time, Cell-to-Cell	Rising edge of DONE to rising edge of EN			**2.4**	ms
	Driver set up time from shutdown	Rising edge of $\overline{CS}$ to rising edge of EN		1.23	**2.4**	ms
t_{PD}	Shutdown time	Rising edge of DONE to last clock pulse on CEXT2		330	**500**	µs
V_{GSON}	Driver output 'on' voltage, V_{GATE}-V_{SOURCE}		**10.8**	12.1	**14**	V
ΔV_{GSON}	VSTACK Line Regulation	SOURCEx = 0V, VSTACK = 15V to 60V		3.5	**9**	mV/V
	VSOURCE Line Regulation	SOURCEx = 0V to 60V, VSTACK = 60V		5.5	**20**	mV/V
I_{GON}	GATE pin output drive current during FET turn-on transient	(GATE-SOURCE) = V_{GSON}/2	**100**	225		µA
$R_{GSTRANS}$	Driver output pull-down resistance during FET turn-off transient, GATE to SOURCE pin	(GATE-SOURCE) = V_{GSON}/2		16.2	**17.5**	Ω
R_{GSON}	Driver output pull-down resistance active		**100**	150	**220**	Ω
R_{GSOFF}	Driver output pull-down resistance after FET turn-off transient has finished, GATE to SOURCE pin	(GATE-SOURCE) ≤ 0.2V	**100**	150	**220**	Ω
I_{SRC}	SOURCE pin bias current, power-up, driver output on			210		µA
	SOURCE pin bias current, power-up, driver output off			80		µA
I_{SRC_SD}	SOURCE pin bias current, power-down	Shutdown		100		nA

(1) Typical specifications represent the most likely parametric norm at 25°C operation.

ELECTRICAL CHARACTERISTICS (continued)

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Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
Charge Pump Parameters						
V_{CPO}	Charge pump output measured with respect to VSTACK	VDDP = 12V, System connected to Cell 1, EN high		23.5		V
R_{OUT_CP}	Charge pump output resistance			1.7		Ω
V_{CP_UVH}	Charge pump UVLO upper trip voltage, VDDCP - VSTACK			16		V
V_{CP_UVL}	Charge pump UVLO lower trip voltage, VDDCP - VSTACK			14		V
f_{CLK}	$C_{EXT1,2}$ pin clock frequency		**0.9**	1.0	**1.15**	MHz
SPI/Microcontroller Interface Input Parameters ($\overline{CS}$, SDI, SCLK, RST)						
V_{IH}	$\overline{CS}$, SDI, SCLK Logic high threshold			2.25	**2.35**	V
V_{IL}	$\overline{CS}$, SDI, SCLK Logic low threshold		**0.95**	1.0		V
V_{IH-5V}	$\overline{CS}$, SDI, SCLK Logic high threshold	VDDIO = 5.0V		3.47	**3.6**	V
V_{IL-5V}	$\overline{CS}$, SDI, SCLK Logic low threshold		**1.45**	1.55		V
I_{IN}	SDI, SCLK Input bias current	V_{SDI}, V_{SCLK} = VDDIO = 5.0V			0.01 **0.1**	µA
R_{PUCS}	Internal Pull-up resistance from $\overline{CS}$ to VDDIO			98		kΩ
V_{IH_RST}	Reset Logic high threshold			1.0	**1.35**	V
V_{IL_RST}	Reset Logic low threshold		**0.55**	0.95		V
R_{PDRST}	Internal Pull-down resistance from RST to GND			98		kΩ
SPI/Microcontroller Interface Output Parameters (FAULT_INT, SDO)						
V_{OH}	Output High Voltage	I_{SOURCE} = 200µA	**3.15**	3.19		V
		I_{SOURCE} = 1mA		2.7		V
V_{OL}	Output Low Voltage	I_{SINK} = 200µA		0.12	**0.155**	V
		I_{SINK} = 1mA		0.6		V
I_{OZH}	SDO TRI-STATE Leakage current (high)	V_{SDO} = 0V or VDDIO			**3**	µA
I_{OZL}	SDO TRI-STATE Leakage current (low)	V_{SDO} = 0V or VDDIO			**0.2**	µA
SPI/Microcontroller Interface Timing Specifications (Need SPI mode)						
f_{SCLK}	Serial clock from CPU			1.0	**1.1**	MHz
DC	SCLK Duty Cycle		10	50	75	%
t_{CSU}	$\overline{CS}$ falling edge to SCLK rising edge		**100**			ns
t_{CDSU}	$\overline{CS}$ rising edge to SCLK rising edge		**50**			ns
t_{TRANS}	$\overline{CS}$ high pulse width		**1.5**			µs
t_{SU}	SDI setup to SCLK rising edge		**50**			ns
	SDO setup from SCLK rising edge		**200**			ns

ELECTRICAL CHARACTERISTICS (continued)

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Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
t_{HD}	$\overline{CS}$and SDI hold time from SCLK rising edge		**200**			ns
	SDO hold time from SCLK rising edge		**250**			ns
t_{CS}	$\overline{CS}$ falling edge to SDO enabled				**50**	ns
t_{DIS}	$\overline{CS}$ rising edge to SDO disabled (tri-state)				**60**	ns
EMB1499 Interface Input Parameters (FAULT0, FAULT1, FAULT2, $\overline{DIR\_RT}$, DONE)						
$V_{IH-EMB1499}$	Logic high threshold			3.4	**3.6**	V
$V_{IL-EMB1499}$	Logic low threshold		**1.4**	1.6		V
$I_{IN-EMB1499}$	Input bias current	V(FAULT$_X$, $\overline{DIR\_RT}$, DONE) = 12V			0.6 **1**	µA
EMB1499 Interface Output Parameters (EN, DIR)						
$V_{OH-EMB1499}$	Output High Voltage	I_{SOURCE} = 200µA	**4.86**	4.9		V
		I_{SOURCE} = 1mA		4.4		V
$V_{OL-EMB1499}$	Output Low Voltage	I_{SINK} = 200µA		0.11	**0.3**	V
		I_{SINK} = 1mA		0.56		V
EMB1499 Interface Timing Specifications						
t_{DIR}	DIR transition to corresponding $\overline{DIR\_RT}$				**700**	ns
t_{DIRSU}	DIR setup to EN rising edge		**3.4**			µs
t_{INT}	Any fault condition to FAULT_INT rising edge			2		µs
t_{DNL}	DONE low pulse width	Prior to EMB1499 fault condition	**3**			µs
t_{FSU}	FAULT[2, 1, 0] setup to DONE rising edge	EMB1499 reporting a fault condition	**1**			µs
t_{FHD}	FAULT[2, 1, 0] hold time from DONE rising edge		**8**			µs

BLOCK DIAGRAM

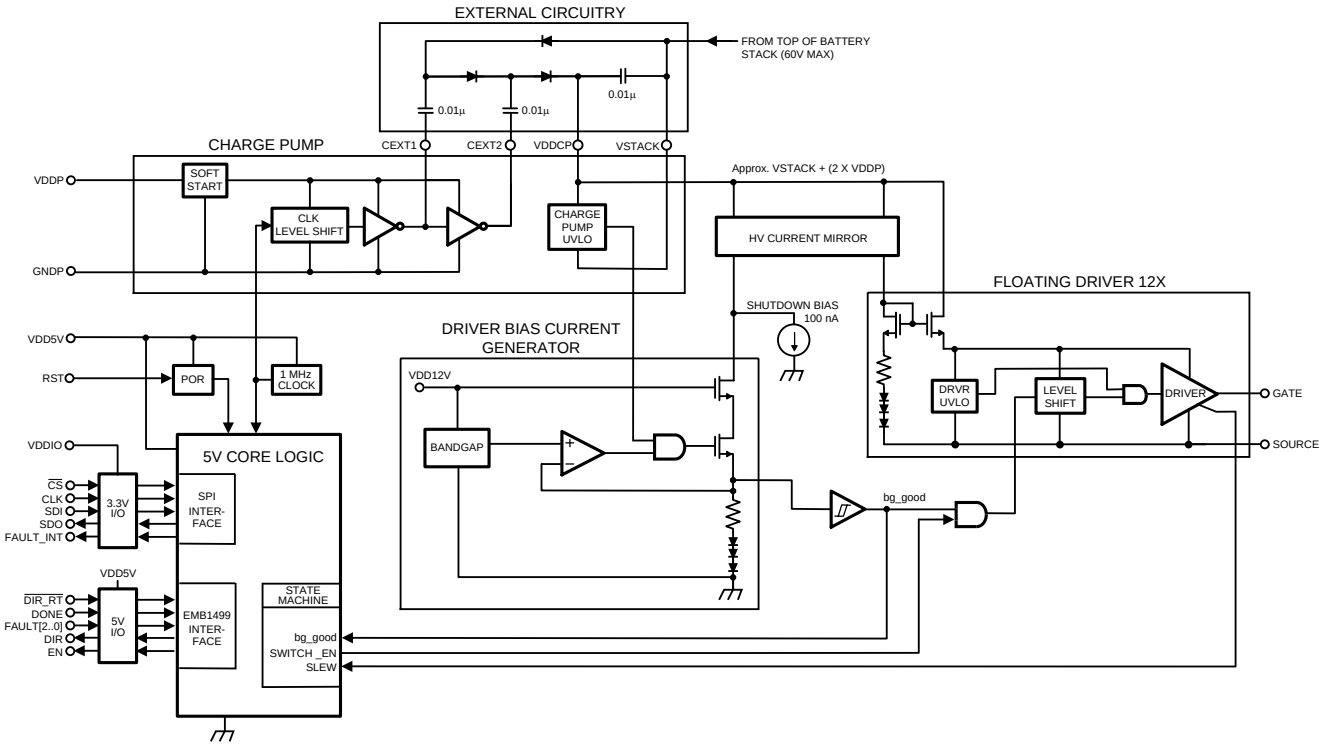

Figure 2. EMB1428 High -Level Block Diagram

APPLICATION INFORMATION

The EMB1428 and the EMB1499 work in conjunction to control an active balancing circuit for up to 7 battery cells connected in series. See Typical Application for the typical system architecture. The EMB1428 provides 12 floating gate drivers that are needed for the control of the FET switch matrix in the circuit. The EMB1499 is a DC/DC controller that regulates the inductor current in the bi-directional forward converter. In a typical application, the forward converter has the inductor side connected to the switch matrix and the other side to the battery stack. With such an arrangement, every cell balancing action is an energy exchange between a cell and the whole stack. The maximum number of cells in such a stack is constrained by the maximum stack voltage the EMB1428 can handle (60V). Theoretically the 7 cells associated with an EMB1428 can be anywhere along the stack. So in the case of a 14-cell stack, one EMB1428 can be used to handle the lower 7 cells (lower half-stack), and another EMB1428 can be used to handle the upper 7 cells (upper half-stack).

When the EMB1428 receives a cell balance command from the micro controller to charge or discharge a particular cell, it will first turn off all switches irrelevant to the balancing of that cell and then turn on the switches that will properly connect the cell to the forward converter. Once the proper switches in the switch matrix have been turned on, the EMB1428 will signal the EMB1499 to start charging or discharging the cell. The EMB1499 will then ramp the forward converter's inductor current (positive or negative) to a user-defined magnitude and keep a current constant. The inductor current is the balancing current the cell receives. Upon receiving a command from the microcontroller to stop balancing or to switch balancing action to a different cell, the EMB1428 will inform the EMB1499 to bring the balancing current towards zero. Once the inductor current has ramped down to zero, the EMB1428 will turn off all the switches that are not needed by the new command and turn on the switches that are needed (if any). If the new command is to balance a different cell, the EMB1428 will then signal the EMB1499 to ramp the inductor current again. If the new command is to stop balancing, the EMB1428 will enter a low power sleep mode, also known as shutdown mode.

The Switch Matrix

The FET switches in a switch matrix fall into two categories. See Figure 3 for a detailed illustration. The switches directly connected to the battery cells are called the "cell switches". Each cell switch is comprised of two N-FETs that are connected in a common source and common gate manner and is capable of blocking current flow in both directions. The switches directly connected to the DC/DC converter are called the "polarity switches". Each polarity switch is simply an N-FET and is capable of blocking current flow in one direction only.

Of the 7 cells handled by the EMB1428, assume the bottom cell is Cell 1, the one above it is Cell 2, and so on. Cell 1 is connected to two cell switches, i.e. Cell Switch 0 and Cell Switch 1 (CSW0 and CSW1). Cell 2 is connected to CSW1 and CSW2. This pattern repeats through all cell connections. Each cell switch has one drain node connected to either the EVEN rail (if the switch is even numbered) or the ODD rail (if the switch is odd numbered). Each of the four polarity switches (PSW0 through PSW3) either has a drain connected to the positive end of the DC/DC converter and a source connected to the EVEN or ODD rail, or has a source connected to the negative end of the DC/DC converter and a drain to the EVEN or ODD rail. The function of the cell switches is to select the chosen cell on the EVEN and ODD rails and the function of the polarity switches is to connect the cell to the DC/DC converter in a positive-to-positive and negative-to-negative manner.

Each time the EMB1428 tries to charge or discharge a certain cell, it will first turn off all irrelevant switches, and turn on or keep on relevant cell switches. It will then connect the cell to the EVEN and ODD rails and turn on the appropriate polarity switches.

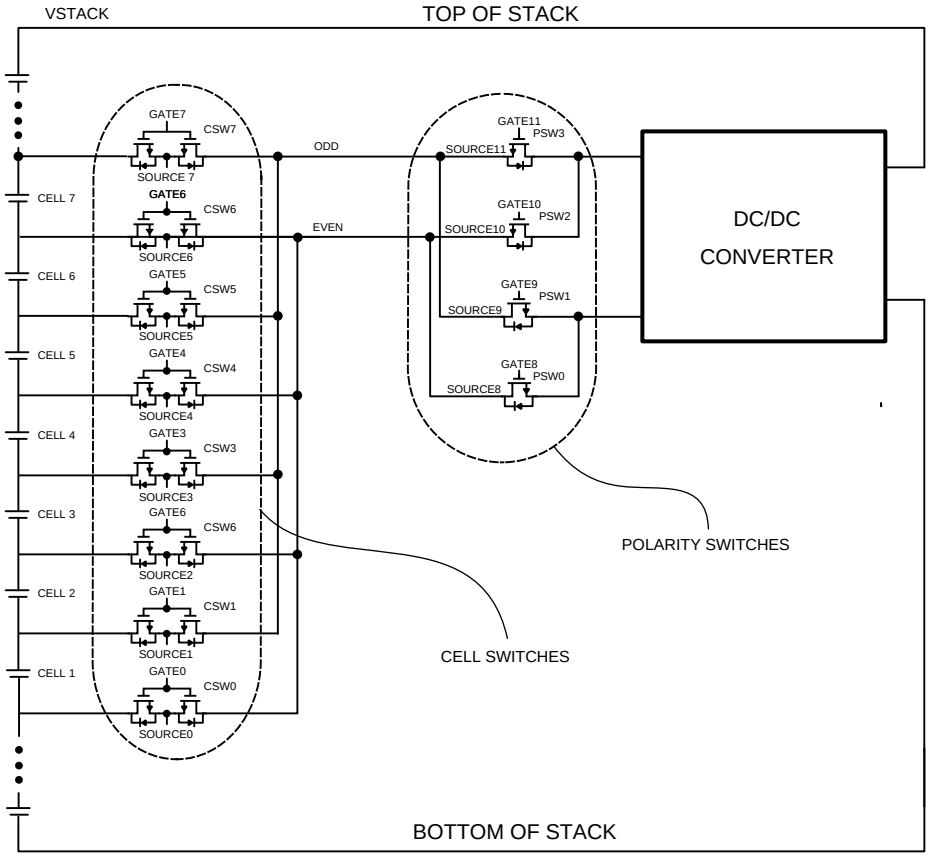

Figure 3. Switch Matrix

Reference Current Generator

A block diagram of the reference current generator is shown in Figure 4. This block generates bias currents that are used in the 12 floating drivers to create temperature-stable driver output voltages. The main blocks in the reference current generator are bandgap, opamp, resistor/diode stack, and shutdown bias generator.

The 5V bandgap voltage is forced across a stack of resistors and diodes in the operational amplifier feedback loop to generate a reference current. The reference current is mirrored from the VDDCP rail to each of the 12 floating drivers.

During sleep mode the bandgap output is held at 0V such that the reference current output is zero. A SOURCE shutdown bias current, I_{SRC}, is already created by a parallel bias generator that is active any time VSTACK is greater than 2V typical. The SOURCE shutdown bias current ensures that the driver outputs will be clamped off during shutdown if there is any significant voltage applied to VSTACK.

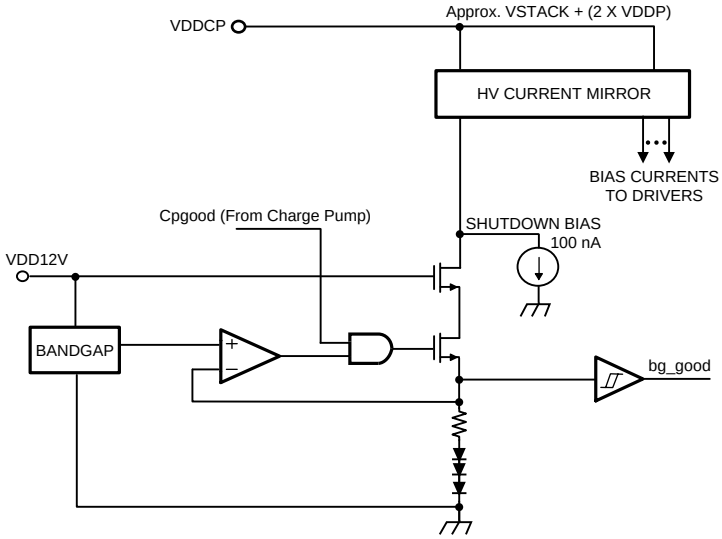

Figure 4. Reference Current Generator

The reference generator also monitors the cpgood signal which comes from the charge pump UVLO. If cpgood is low then the reference generator is held in a standby mode with zero output current until the charge pump has started. This delay prevents supply headroom issues that can occur if the drivers are turned on before the charge pump has created a large enough voltage at the VDDCP pin.

The bg_good signal is generated by a Schmitt trigger inverter that is driven by the operational amplifier feedback loop. This signal indicates that the bandgap has started up, the charge pump is operational, and the reference current is flowing to the drivers. The digital block monitors the bg_good signal and generates a fault if it is low when an SPI command is received.

Floating Gate Driver

Figure 5 shows the main blocks in the floating gate driver cell along with a dual-FET load and the built-in bleeder resistor. Each of the 12 drivers has a floating supply generator, shutdown circuit, UVLO, level-shift, and output buffer. The SOURCE pin can be up to 60V above ground for a 14 cell pack (14X4.3V) and the GATE pin must be able to swing 12V above the SOURCE pin (in some cases above the top of the battery stack) to turn on the external FETs.

The internal 100k bleeder resistors ensure that the FET switches will automatically turn off in the event of a catastrophic driver failure and that the FET switches are in an off state upon system power-up. The driver is designed to drive the FET switch directly with no gate-source resistor.

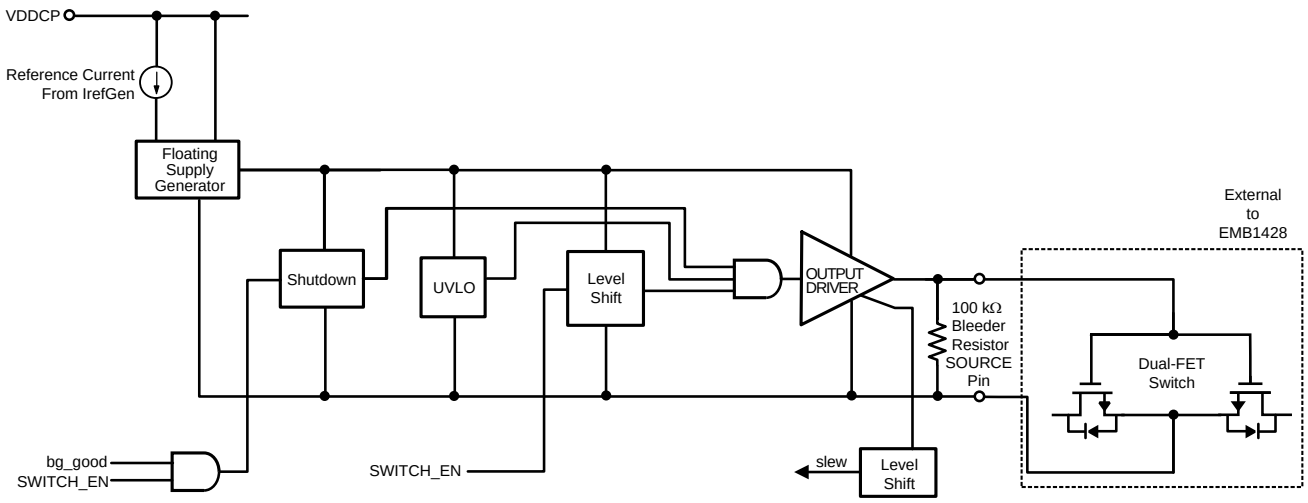

Figure 5. Floating Gate Driver

Each driver receives a reference current from the VDDCP rail that must flow out of the SOURCE pin and into the FET network along with the rest of the driver's bias current. The total SOURCE pin current for each driver with an off output is I_{SRC}. For drivers with outputs that are 'on', I_{GON} flows through the bleeder resistor and out of the source connection. For drivers 0 through 7 this current can flow into the battery stack or into the EVEN or ODD rail depending on which of the two FET body diodes is forward biased. This current helps ensure that the source connection of the dual-FET switches does not get pulled down such that a drain-source breakdown occurs. For drivers 8 through 11 this current usually flows into the EVEN or ODD rails, through an 'ON' dual-FET switch, and back into the battery stack.

Driver Shutdown Circuit

The driver shutdown block is essentially a simple level-shift circuit that monitors the system level shutdown signal (SWITCH_EN) and the bg_good signal. If shutdown is high and/or bg_good is low then the driver output is forced low and the driver enters a low power shutdown state. The bg_good signal indicates that the charge pump and bandgap are powered up and functional. This circuit also indirectly ensures that the drivers will automatically shut down if either the 5V or 12V supplies are not operational.

Floating Driver UVLO

A UVLO circuit is included in each driver to prevent the driver output from turning on unless its floating supply is active.

Floating Driver Output Buffer

Figure 6 shows the architecture for the floating driver output buffer along with a dual-FET load. The output buffer uses a two-stage parallel architecture to help control output currents that must be supplied by the charge pump. A low-output-drive slewing stage begins every output transition and a parallel high-output-drive latching stage is activated once the output has slewed to within 300mV(typical) of whichever rail it is approaching. The latching stage also provides a low output impedance to hold the output on or off in the presence of external noise transients. This architecture is used because all current provided by the output buffer to charge the external FET switch gate-source capacitance (i.e. turn a switch 'ON') must be supplied to the VDDCP pin by the charge pump. Turning a switch off is much simpler: all charge drained from the external FET gate-source capacitance flows into the GATE pin, through the driver pull-down circuitry, and back out through the SOURCE pin.

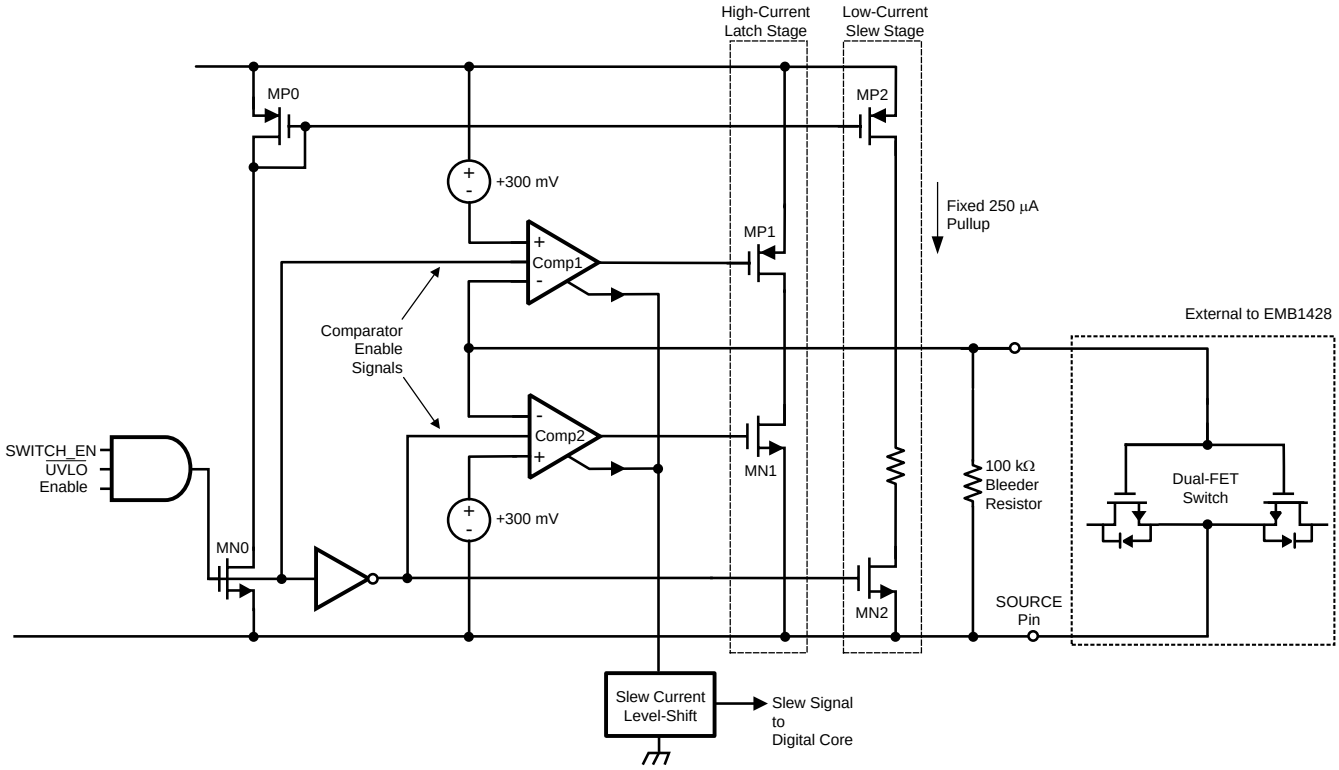

Figure 6. Floating Driver Output Buffer

The slewing output stage consists of a pull-up current source (MN0, MP0, and MP2) and a resistive pull-down circuit (MN2, and 20K resistor). The pull-up slewing current is I_{GON}. The approximate pull-up time can be estimated using the model shown in Figure 7 where the input is a current step waveform. R_{BLD} is the 100k bleeder resistance, typical. Vo is the voltage to which the slewing stage pulls the gate voltage up to (12V-0.3V = 11.7V). The equation for the slewing time is:

$$t_{SLEW} = C_{gs} \times R_{BLD} \times \ln\left(\frac{I_{GON} \times R_{BLD}}{I_{GON} \times R_{BLD} - V_o}\right) \quad (1)$$

Using the above equation along with a conservative estimate for the Cgs of the dual-FETs of 5nF gives pull-up times of 316 µs (R_{BLD} = 100k; V_o = 11.7V).

The pull-down behavior of the slewing output stage is determined by the RC circuit formed by the 20K resistor, the 100k bleeder resistor, and the Cgs of the external FETs. Using an analysis very similar to the above equation, the pull-down time can be estimated at approximately 307 µs.

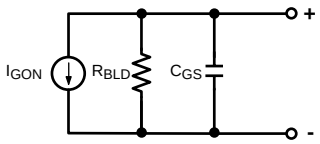

Figure 7. Driver Output Slewing Model

The latching output stage shown in Figure 6 consists of comparators Comp1 and Comp2 along with output devices MP1 and MN1. Half of this stage is de-activated each time the output begins a transition so that it does not conflict with the slewing stage. Comp1 and Comp2 receive an enable signal that switches them between normal comparator operation and a low-power mode where their outputs are forced high (Comp1) or low (Comp2) to unlatch. These comparators have a current output that is activated whenever the comparator is in comparator mode but un-latched (i.e. the output is still slewing). These currents are wire-ORed and processed by a level-shift circuit to produce a 5V logic slew signal. This slew signal is used by the digital core to control the timing of the switch enable signals.

Charge Pump

The EMB1428 uses a two-stage charge pump architecture that is shown in Figure 8. The main components of the charge pump are a soft start generator, clock level shift, output drivers, and a UVLO. This type of charge pump produces a floating supply voltage, VCPP that is typically (2 x VDDP) - (3 x Vdiode) with no load. The typical values for C1-C3 are expected to be 0.01 µF.

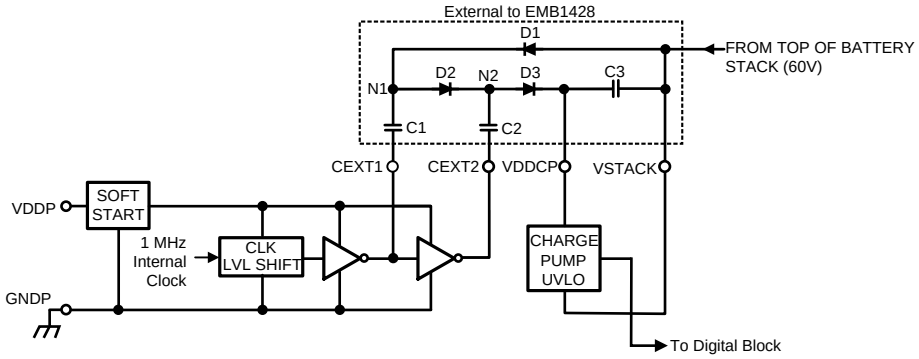

Figure 8. Charge Pump

In steady-state, the signals at the CEXT1 and CEXT2 pins are square wave voltages that are 180° out of phase, with an amplitude equal to the supply voltage VDDP. When CEXT1 is pulled low, C1 is charged through D1 to VSTACK minus the diode drop. With no loading at the output of the charge pump, the capacitor C1 acts like a simple electro-static level shift such that the CEXT1 square wave is reproduced at node N1 but switching between VSTACK and VSTACK+VDDP. During the opposite clock phase, the phase difference between the CEXT1 and CEXT2 pins allows charge to flow from C1 to C2 through D2 such that C2 is charged to VSTACK+VDDP when N1 is high and N2 is low. The next phase of the clock causes N2 to be pushed up to VSTACK + (2 x VDDP) through C2 which reverse biases D2 and forward biases D3. The D3/C3 circuit simply rectifies this square wave and creates a DC voltage of approximately 2 x VDDP across C3. The voltage developed across C3 is used as a floating supply for the VDDCP pin that is referenced to VSTACK. The VDDP supply current is always 2 times the load current pulled from the output of the charge pump.

Charge Pump UVLO

A floating UVLO circuit is connected between the VDDCP and VSTACK pins to monitor the charge pump output. The output of the UVLO has also been modified to produce the ground-referenced 5V cpgood signal through a level-shift circuit. The UVLO trip points are listed in the ELECTRICAL CHARACTERISTICS table as V_{CP_UVH} and V_{CP_UVL}.

Serial Interface

The serial interface operates on 8-bit transactions. See Figure 9 for proper operation of the serial interface. The microcontroller must send a 4-bit command on SDI followed by 4 zeros. The EMB1428 will provide fault[3:0] on SDO (related to the previous command), followed by the 4-bit command that it just received. The EMB1428 will drive SDO on the falling edge of SCLK and sample SDI on the rising edge of SCLK. The assertion of $\overline{CS}$ will cause an internal signal sdo_en to go high and actively drive the SDO pin high or low. A short delay after $\overline{CS}$ has been de-asserted, sdo_en will go low and the SDO pin will tri-state and be ready to be driven by other devices on the SPI bus.

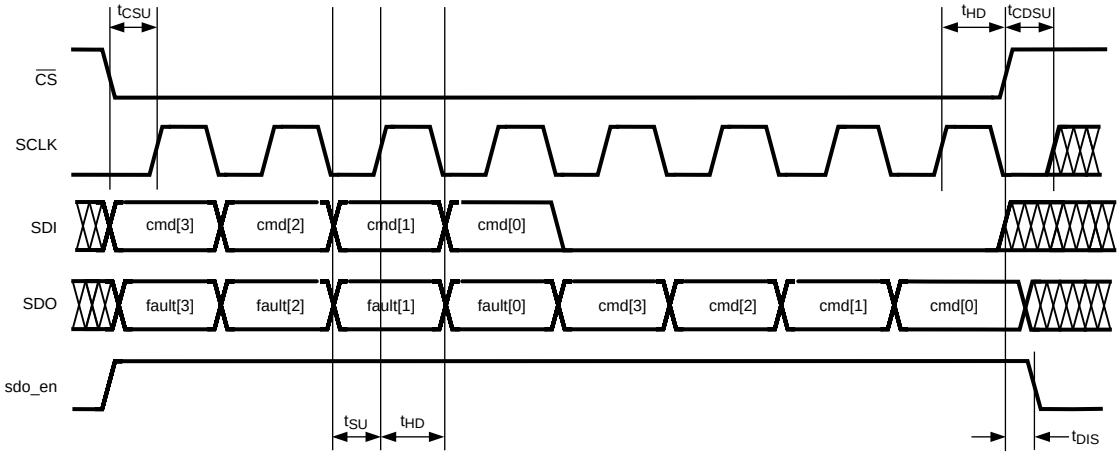

Figure 9. Serial Interface (proper operation)

If $\overline{CS}$ goes high at any point before the 8th rising edge of SDI, the transaction will be considered aborted and the data that was received on SDI will be discarded. No command change will occur from such a transaction. However, if FAULT_INT was cleared by the transaction it will remain cleared and the fault data will no longer be accessible.

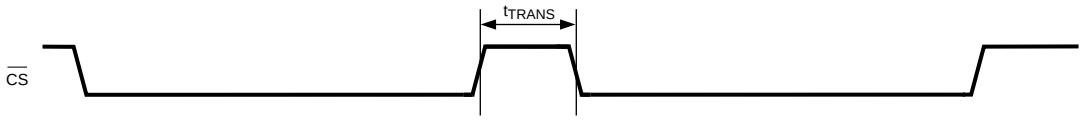

Figure 10. Serial Interface (inter transaction timing)

The serial clock (SCLK) will be gated low outside this block (in the IO). Thus SCLK will always be low when $\overline{CS}$ is high.

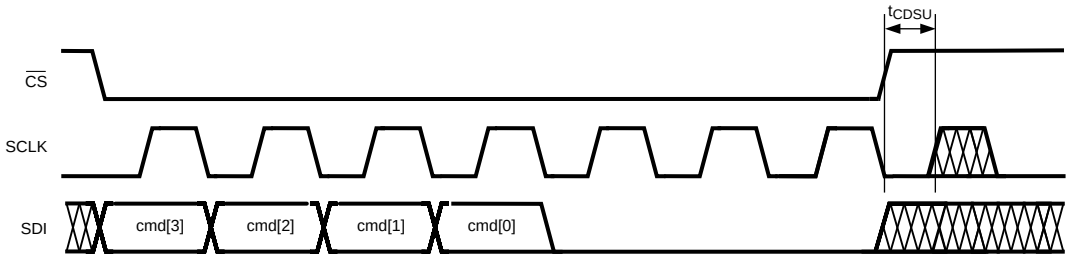

Figure 11. Serial Interface (aborted transaction)

Command Decoding

The EMB1428 will receive the cmd[3:0] from the SPI interface, synchronize it into the internal clock domain, and enable the switches according to the following table:

Table 2. Switch Settings for Each Command

SPI Command	State of Cell Switches	State of Polarity Switches	Description
cmd[3:0]	CSW[7:0]	PSW[3:0]	
0_000	0000_0000	0000	Open all switches
0_001	0000_0011	1001	Connect Cell 1
0_010	0000_0110	0110	Connect Cell 2
0_011	0000_1100	1001	Connect Cell 3
0_100	0001_1000	0110	Connect Cell 4
0_101	0011_0000	1001	Connect Cell 5
0_110	0110_0000	0110	Connect Cell 6
0_111	1100_0000	1001	Connect Cell 7
1_000	0000_0000	0000	Test Mode
1_001	0000_0011	1001	Connect Cell 1
1_010	0000_0110	0110	Connect Cell 2
1_011	0000_1100	1001	Connect Cell 3
1_100	0001_1000	0110	Connect Cell 4
1_101	0011_0000	1001	Connect Cell 5
1_110	0110_0000	0110	Connect Cell 6
1_111	1100_0000	1001	Connect Cell 7

Power On Reset

The following will be asynchronously reset when the internal POR block is triggered:

1. Serial Interface
2. cmd[3:0] = 4'h0
3. FAULT_INT = 1'b0
4. EN = 1'b0
5. PSW[3:0] = 4'h0
6. CSW[7:0] = 8'h00

7. Shutdown Mode = yes
8. Internal Clock = off
9. Normal Mode/Test Mode = Normal Mode

The serial interface is reset so that it is prepared to detect aborted transactions. If POR block isn't triggered, the serial interface will still function. However the initial state of the part will be unknown, so the first transaction may clock out a fault code.

Normal Control Sequencing

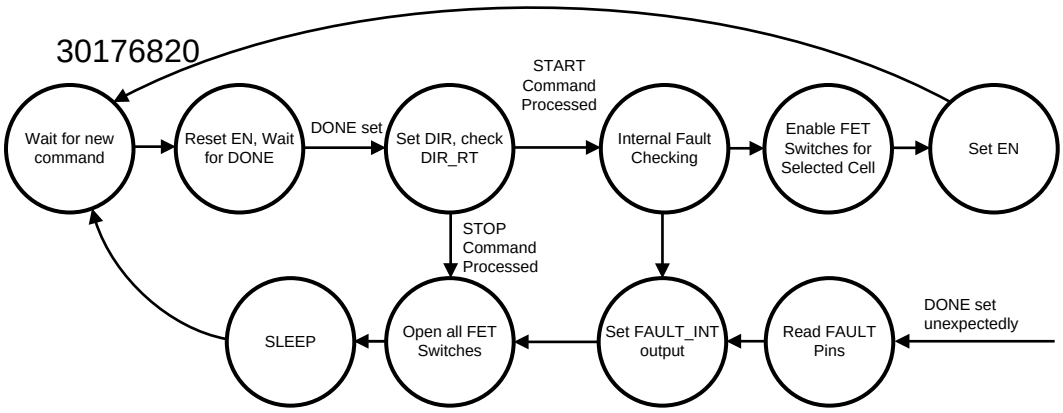

Figure 12. EMB1428 Flowchart

Switches are turned on one at a time to avoid drawing too much current from the charge pump. The following list details the normal sequence that will be used for changing the Switch and EMB1499 Controls each time a new command is received. Exceptions to the sequence (due to errors) will be explained later.

1. Wait for new command.
2. Set EN low.
3. Wait for DONE to be high.
4. Wait for those cell and polarity switches to be turned off as necessitated by the new command.
5. If new command is 4'b0_000 and the EMB1428 is in shutdown mode, go to #1. If new command is not 4'b0_000 and the EMB1428 is in shutdown mode, then exit shutdown mode.
6. Set DIR to be logically equal to the complement of cmd[3]
7. Wait for /DIR_RT to become logically equal to cmd[3]
8. If any switches are currently on, turn off the ones that are not needed for this new command. (All switches can be turned off at once. Switches that are currently on and needed for the new command will not be turned off.)
9. If any switches were turned off in #9, wait for them to complete their turn-off process.
10. If the new command is 4'b0_000 (open all switches), enter shutdown mode. Then go to #1. Otherwise, continue with next step.
11. Turn on next cell switch that is currently off. If all requested cell switches are on, go to #14. (Order for selecting the next cell switch does not matter.)
12. Wait for the cell switch to fully turn on. Then go to #12.
13. Turn on next polarity switch that is currently off. If all requested polarity switches are on, go to #16. (Order for selecting the next polarity switch does not matter.)
14. Wait for the polarity switch to fully turn on. Then go to #14.
15. Set EN high.
16. Wait for DONE to go low.
17. Go to #1.

Any time a new command arrives, the EMB1428 immediately goes back to step #2, regardless of where it was at in the sequence. Any time an error occurs that causes FAULT_INT to go high, the EMB1428 immediately goes back to step #1 and acts as if it received a command to open all switches.

Emergency Shutdown

If the EMB1428 receives two consecutive commands to open all switches (no intervening commands), it will immediately set {CSW[7:0], PSW[3:0]} = 12'h0. This allows all switches to be shut off if there is a problem in the EMB1499 communication or in the EMB1428 charge pump circuitry.

An emergency shutdown will cause the EMB1428 to enter shutdown mode and turn off its internal clock within a few clock cycles without waiting for switches to finish turning on or off.

EMB1499 Control Signaling

The $\overline{\text{DIR\_RT}}$ from the EMB1499 will be synchronized into the EMB1428's internal clock domain. On every rising edge of the internal clock, $\overline{\text{DIR\_RT}}$ will be compared to DIR. If they are ever at the same logic level, a fault will be generated.

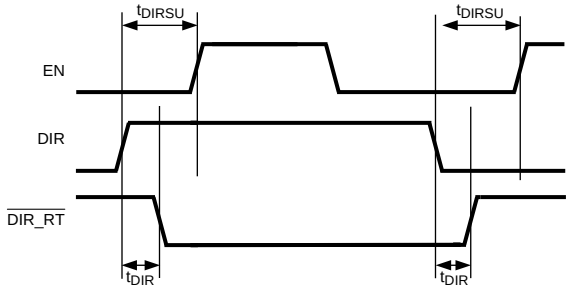

Figure 13. Direction Signals

Error Detection

The EMB1428 contains combinatorial circuitry that will monitor the CSW[7:0], PSW[3:0] outputs for any illegal combination. If an illegal combination occurs, all 12 of the switch control outputs will be forced to zero. The switch control outputs are allowed to glitch low as long as the glitches are typically less than 10ns in length. These short glitches will not pass through the switch circuitry and cause a problem. The switch control output will return to normal operation after the next serial transaction.

This circuitry is included in case the POR circuit does not function or if a radiation event occurs that could be destructive to the battery pack.

The illegal combinations are:

1. More than two bits of CSW[7:0] set.
2. Two non-consecutive bits of CSW[7:0] set.
3. (PSW3 | PSW0) & (PSW2 | PSW1) = 1

Fault Reporting

The EMB1428 detects and reports faults from various sources. If a fault causes FAULT_INT to go high, the IC will immediately act as if it received a command to open all switches: EN will go low, all switches will be turned off, and the IC will enter sleep/shutdown mode. Some faults that are only detected by a subsequent serial transaction do not trigger FAULT_INT and thus do not cause all switches to be opened.

The fault code should always be interpreted as a problem completing the prior command. Reading the fault code clears the fault condition. The EMB1428 will always attempt to perform the command that was sent as the fault code was being read. If two commands are sent in quick succession, a fault may be read when the second command is sent because the first did not have time to complete. At this point, the EMB1428 will attempt to perform the second command.

Serial Interface Faults

If a 9th rising edge of SCLK is detected while $\overline{CS}$ is low (Figure 14), a fault will be generated and the IC will drive FAULT_INT high.

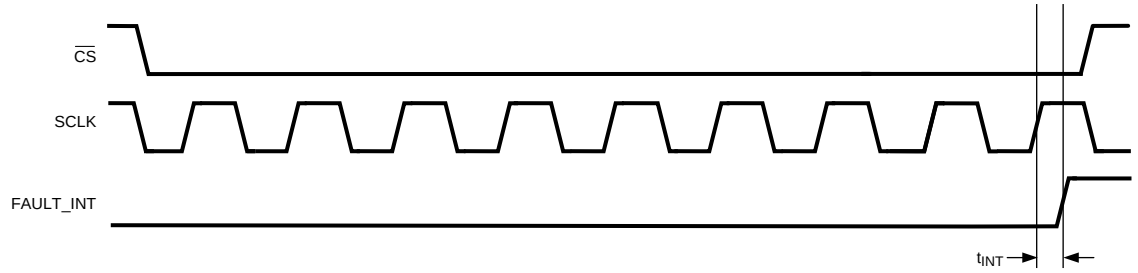

Figure 14. Serial Interface (too many clocks)

If SDI clocks in a high during any of the 4 bits when it should be low, a fault will be generated and the IC will drive FAULT_INT high. See Figure 15.

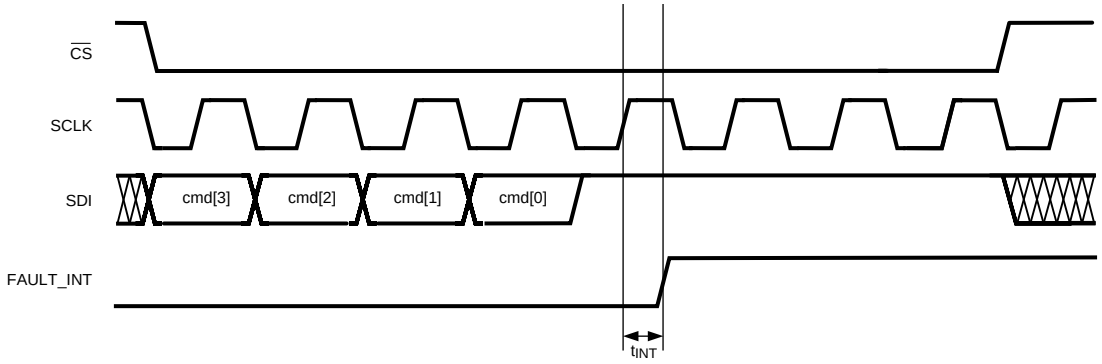

Figure 15. Serial Interface (invalid SDI high)

EMB1499 Control Faults

Incorrect $\overline{DIR\_RT}$

If $\overline{DIR\_RT}$ matches DIR on any rising edge of the internal clock, a fault will be generated and the IC will drive FAULT_INT high. This fault will be masked during serial transactions. If $\overline{DIR\_RT}$ is the wrong value only during the serial transaction, it will be masked and never reported.

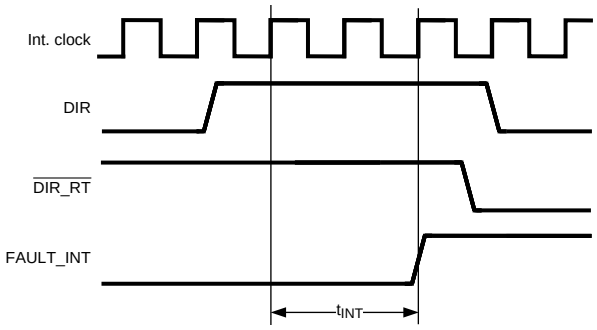

Figure 16. Direction failure (DIR rising case)

EMB1499 Fault

If there is a rising edge on DONE while EN is high, the EMB1428 will detect it as an EMB1499 fault. If this occurs, the EMB1428 will drive FAULT_INT high. If FAULT[2:0] ≠ 000, then the EMB1428 will output the corresponding EMB1499 fault code.

The EMB1499 faults are masked during serial transactions. If an EMB1499 failure occurs between the start of a serial transaction and the falling edge of EN, it will be masked and never reported.

UVLO Tripping

if a UVLO event occurs, the internal signal bg_good will be driven low. If a falling edge is seen on the internal signal bg_good while the EMB1428 is in active mode, the EMB1428 will drive FAULT_INT high.

Previous Command Not Completed

If $\overline{CS}$ goes low and the EMB1428 has not completed its sequence from the previous command, this will generate a fault. These fault conditions will be generated immediately and the fault code will be shifted out in the current serial transaction. The EMB1428 will not drive FAULT_INT high in any of these situations.

If $\overline{CS}$ goes low and the EMB1428 is still waiting for DONE to go high (i.e. the EMB1428 is still waiting for the EMB1499 to stop charging or discharging so it can set up for the command it received on the previous serial transaction), then the EMB1428 will generate a fault.

If $\overline{CS}$ goes low and the EMB1428 has set EN high but is still waiting for DONE to go low, the EMB1428 will generate a fault.

If $\overline{CS}$ goes low while slew is low or the EMB1428 is waiting for the falling edge of slew, the EMB1428 will generate a fault.

If $\overline{CS}$ goes low while bg_good is low and the current command is not 4'h0 (open all switches), the EMB1428 will generate a fault.

Clearing FAULT_INT

The EMB1428 will clear FAULT_INT between the 4th and 6th rising edges of the SCLK. Faults from the EMB1499 that occur between the falling edge of $\overline{CS}$ and the point where DIR is set in the control sequence will be ignored. This way, the user can be assured that triggered faults are always related to the current serial command.

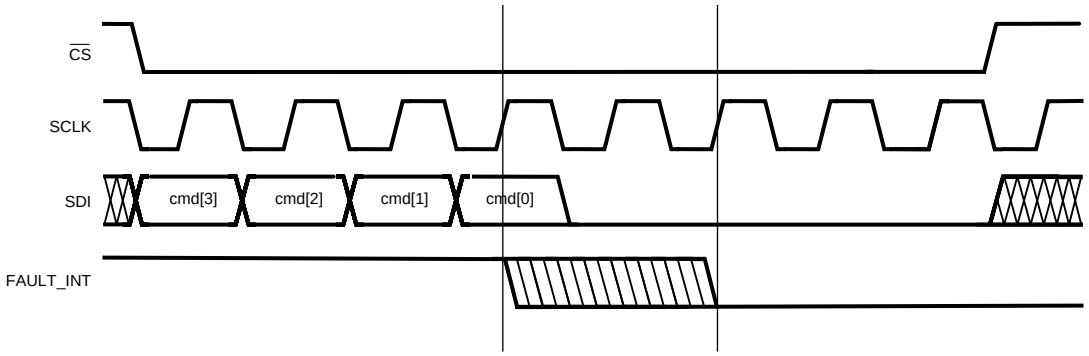

Figure 17. Clearing FAULT_INT

Generating Fault Codes

The EMB1428 will generate FAULT[3:0] according to the following table. This table is in order of priority. So if multiple fault conditions occur, the fault code that is higher in the table will be generated.

Table 3. Fault Codes

Failure Description	fault[3:0]	FAULT_INT triggered?
DONE went high while EN was high and FAULT[2:0] ≠ 000	{1'b0, FAULT[2:0]}	yes
DONE went high while EN was high and FAULT[2:0] = 000	1100	yes
SDI sampled high when it should be low	1101	yes
9th SCLK rising edge seen while $\overline{CS}$ is low		
$\overline{DIR\_RT}$ is not the opposite of DIR	1110	yes
$\overline{CS}$ falling edge while the EMB1428 is still waiting for a transition on DONE (rising or falling edge)	1000	no
$\overline{CS}$ falling edge while slew is low or the EMB1428 is waiting for it to go high	1001	no
$\overline{CS}$ falling edge while bg_good is low and the current command is not 4'h0 (open all switches)	1011	no
bg_good went low after it was sampled high		yes
No fault condition	1010	yes

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	22

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
EMB1428QSQ/NOPB	PREVIEW			48		Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	EMB1428Q	
EMB1428QSQE/NOPB	PREVIEW			48		Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	EMB1428Q	
EMB1428QSX/NOPB	PREVIEW			48		TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
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(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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