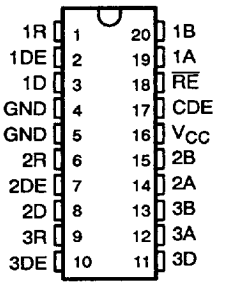
SLLS117A – D3848, APRIL 1991 – REVISED FEBRUARY 1993

- Three Bidirectional Transceivers
- Driver/Receiver Meets EIA Standard RS-485 and ANSI Standard X3.131-1986 (SCSI)
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Wide Positive and Negative Input/Output Bus Voltages Ranges . . . –7 V to 12 V
- Driver Output Capacity . . . ±60 mA
- Driver Positive and Negative Current Limiting
- Thermal Shutdown Protection
- Receiver Input Sensitivity . . . ±200 mV Max
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From a Single 5-V Supply
- Low Supply-Current Requirements 72 mA Max
- Glitch-Free Power-Up and Power-Down Protection

DW OR N PACKAGE
(TOP VIEW)



Function Tables

EACH DRIVER

INPUT	ENABLES		OUTPUTS	
D	DE	CDE	A	B
H	H	H	H	L
L	H	H	L	H
X	L	X	Z	Z
X	X	L	Z	Z

EACH RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
$V_{ID} = -0.2$ V to 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high-level, L = low-level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

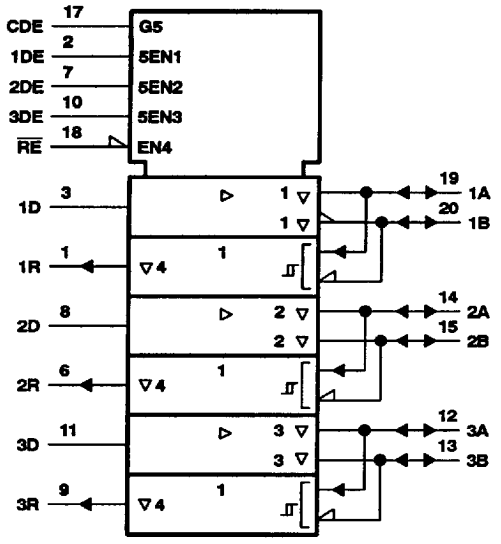
description

The SN75ALS1711 triple differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets EIA Standards RS-485 and ANSI Standard X3.131-1986 (SCSI).

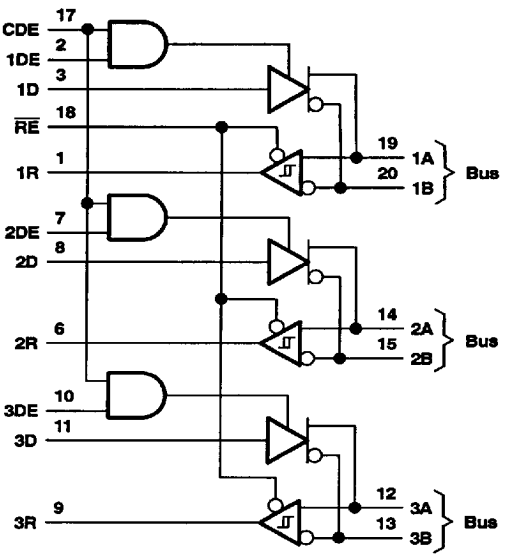
The SN75ALS1711 operates from a single 5-V power supply. The drivers and receivers have individual active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential output and the receiver differential input pairs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} is at 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS1711 is characterized for operation from 0°C to 70°C.

logic symbol†

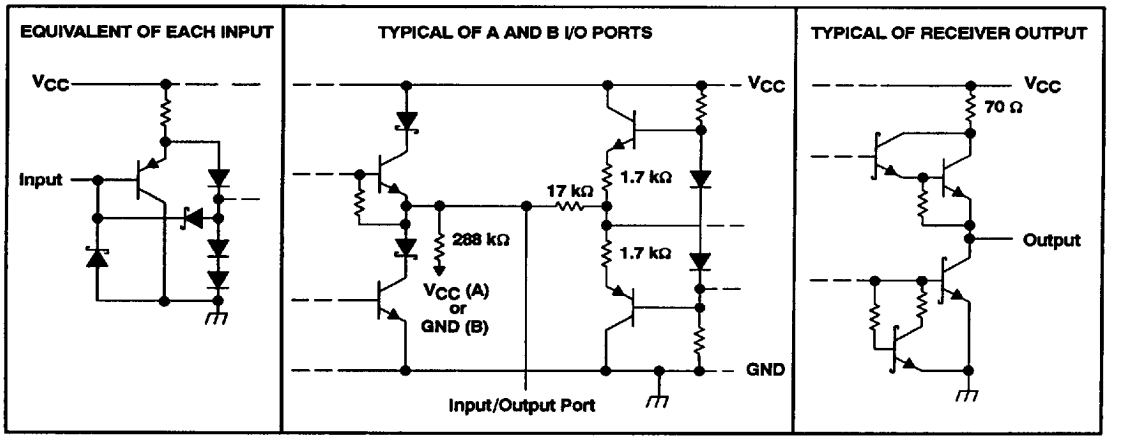


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



All values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Enable input voltage range ..... −0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I: Driver ..... −0.5 V to V_{CC} + 0.5 V
Receiver ..... −9 V to 14 V
Output voltage range, V_O: Driver ..... −9 V to 14 V
Receiver ..... −0.5 V to V_{CC} + 0.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage at any bus terminal, V_{IC} (see Note 2)		−7†		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$, CDE	2			V
Low-level input voltage, V_{IL}	D, DE, $\overline{RE}$, CDE			0.8	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

† The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
V_{OD1}	Differential output voltage	$I_O = 0$		1.5		5	V
V_{OD2}	Differential output voltage	$R_L = 54\ \Omega$, See Figure 1		1.5		5	V
V_{OD3}	Differential output voltage	See Note 3 and Figure 2		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡	$R_L = 54\ \Omega$, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage	$R_L = 54\ \Omega$, See Figure 1				3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡	$R_L = 54\ \Omega$, See Figure 1				±0.2	V
I_{OZ}	High-impedance state output current	Output disabled, $V_{CC} = 5.25$ V	$V_O = 12$ V			1	mA
			$V_O = 7$ V			−0.8	
I_{IH}	High-level input current, DE, EN, CDE	$V_{IH} = 2.4$ V				20	μA
I_{IL}	Low-level input current, DE, EN, CDE	$V_{IL} = 0.4$ V				−200	μA
I_{OS}	Short-circuit output current	$V_O = 12$ V				−250	mA
		$V_O = 7$ V				250	
I_{CC}	Supply current	No load	Outputs enabled		48	72	mA
			Outputs disabled		30	48	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

switching characteristics, $V_{CC} = 5$ V ±5%, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Differential propagation delay time, low-to-high level output	$R_L = 54\ \Omega$, $C_L = 100$ pF, See Figure 3		8	13	22	ns
t_{PHL}	Differential propagation delay time, high-to-low level output			8	15	22	
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$, See Figure 4	S1 open, S2 closed	30	50	60	ns
t_{PHZ}	Output disable time from high level			4	16	30	
t_{PZL}	Output enable time to low level		S1 closed, S2 open	16	26	45	
t_{PLZ}	Output disable time from low level			4	8	20	

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Negative-going threshold voltage	V_O = 0.5 V,	I_O = 4 mA	−0.2‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				50		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	I_I = 18 mA				−1.5	V
V_{OH}	High-level output voltage	I_{OH} = −0.4 mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA				0.5	V
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V,	V_O = 0.4 V to 2.4 V			±20	μA
I_I	Line input current	Other input at 0 V, See Note 3	V_I = 12 V			1	mA
			V_I = 7 V			−0.8	
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2.4 V				20	μA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.4 V				−200	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current§	V_O = 0		−15		−130	mA
I_{CC}	Supply current	No load	Outputs enabled		48	72	mA
			Outputs disabled		30	48	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§ Not more than one output should be shorted at one time.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V ± 5%, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figures 5 and 6		13	20	37	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	20	37	
t_{PZH}	Output enable time to high level	See Figures 5 amd 7	S1 to 1.5 V, S2 open, S3 closed	3	9	20	ns
t_{PHZ}	Output disable time from high level			8	15	22	
t_{PZL}	Output enable time to low level		S1 to −1.5 V, S2 closed, S3 open	5	10	20	
t_{PZL}	Output enable time to low level			5	9	16	

PARAMETER MEASUREMENT INFORMATION

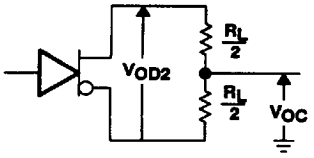


Figure 1. Driver V_{OD} and V_{OC}

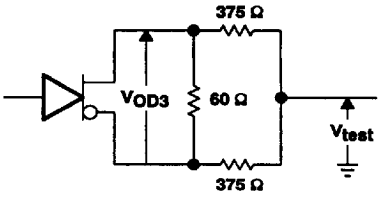
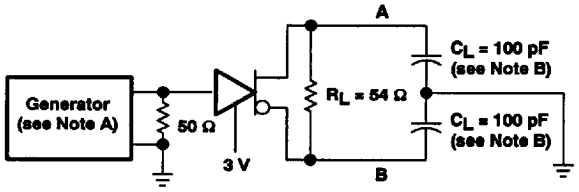


Figure 2. Driver V_{OD3}



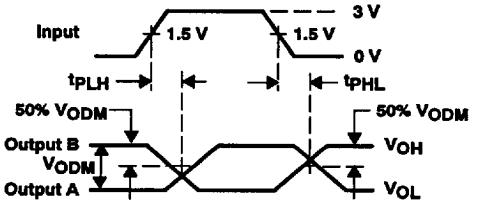
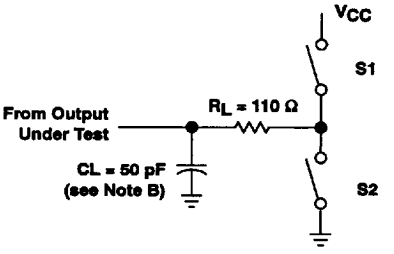


Figure 3. Driver Propagation Delay Times



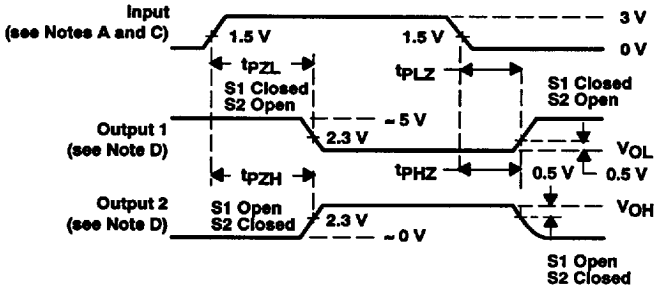


Figure 4. Driver Enable/Disable Times

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.
C. Each enable is tested separately.
D. Output 1 and output 2 are outputs with internal conditions such that the output is low or high except when disabled by the output control.

TEXAS INSTRUMENTS
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PARAMETER MEASUREMENT INFORMATION

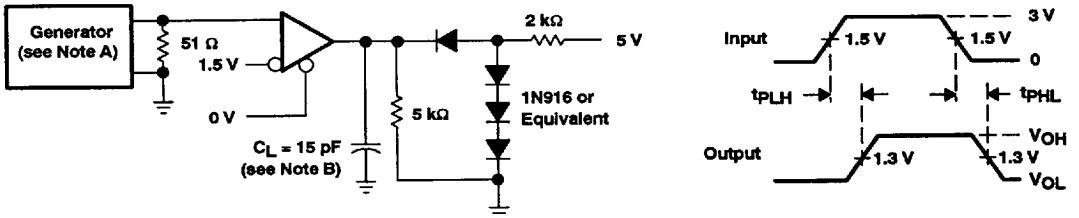

Figure 5. Receiver Propagation Delay Times

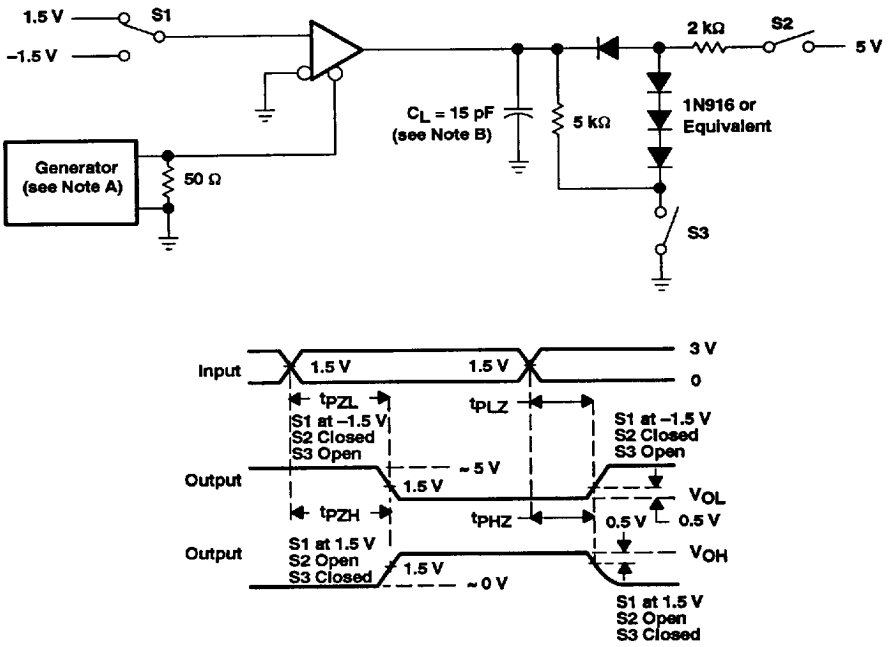

Figure 6. Receiver Enable/Disable Times

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.