

December 1995

### Features

- 14A, 50V
- $r_{DS(ON)} = 0.100\Omega$
- *Temperature Compensating* PSPICE Model
- Can be Driven Directly from CMOS, NMOS, and TTL circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

### Description

The RFD14N05L, RFD14N05LSM, and RFP14N05L are N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

#### PACKAGE AVAILABILITY

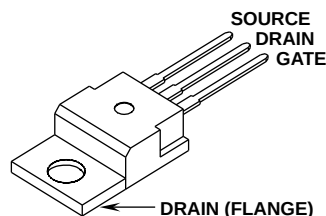
| PART NUMBER | PACKAGE  | BRAND    |
|-------------|----------|----------|
| RFD14N05L   | TO-251AA | 14N05L   |
| RFD14N05LSM | TO-252AA | 14N05L   |
| RFP14N05L   | TO-220AB | FP14N05L |

NOTE: When ordering, use the entire part number. Add the suffix 9A, to obtain the TO-252AA variant in tape and reel, i.e. RFD14N05LSM9A.

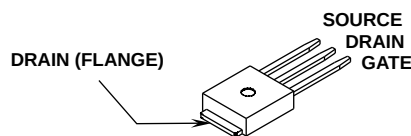
Formerly developmental type TA09870.

### Packaging

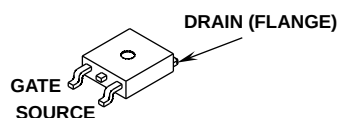
JEDEC TO-220AB



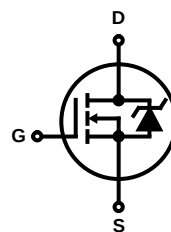
JEDEC TO-251AA



JEDEC TO-252AA



### Symbol



### Absolute Maximum Ratings $T_C = +25^\circ\text{C}$

|                                                  | RFD14N05L, RFD14N05LSM, RFP14N05L | UNITS                       |
|--------------------------------------------------|-----------------------------------|-----------------------------|
| Drain-Source Voltage . . . . .                   | $V_{DSS}$ 50                      | V                           |
| Drain-Gate Voltage . . . . .                     | $V_{DGR}$ 50                      | V                           |
| Gate-Source Voltage . . . . .                    | $V_{GS}$ $\pm 10$                 | V                           |
| Drain Current                                    |                                   |                             |
| RMS Continuous . . . . .                         | $I_D$ 14                          | A                           |
| Pulsed Drain Current . . . . .                   | $I_{DM}$                          | Refer to Peak Current Curve |
| Pulsed Avalanche Rating . . . . .                | $E_{AS}$                          | Refer to UIS Curve          |
| Power Dissipation                                |                                   |                             |
| $T_C = +25^\circ\text{C}$ . . . . .              | $P_D$ 48                          | W                           |
| Derate above +25°C . . . . .                     | 0.32                              | W/°C                        |
| Operating and Storage Temperature . . . . .      | $T_{STG}, T_J$ -55 to +175        | °C                          |
| Soldering Temperature of Leads for 10s . . . . . | $T_L$ 260                         | °C                          |

## Specifications RFD14N05L, RFD14N05LSM, RFP14N05L

### Electrical Specifications $T_C = +25^{\circ}\text{C}$ , Unless Otherwise Specified

| PARAMETERS                             | SYMBOL          | TEST CONDITIONS                                                                                                 | MIN | TYP | MAX   | UNITS                |
|----------------------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------|-----|-----|-------|----------------------|
| Drain-Source Breakdown Voltage         | $BV_{DSS}$      | $I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$                                                                   | 50  | -   | -     | V                    |
| Gate Threshold Voltage                 | $V_{GS(TH)}$    | $V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$                                                                      | 1   | -   | 2     | V                    |
| Zero Gate Voltage Drain Current        | $I_{DSS}$       | $V_{DS} = 50\text{V}$ , $V_{GS} = 0\text{V}$ , $T_C = +25^{\circ}\text{C}$                                      | -   | -   | 1     | $\mu\text{A}$        |
|                                        |                 | $T_C = +150^{\circ}\text{C}$                                                                                    | -   | -   | 50    | $\mu\text{A}$        |
| Gate-Source Leakage Current            | $I_{GSS}$       | $V_{GS} = \pm 10\text{V}$                                                                                       | -   | -   | 100   | nA                   |
| On Resistance                          | $r_{DS(ON)}$    | $I_D = 14\text{A}$ , $V_{GS} = 5\text{V}$                                                                       | -   | -   | 0.100 | $\Omega$             |
| Turn-On Time                           | $t_{ON}$        | $V_{DD} = 25\text{V}$ , $I_D = 7\text{A}$ , $R_L = 3.57\Omega$ ,<br>$V_{GS} = 5\text{V}$ , $R_{GS} = 0.6\Omega$ | -   | -   | 60    | ns                   |
| Turn-On Delay Time                     | $t_{D(ON)}$     |                                                                                                                 | -   | 13  | -     | ns                   |
| Rise Time                              | $t_R$           |                                                                                                                 | -   | 24  | -     | ns                   |
| Turn-Off Delay Time                    | $t_{D(OFF)}$    |                                                                                                                 | -   | 42  | -     | ns                   |
| Fall Time                              | $t_F$           |                                                                                                                 | -   | 16  | -     | ns                   |
| Turn-Off Time                          | $t_{OFF}$       |                                                                                                                 | -   | -   | 100   | ns                   |
| Total Gate Charge                      | $Q_{G(TOT)}$    | $V_{GS} = 0\text{V}$ to $10\text{V}$                                                                            | -   | -   | 40    | nC                   |
| Gate Charge at 5V                      | $Q_{G(5)}$      | $V_{GS} = 0\text{V}$ to $5\text{V}$                                                                             | -   | -   | 25    | nC                   |
| Threshold Gate Charge                  | $Q_{G(TH)}$     | $V_{GS} = 0\text{V}$ to $1\text{V}$                                                                             | -   | -   | 1.5   | nC                   |
| Input Capacitance                      | $C_{ISS}$       | $V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ ,<br>$f = 1\text{MHz}$                                             | -   | 670 | -     | pF                   |
| Output Capacitance                     | $C_{OSS}$       |                                                                                                                 | -   | 185 | -     | pF                   |
| Reverse Transfer Capacitance           | $C_{RSS}$       |                                                                                                                 | -   | 50  | -     | pF                   |
| Thermal Resistance Junction-to-Case    | $R_{\theta JC}$ |                                                                                                                 | -   | -   | 3.125 | $^{\circ}\text{C/W}$ |
| Thermal Resistance Junction-to-Ambient | $R_{\theta JA}$ | TO -251 and TO-252                                                                                              | -   | -   | 100   | $^{\circ}\text{C/W}$ |
|                                        |                 | TO-220                                                                                                          | -   | -   | 80    | $^{\circ}\text{C/W}$ |

### Source-Drain Diode Ratings and Specifications

| PARAMETERS            | SYMBOL   | TEST CONDITIONS                                                | MIN | TYP | MAX | UNITS |
|-----------------------|----------|----------------------------------------------------------------|-----|-----|-----|-------|
| Forward Voltage       | $V_{SD}$ | $I_{SD} = 14\text{A}$                                          | -   | -   | 1.5 | V     |
| Reverse Recovery Time | $t_{RR}$ | $I_{SD} = 14\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$ | -   | -   | 125 | ns    |

## Typical Performance Curves

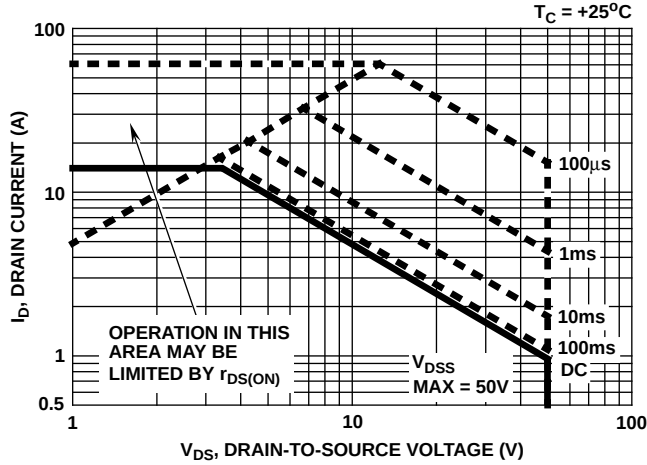


FIGURE 1. SAFE OPERATING AREA CURVE

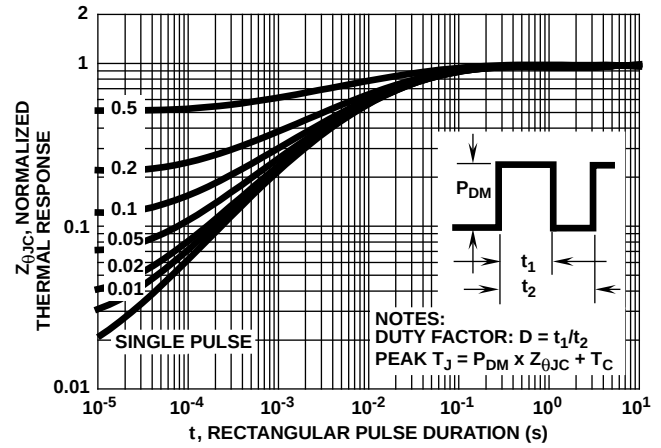


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

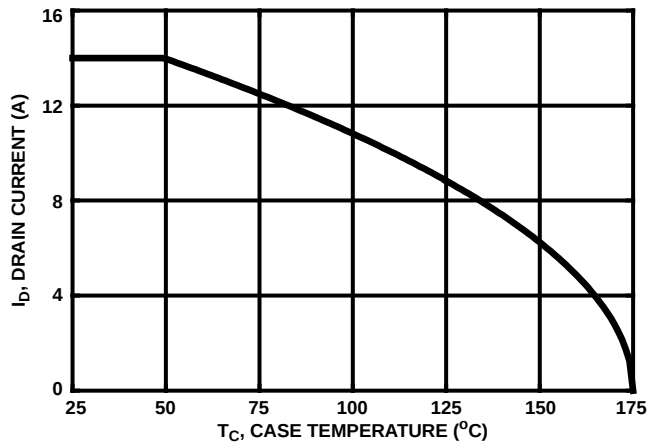


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

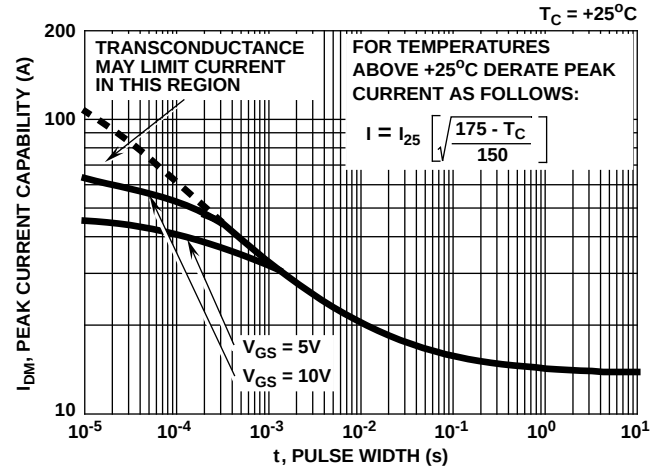


FIGURE 4. PEAK CURRENT CAPABILITY

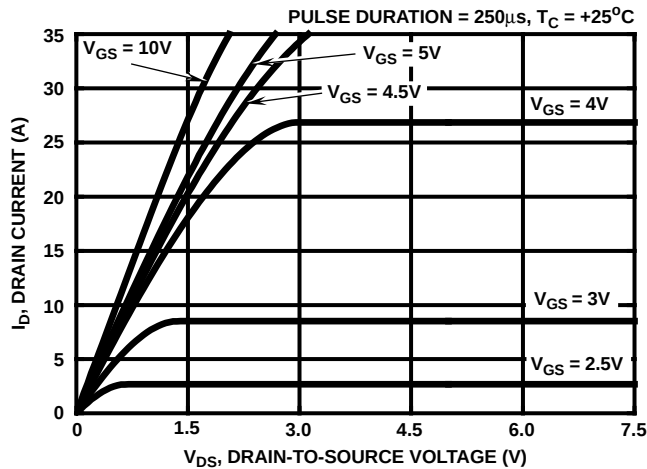


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

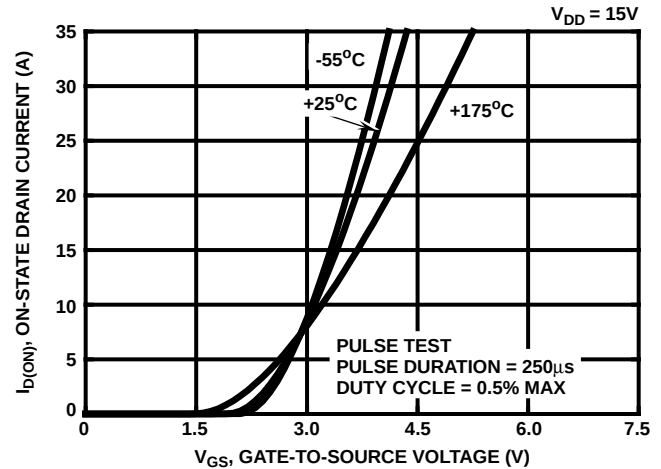


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

# Typical Performance Curves (Continued)

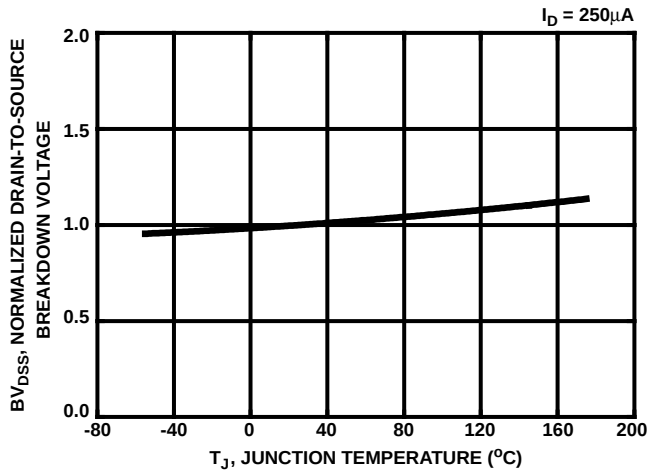


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

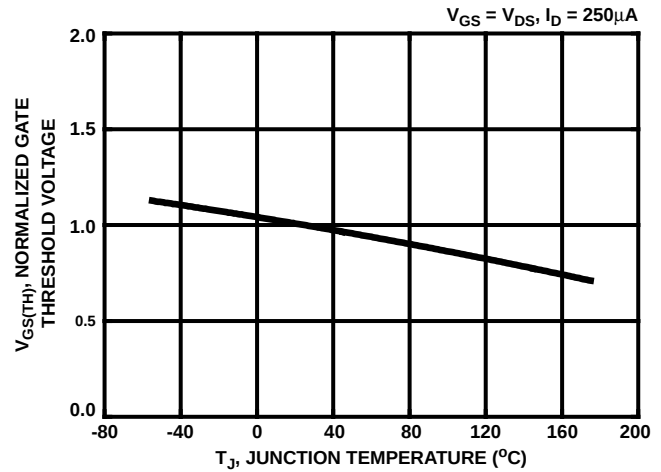


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

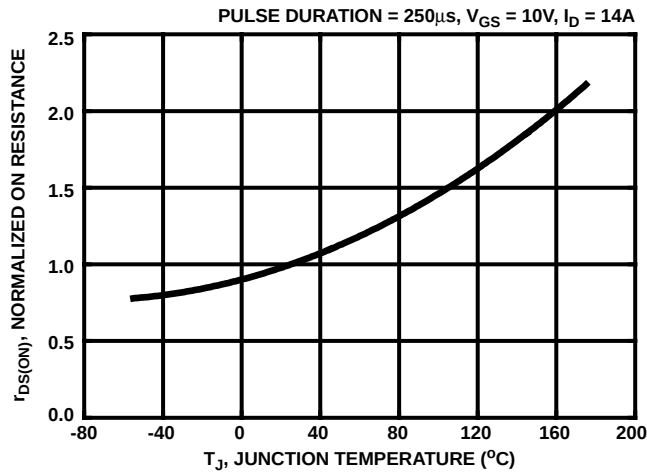


FIGURE 9. NORMALIZED  $r_{DS(ON)}$  vs JUNCTION TEMPERATURE

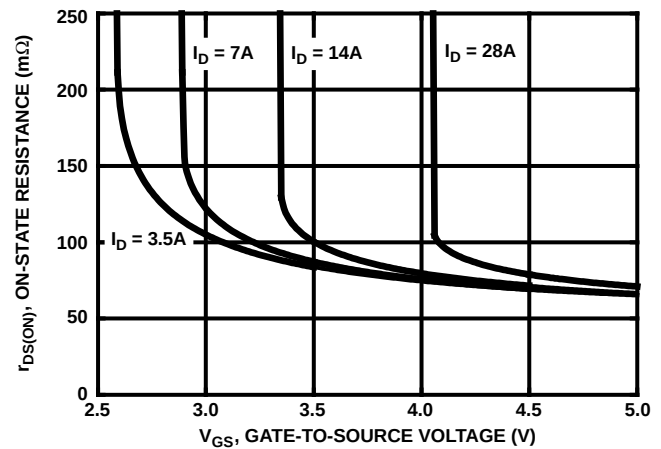


FIGURE 10.  $r_{DS(ON)}$  FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

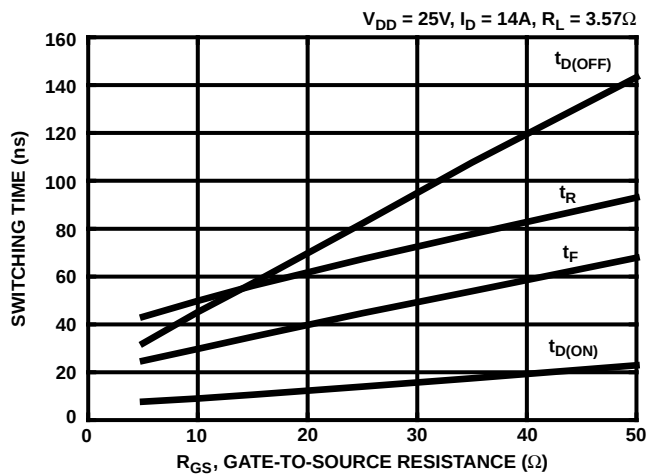


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

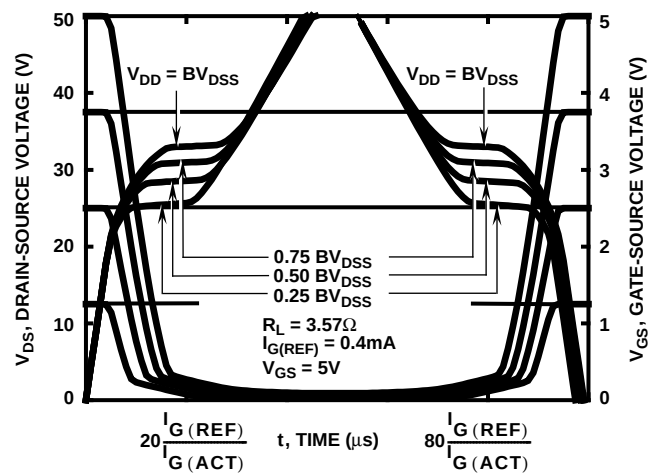


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

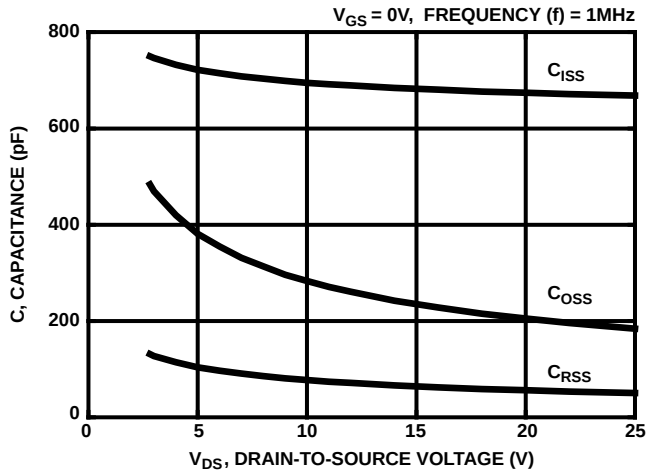


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

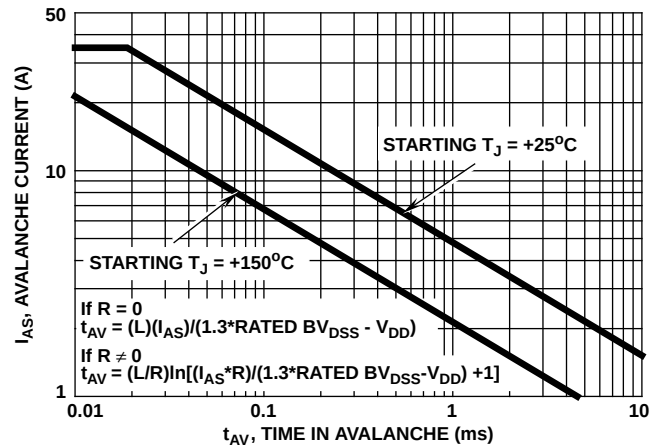


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

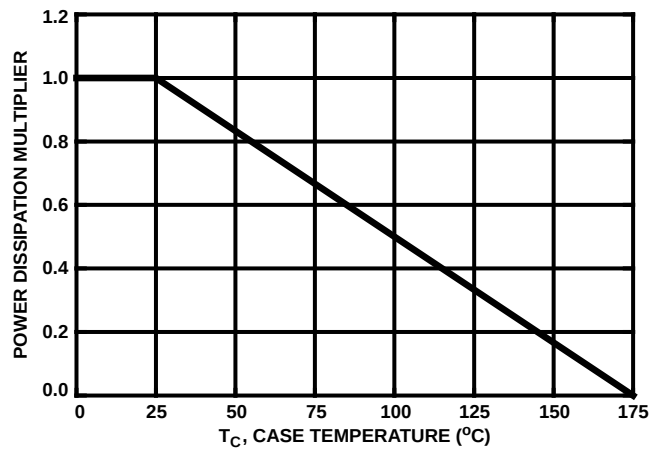


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

## Test Circuits and Waveforms

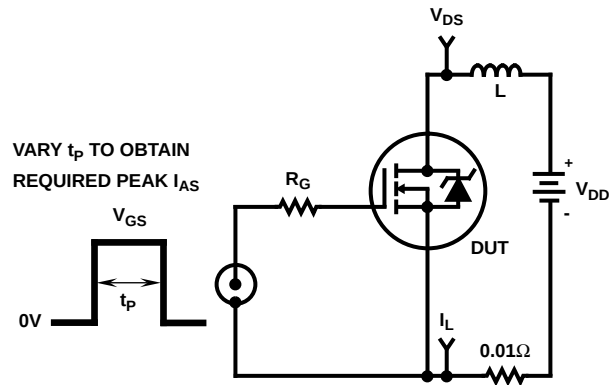


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

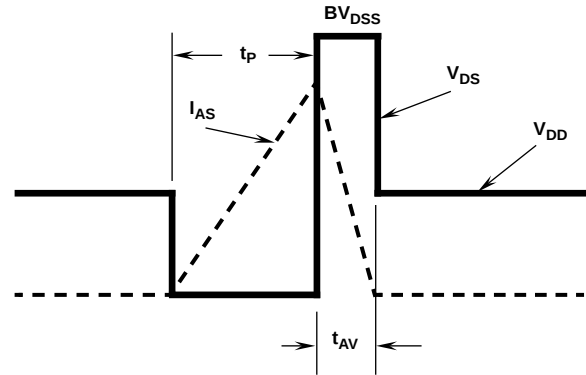


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

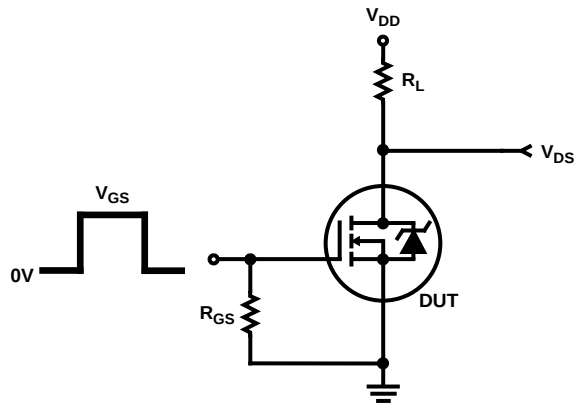


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

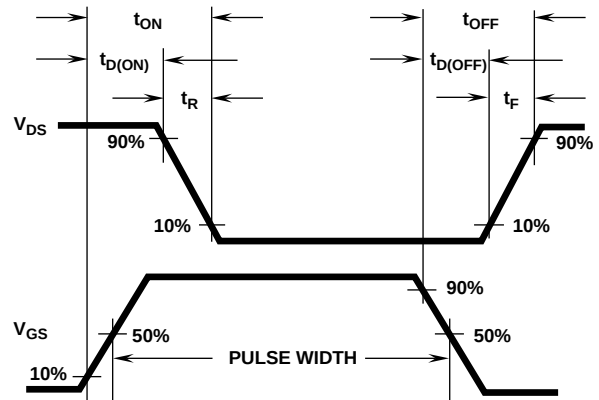


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

***RFD14N05L, RFD14N05LSM, RFP14N05L***

### ***Temperature Compensated PSPICE Model for the RFD14N05L, RFD14N05LSM, RFP14N05L***

SUBCKT RFP14N05L 2 1 3 ; rev 9/15/94

|     |    |    |          |
|-----|----|----|----------|
| CA  | 12 | 8  | 1.464e-9 |
| CB  | 15 | 14 | 1.64e-9  |
| CIN | 6  | 8  | 6.17e-10 |

```
DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD
```

```
EBREAK 11 7 17 18 65.35
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1
```

IT 8 17 1

```
LDRAIN 2 5 1e-9
LGATE 1 9 5.68e-9
LSOURCE 3 7 5.35e-9
```

MOS1 16 6 8 8 MOSMOD M = 0.99  
MOS2 16 21 8 8 MOSMOD M = 0.01

```
RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 33.1e-3
RGATE 9 20 5.85
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 14.3e-3
RVTO 18 19 RVTOMOD 1
```

```
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD
```

```
VBAT 8 19 DC 1
VTO 21 6 0.485
```

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)\*1e6/46,7))}

```
.MODEL DBDMOD D (IS = 2.23e-13 RS = 1.15e-2 TRS1 = 1.64e-3 TRS2 = 7.89e-6 CJO = 6.83e-10 TT = 3.68e-8)
.MODEL DBKMOD D (RS = 3.8e-1 TRS1 = 1.89e-3 TRS2 = 1.13e-5)
.MODEL DPLCAPMOD D (CJO = 25.7e-11 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 1.935 KP = 18.89 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 7.18e-4 TC2 = 1.53e-6)
.MODEL RDSMOD RES (TC1 = 4.45e-3 TC2 = 2.9e-5)
.MODEL RSCLMOD RES (TC1 = 2.8e-3 TC2 = 6.0e-6)
.MODEL RVTOMOD RES (TC1 = -1.7e-3 TC2 = -2.0e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.55 VOFF = -1.55)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.55 VOFF = -3.55)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.55 VOFF = 2.45)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.45 VOFF = -2.55)
```

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

