

SIEMENS

Microcomputer Components

8-Bit CMOS Microcontroller

C517A

Data Sheet 10.97

C517A Data Sheet

Revision History: **Current Version: 10.97**

Previous Version: none

Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)

Edition 10.97

**Published by Siemens AG,
Bereich Halbleiter, Marketing-
Kommunikation, Balanstraße 73,
81541 München**

© Siemens AG 1997.
All Rights Reserved.

Attention please!

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact the Semiconductor Group Offices in Germany or the Siemens Companies and Representatives worldwide (see address list).

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Siemens Office, Semiconductor Group.

Siemens AG is an approved CECC manufacturer.

Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.

For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

Components used in life-support devices or systems must be expressly authorized for such purpose!

Critical components¹ of the Semiconductor Group of Siemens AG, may only be used in life-support devices or systems² with the express written approval of the Semiconductor Group of Siemens AG.

- 1 A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.
- 2 Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.

Advance Information

- Full upward compatibility with SAB 80C517A/83C517A-5
- Up to 24 MHz external operating frequency
 - 500 ns instruction cycle at 24 MHz operation
- Superset of the 8051 architecture with 8 datapointers
- On-chip emulation support logic (Enhanced Hooks Technology™)
- 32K byte on-chip ROM (with optional ROM protection)
 - alternatively up to 64K byte external program memory
- Up to 64K byte external data memory
- 256 byte on-chip RAM
- Additional 2K byte on-chip RAM (XRAM)
- Seven 8-bit parallel I/O ports
- Two input ports for analog/digital input

(further features are on next page)

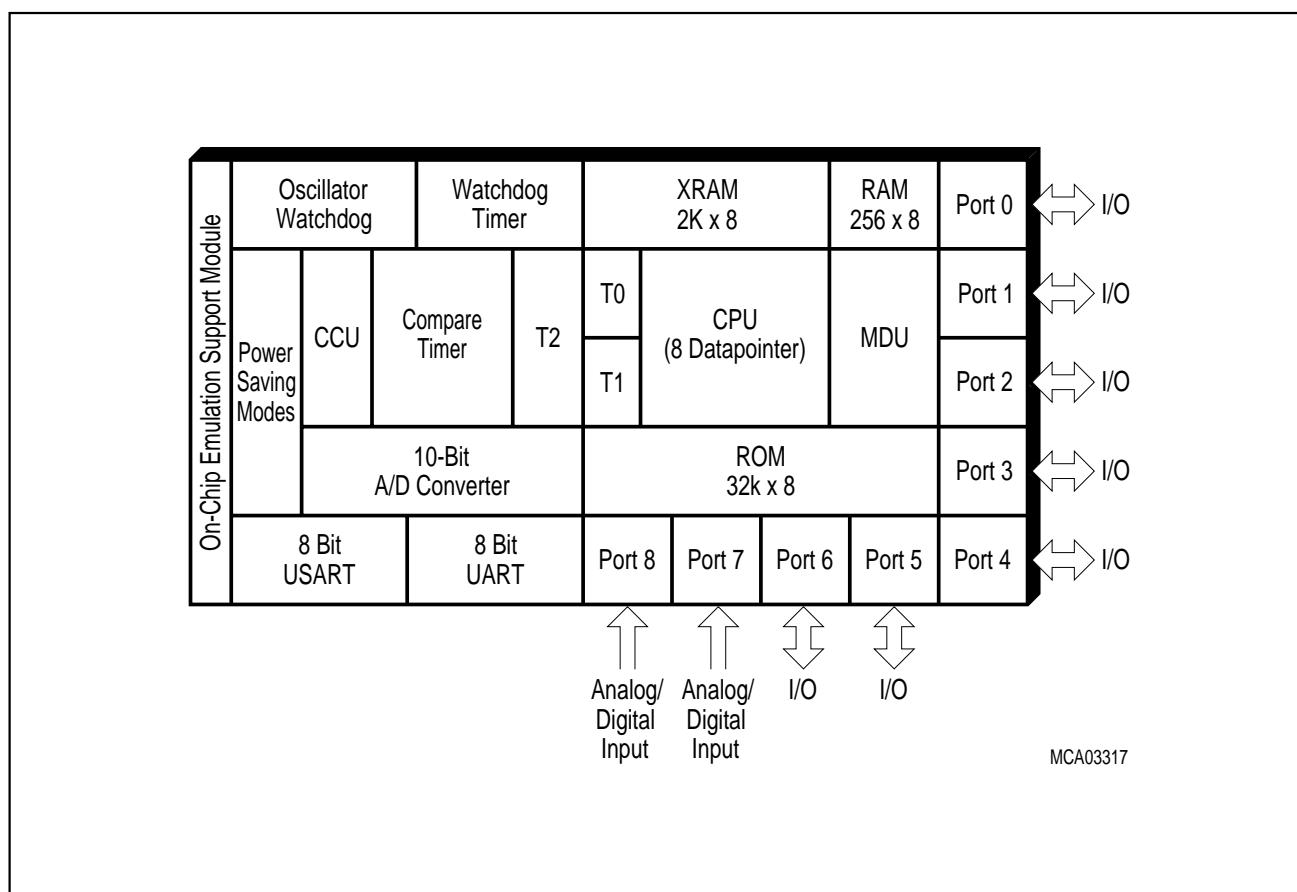


Figure 1
C517A Functional Units

Features (cont'd):

- Two full duplex serial interfaces (USART)
 - 4 operating modes, fixed or variable baud rates
 - programmable baud rate generators
- Four 16-bit timer/counters
 - Timer 0 / 1 (C501 compatible)
 - Timer 2 for 16-bit reload, compare, or capture functions
 - Compare timer for compare/capture functions
- Powerful 16-bit compare/capture unit (CCU) with up to 21 high-speed or PWM output channels and 5 capture inputs
- 10-bit A/D converter
 - 12 multiplexed analog inputs
 - Built-in self calibration
- Extended watchdog facilities
 - 15-bit programmable watchdog timer
 - Oscillator watchdog
- Power saving modes
 - Slow down mode
 - Idle mode (can be combined with slow down mode)
 - Software power-down mode
 - Hardware power-down mode
- 17 interrupt sources (7 external, 10 internal) selectable at 4 priority levels
- P-MQFP-100 packages
- Temperature Ranges: SAB-C517A $T_A = 0$ to 70 °C
SAF-C517A $T_A = -40$ to 85 °C
SAH-C517A $T_A = -40$ to 110 °C

Table 1
Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C517A-4RM	Q67120-DXXXX	P-MQFP-100-2	with mask programmable ROM (18 MHz)
SAF-C517A-4RM	Q67120-DXXXX	P-MQFP-100-2	with mask programmable ROM (18 MHz) ext. temp. – 40 °C to 85 °C
SAB-C517A-4R24M	Q67120-DXXXX	P-MQFP-100-2	with mask programmable ROM (24 MHz)
SAF-C517A-4R24M	Q67120-DXXXX	P-MQFP-100-2	with mask programmable ROM (24 MHz) ext. temp. – 40 °C to 85 °C
SAB-C517A-LM	Q67127-C1071	P-MQFP-100-2	for external memory (18 MHz)
SAF-C517A-LM	Q67127-C1063	P-MQFP-100-2	for external memory (18 MHz) ext. temp. – 40 °C to 85 °C
SAB-C517A-L24M	Q67127-C1072	P-MQFP-100-2	for external memory (24 MHz)

Note: Versions for extended temperature ranges – 40 °C to 110 °C (SAH-C517A) are available on request. The ordering number of ROM types (DXXXX extensions) is defined after program release (verification) of the customer.

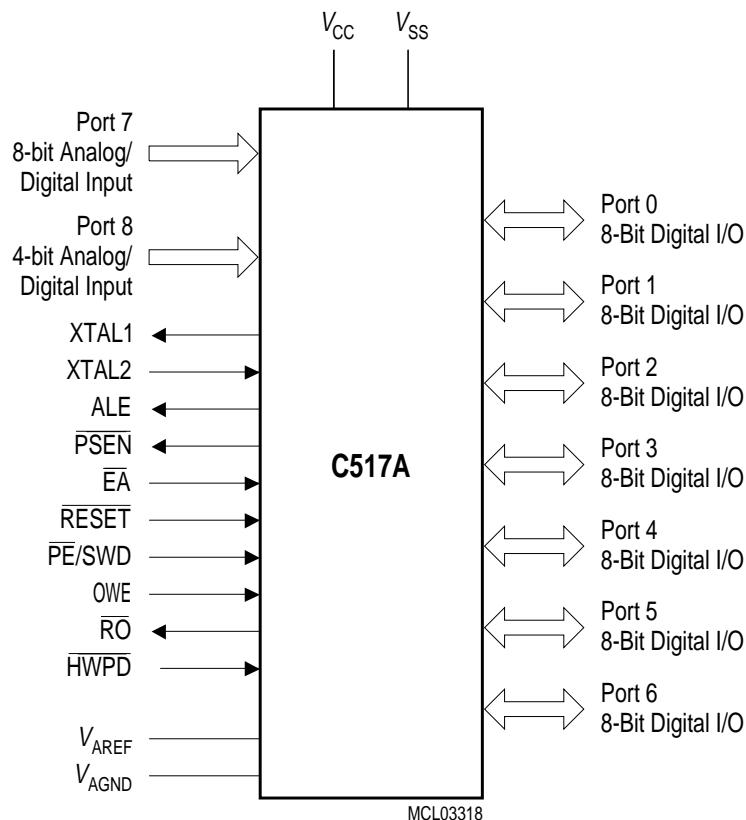


Figure 2
Logic Symbol

Additional Literature

For further information about the C517A the following literature is available:

Title	Ordering Number
C517A 8-Bit CMOS Microcontroller User's Manual	B158-H7053-X-X-7600
C500 Microcontroller Family Architecture and Instruction Set User's Manual	B158-H6987-X-X-7600
C500 Microcontroller Family - Pocket Guide	B158-H6986-X-X-7600

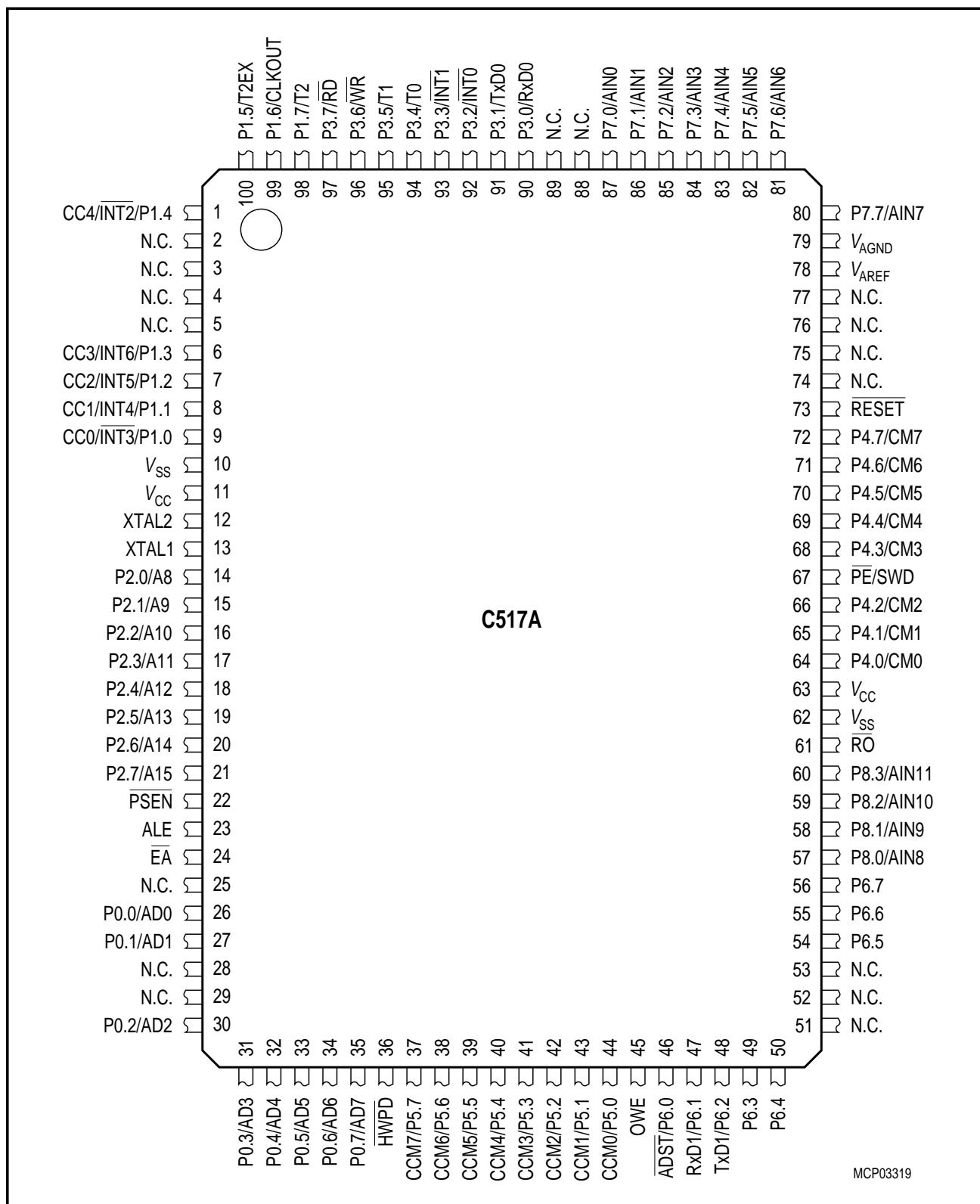


Figure 3
Pin Configuration P-MQFP-100 Package (Top View)

Table 2
Pin Definitions and Functions

Symbol	Pin Number	I/O*	Function																																								
			P-MQFP-100																																								
P1.0 - P1.7	9 - 6, 1, 100 - 98	I/O	<p>Port 1 is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. The port is used for the low-order address byte during program verification. Port 1 also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows:</p> <table> <tbody> <tr> <td>9</td> <td>P1.0</td> <td>INT3</td> <td>CC0</td> <td>Interrupt 3 input / compare 0 output / capture 0 input</td> </tr> <tr> <td>8</td> <td>P1.1</td> <td>INT4</td> <td>CC1</td> <td>Interrupt 4 input / compare 1 output / capture 1 input</td> </tr> <tr> <td>7</td> <td>P1.2</td> <td>INT5</td> <td>CC2</td> <td>Interrupt 5 input / compare 2 output / capture 2 input</td> </tr> <tr> <td>6</td> <td>P1.3</td> <td>INT6</td> <td>CC3</td> <td>Interrupt 6 input / compare 3 output / capture 3 input</td> </tr> <tr> <td>1</td> <td>P1.4</td> <td>INT2</td> <td></td> <td>Interrupt 2 input</td> </tr> <tr> <td>100</td> <td>P1.5</td> <td>T2EX</td> <td></td> <td>Timer 2 external reload / trigger input</td> </tr> <tr> <td>99</td> <td>P1.6</td> <td>CLKOUT</td> <td></td> <td>System clock output</td> </tr> <tr> <td>98</td> <td>P1.7</td> <td>T2</td> <td></td> <td>Counter 2 input</td> </tr> </tbody> </table>	9	P1.0	INT3	CC0	Interrupt 3 input / compare 0 output / capture 0 input	8	P1.1	INT4	CC1	Interrupt 4 input / compare 1 output / capture 1 input	7	P1.2	INT5	CC2	Interrupt 5 input / compare 2 output / capture 2 input	6	P1.3	INT6	CC3	Interrupt 6 input / compare 3 output / capture 3 input	1	P1.4	INT2		Interrupt 2 input	100	P1.5	T2EX		Timer 2 external reload / trigger input	99	P1.6	CLKOUT		System clock output	98	P1.7	T2		Counter 2 input
9	P1.0	INT3	CC0	Interrupt 3 input / compare 0 output / capture 0 input																																							
8	P1.1	INT4	CC1	Interrupt 4 input / compare 1 output / capture 1 input																																							
7	P1.2	INT5	CC2	Interrupt 5 input / compare 2 output / capture 2 input																																							
6	P1.3	INT6	CC3	Interrupt 6 input / compare 3 output / capture 3 input																																							
1	P1.4	INT2		Interrupt 2 input																																							
100	P1.5	T2EX		Timer 2 external reload / trigger input																																							
99	P1.6	CLKOUT		System clock output																																							
98	P1.7	T2		Counter 2 input																																							
V_{SS}	10, 62	—	Ground (0V) during normal, idle, and power down operation.																																								
V_{CC}	11, 63	—	Supply voltage during normal, idle, and power down mode.																																								

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*	Function
			P-MQFP-100
XTAL2	12	—	<p>XTAL2 is the input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.</p>
XTAL1	13	—	<p>XTAL1 is the output of the inverting oscillator amplifier. This pin is used for the oscillator operation with crystal or ceramic resonator.</p>
P2.0 - P2.7	14 - 21	I/O	<p>Port 2 is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1's. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.</p>
PSEN	22	O	<p>The Program Store Enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. The signal remains high during internal program execution.</p>
ALE	23	O	<p>The Address Latch enable output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.</p>

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*	Function
			P-MQFP-100
EA	24	I	External Access Enable When held high, the C517A executes instructions from the internal ROM as long as the PC is less than 8000 _H . When held low, the C517A fetches all instructions from external program memory. For the C517A-L this pin must be tied low.
P0.0 - P0.7	26, 27, 30 - 35	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the C517A. External pullup resistors are required during program verification.
HWPD	36	I	Hardware Power Down A low level on this pin for the duration of one machine cycle while the oscillator is running resets the C517A. A low level for a longer period will force the part into hardware power down mode with the pins floating. There is no internal pullup resistor connected to this pin.
P5.0 - P5.7	44 - 37	I/O	Port 5 is a quasi-bidirectional I/O port with internal pull-up resistors. Port 5 pins that have 1's written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL} , in the DC characteristics) because of the internal pull-up resistors. This port also serves the alternate function "Concurrent Compare" and "Set/Reset Compare". The secondary functions are assigned to the port 5 pins as follows: CCM0 to CCM7 P5.0 to P5.7: concurrent compare or Set/Reset lines

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*	Function												
			P-MQFP-100												
OWE	45	I	<p>Oscillator Watchdog Enable A high level on this pin enables the oscillator watchdog. When left unconnected this pin is pulled high by a weak internal pull-up resistor. The logic level at OWE should not be changed during normal operation. When held at low level the oscillator watchdog function is turned off. During hardware power down the pullup resistor is switched off.</p>												
P6.0 - P6.7	46 - 50, 54 - 56	I/O	<p>Port 6 is a quasi-bidirectional I/O port with internal pull-up resistors. Port 6 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 6 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 6 also contains the external A/D converter control pin and the transmit and receive pins for the serial interface 1. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 6, as follows:</p> <table> <tr> <td>46</td> <td>P6.0</td> <td>\overline{ADST}</td> <td>external A/D converter start pin</td> </tr> <tr> <td>47</td> <td>P6.1</td> <td>RxD1</td> <td>receiver data input of serial interface 1</td> </tr> <tr> <td>48</td> <td>P6.2</td> <td>TxD1</td> <td>transmitter data input of serial interface 1</td> </tr> </table>	46	P6.0	\overline{ADST}	external A/D converter start pin	47	P6.1	RxD1	receiver data input of serial interface 1	48	P6.2	TxD1	transmitter data input of serial interface 1
46	P6.0	\overline{ADST}	external A/D converter start pin												
47	P6.1	RxD1	receiver data input of serial interface 1												
48	P6.2	TxD1	transmitter data input of serial interface 1												
P8.0 - P8.3	57 - 60	I	<p>Port 8 is a 4-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the higher 4-bit of the multiplexed analog inputs of the A/D converter, simultaneously. P8.0 - P8.3 AIN8 - AIN11 analog input 8 - 14</p>												
\overline{RO}	61	O	<p>Reset Output This pin outputs the internally synchronized reset request signal. This signal may be generated by an external hardware reset, a watchdog timer reset or an oscillator watchdog reset. The \overline{RO} is active low.</p>												

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*	Function
			P-MQFP-100
P4.0 - P4.7	64 - 66, 68 - 72	I/O	<p>Port 4 is an 8-bit quasi-bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1's written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors.</p>
PE/SWD	67	I	<p>Power saving mode enable / Start watchdog timer A low level at this pin allows the software to enter the power saving modes (idle mode, slow down mode, and power down mode). In case the low level is also seen during reset, the watchdog timer function is off on default. Usage of the software controlled power saving modes is blocked, when this pin is held at high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor. During hardware power down the pullup resistor is switched off.</p>
RESET	73	I	<p>RESET A low level on this pin for the duration of two machine cycles while the oscillator is running resets the C517A. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.</p>
V_{AREF}	78	—	Reference voltage for the A/D converter
V_{AGND}	79	—	Reference ground for the A/D converter
P7.0 - P7.7	87 - 80		<p>Port 7 is an 8-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the lower 8-bit of the multiplexed analog inputs of the A/D converter, simultaneously. P7.0 - P7.7 AIN0 - AIN7 analog input 8 - 14</p>

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*	Function																																
			P-MQFP-100																																
P3.0 - P3.7	90 - 97	I/O	<p>Port 3 is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:</p> <table> <tr> <td>90</td> <td>P3.0</td> <td>RxD0</td> <td>Receiver data input (asynch.) or data input/output (synch.) of serial interface 0</td> </tr> <tr> <td>91</td> <td>P3.1</td> <td>TxD0</td> <td>Transmitter data output (asynch.) or clock output (synch.) of serial interface 0</td> </tr> <tr> <td>92</td> <td>P3.2</td> <td>INT0</td> <td>External interrupt 0 input / timer 0 gate control input</td> </tr> <tr> <td>93</td> <td>P3.3</td> <td>INT1</td> <td>External interrupt 1 input / timer 1 gate control input</td> </tr> <tr> <td>94</td> <td>P3.4</td> <td>T0</td> <td>Timer 0 counter input</td> </tr> <tr> <td>95</td> <td>P3.5</td> <td>T1</td> <td>Timer 1 counter input</td> </tr> <tr> <td>96</td> <td>P3.6</td> <td>WR</td> <td>WR control output; latches the data byte from port 0 into the external data memory</td> </tr> <tr> <td>97</td> <td>P3.7</td> <td>RD</td> <td>RD control output; enables the external data memory</td> </tr> </table>	90	P3.0	RxD0	Receiver data input (asynch.) or data input/output (synch.) of serial interface 0	91	P3.1	TxD0	Transmitter data output (asynch.) or clock output (synch.) of serial interface 0	92	P3.2	INT0	External interrupt 0 input / timer 0 gate control input	93	P3.3	INT1	External interrupt 1 input / timer 1 gate control input	94	P3.4	T0	Timer 0 counter input	95	P3.5	T1	Timer 1 counter input	96	P3.6	WR	WR control output; latches the data byte from port 0 into the external data memory	97	P3.7	RD	RD control output; enables the external data memory
90	P3.0	RxD0	Receiver data input (asynch.) or data input/output (synch.) of serial interface 0																																
91	P3.1	TxD0	Transmitter data output (asynch.) or clock output (synch.) of serial interface 0																																
92	P3.2	INT0	External interrupt 0 input / timer 0 gate control input																																
93	P3.3	INT1	External interrupt 1 input / timer 1 gate control input																																
94	P3.4	T0	Timer 0 counter input																																
95	P3.5	T1	Timer 1 counter input																																
96	P3.6	WR	WR control output; latches the data byte from port 0 into the external data memory																																
97	P3.7	RD	RD control output; enables the external data memory																																
N.C.	2 - 5, 25, 28, 29, 32, 43, 44, 51 - 53, 74 - 77 88, 89	-	<p>Not connected These pins of the P-MQFP-100 package need not be connected.</p>																																

*) I = Input
O = Output

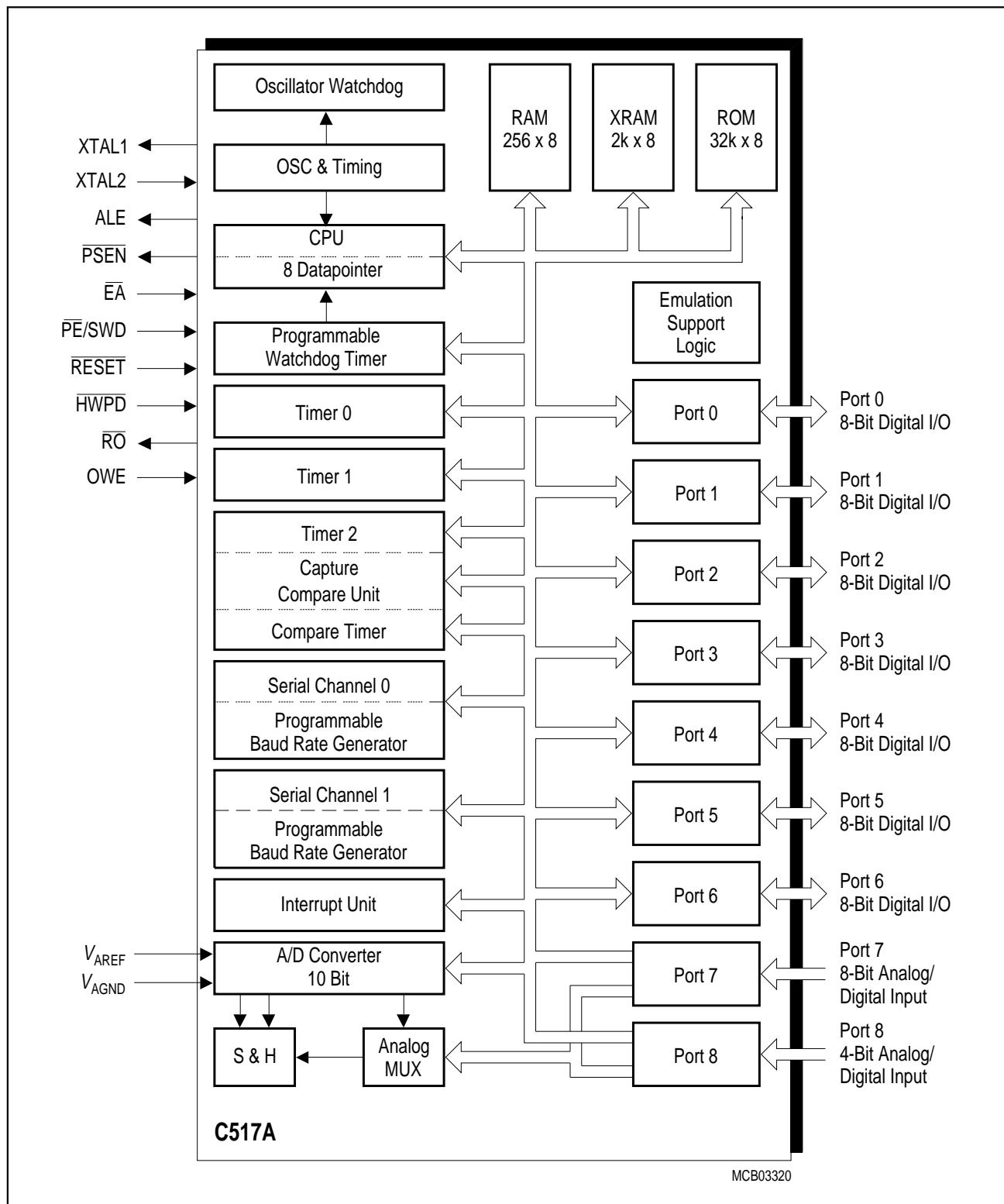


Figure 4
Block Diagram of the C517A

CPU

The C517A is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions are executed in 1 μ s (24 MHz: 500 ns).

Special Function Register PSW (Address D0H)

Reset Value : 00H

Bit No.	MSB	LSB							
	D7H	D6H	D5H	D4H	D3H	D2H	D1H	D0H	
D0H	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function		
CY	Carry Flag Used by arithmetic instruction.		
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.		
F0	General Purpose Flag		
RS1	Register Bank select control bits These bits are used to select one of the four register banks.		
	RS1	RS0	Function
	0	0	Bank 0 selected, data address 00H-07H
	0	1	Bank 1 selected, data address 08H-0FH
	1	0	Bank 2 selected, data address 10H-17H
	1	1	Bank 3 selected, data address 18H-1FH
OV	Overflow Flag Used by arithmetic instruction.		
F1	General Purpose Flag		
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.		

Memory Organization

The C517A CPU manipulates operands in the following five address spaces:

- up to 64 Kbyte of program memory (32K on-chip program memory for C517A-4R)
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- 2K bytes of internal XRAM data memory
- a 128 byte special function register area

Figure 5 illustrates the memory address spaces of the C517A.

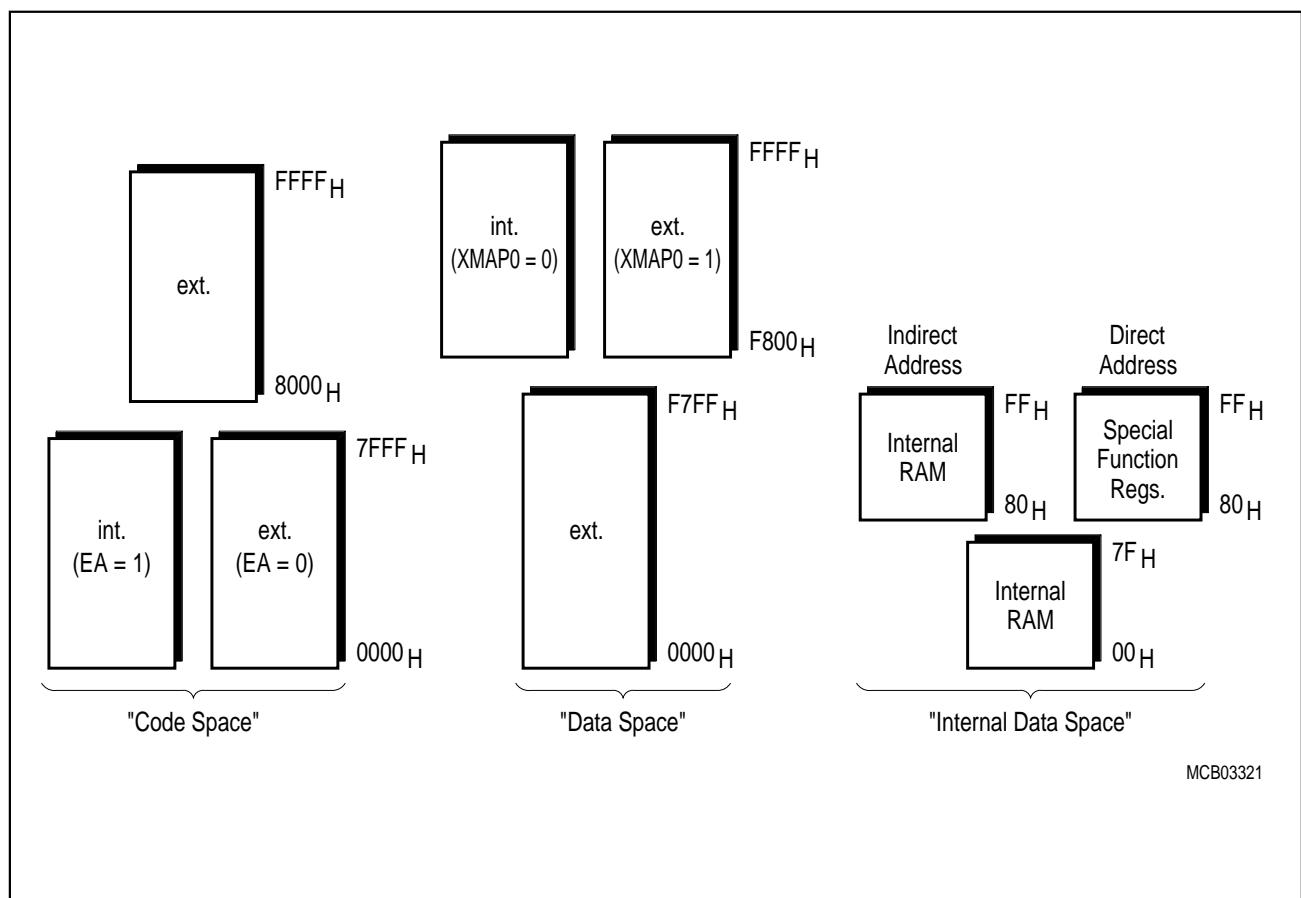


Figure 5
C517A Memory Map

Reset and System Clock

The reset input is an active low input at pin RESET. Since the reset is synchronized internally, the RESET pin must be held low for at least two machine cycles (24 oscillator periods) while the oscillator is running. A pullup resistor is internally connected to V_{CC} to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when V_{CC} is applied by connecting the RESET pin to V_{SS} via a capacitor. **Figure 6** shows the possible reset circuitries.

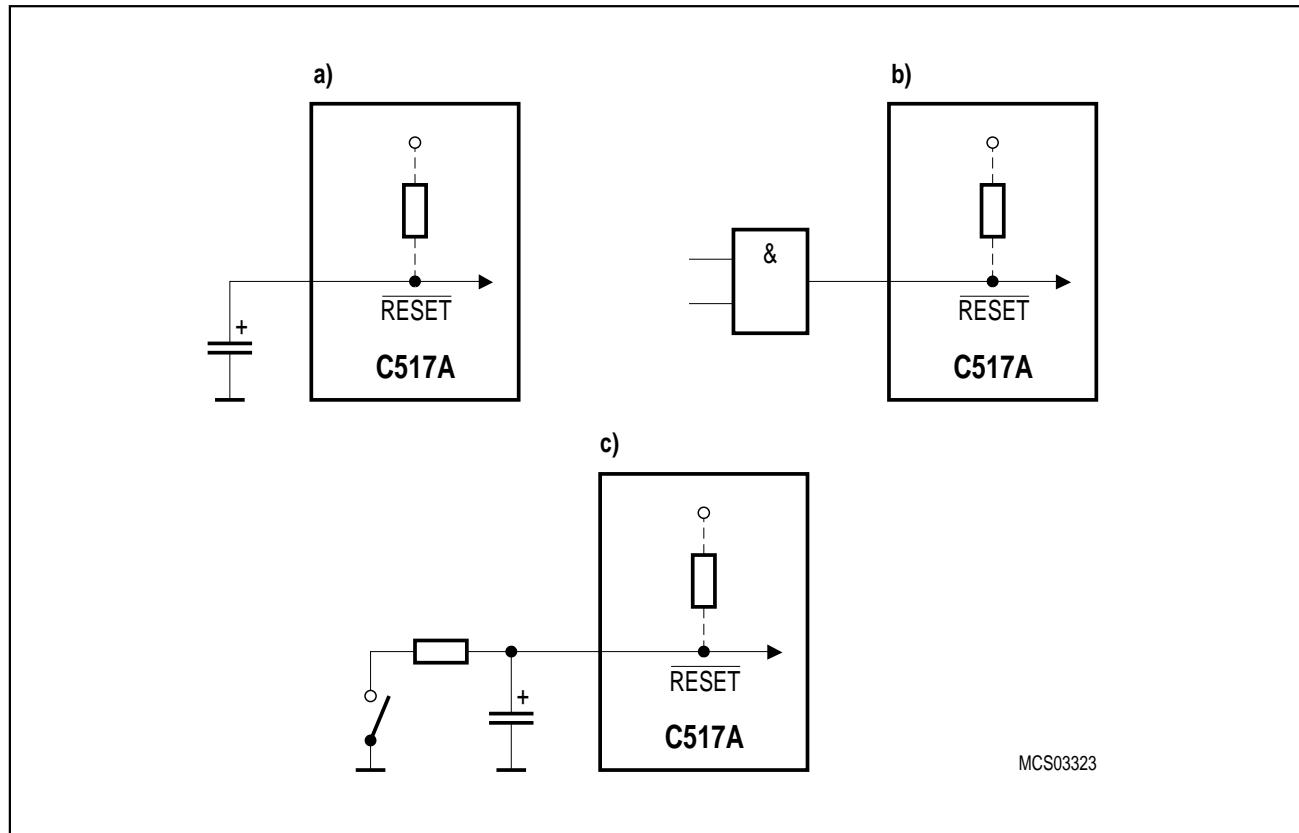
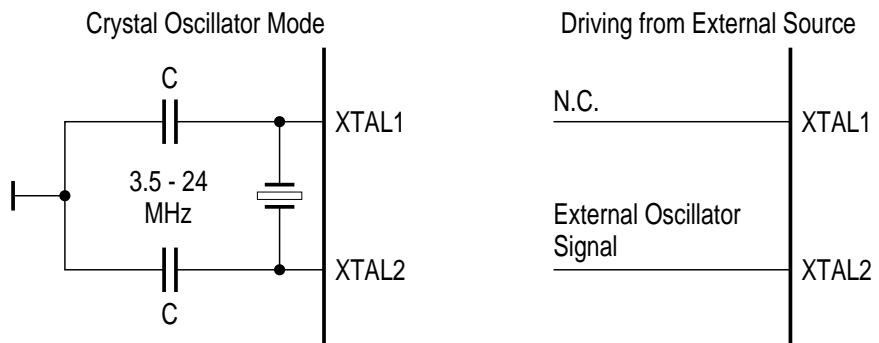


Figure 6
Reset Circuitries

Figure 7 shows the recommended oscillator circuitries for crystal and external clock operation.



MCS03245

Figure 7
Recommended Oscillator Circuitries

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the support of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology^{TM 1)}, which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

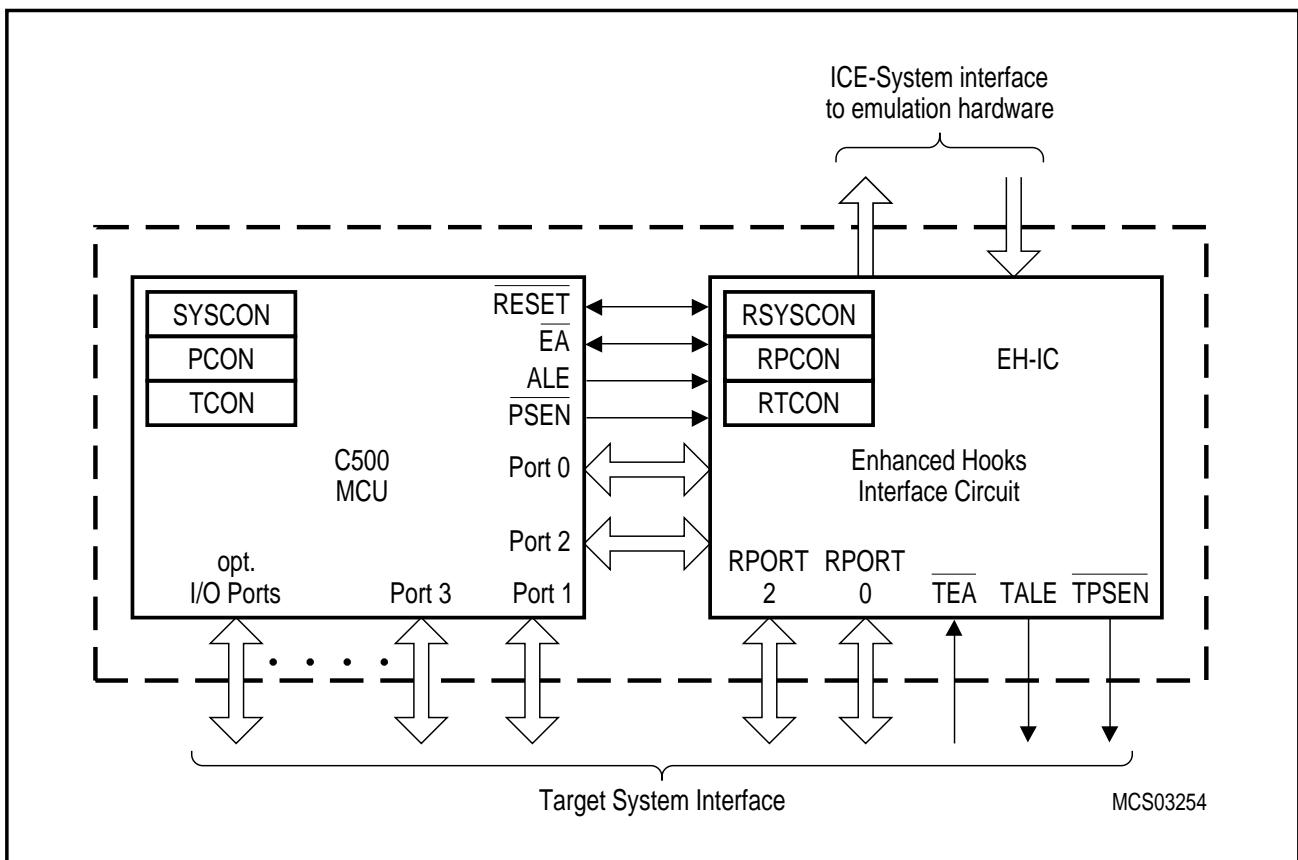


Figure 8
Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the program execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

1 "Enhanced Hooks Technology" is a trademark and patent of Metalink Corporation licensed to Siemens.

Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 94 special function registers (SFRs) in the standard and mapped SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. All SFRs with addresses where address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, 98_H, ..., F8_H, FF_H) are bitaddressable. The SFRs of the C517A are listed in **table 3** and **table 4**. In **table 3** they are organized in groups which refer to the functional blocks of the C517A. **Table 4** illustrates the contents of the SFRs in numeric order of their addresses.

Table 3
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	E0H ¹⁾	00H
	B	B-Register	F0H ¹⁾	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	DPSEL	Data Pointer Select Register	92H	XXXX X000 _B ³⁾
	PSW	Program Status Word Register	D0H ¹⁾	00H
	SP	Stack Pointer	81H	07H
A/D- Converter	ADCON0 ²⁾	A/D Converter Control Register 0	D8H ¹⁾	00H
	ADCON1	A/D Converter Control Register 1	DC _H	0XXX 0000 _B ³⁾
	ADDATH	A/D Converter Data Register, High Byte	D9H	00H
	ADDATL	A/D Converter Data Register, Low Byte	DAH	00XX XXXX _B ³⁾
Interrupt System	IEN0 ²⁾	Interrupt Enable Register 0	A8H ¹⁾	00H
	IEN1 ²⁾	Interrupt Enable Register 1	B8H ¹⁾	00H
	IEN2	Interrupt Enable Register 2	9AH	XX00 00X0 _B ³⁾
	IPO ²⁾	Interrupt Priority Register 0	A9H	00H
	IP1	Interrupt Priority Register 1	B9H	XX00 0000 _B ³⁾
	IRCON0 ²⁾	Interrupt Request Control Register 0	C0H ¹⁾	00H
	IRCON1	Interrupt Request Control Register 1	D1H	00H
	TCON ²⁾	Timer 0/1 Control Register	88H ¹⁾	00H
	T2CON ²⁾	Timer 2 Control Register	C8H ¹⁾	00H
	S0CON ²⁾	Serial Channel 0 Control Register	98H ¹⁾	00H
	CTCON ²⁾	Compare Timer Control Register	E1H	0X00 0000 _B ³⁾
	ARCON	Arithmetic Control Register	EF _H	XXXXXXXX _B ³⁾
MUL/DIV Unit	MD0	Multiplication/Division Register 0	E9H	XX _H ³⁾
	MD1	Multiplication/Division Register 1	EAH	XX _H ³⁾
	MD2	Multiplication/Division Register 2	EBH	XX _H ³⁾
	MD3	Multiplication/Division Register 3	EC _H	XX _H ³⁾
	MD4	Multiplication/Division Register 4	EDH	XX _H ³⁾
	MD5	Multiplication/Division Register 5	EEH	XX _H ³⁾
Timer 0 / Timer 1	TCON ²⁾	Timer 0/1 Control Register	88H ¹⁾	00H
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) 'X' means that the value is undefined and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Compare/	CCEN	Compare/Capture Enable Register	C1H	00H
Capture	CC4EN	Compare/Capture 4 Enable Register	C9H	00H
Unit	CCH1	Compare/Capture Register 1, High Byte	C3H	00H
(CCU)	CCH2	Compare/Capture Register 2, High Byte	C5H	00H
Timer 2	CCH3	Compare/Capture Register 3, High Byte	C7H	00H
	CCH4	Compare/Capture Register 4, High Byte	CFH	00H
	CCL1	Compare/Capture Register 1, Low Byte	C2H	00H
	CCL2	Compare/Capture Register 2, Low Byte	C4H	00H
	CCL3	Compare/Capture Register 3, Low Byte	C6H	00H
	CCL4	Compare/Capture Register 4, Low Byte	CEH	00H
	CMEN	Compare Enable Register	F6H	00H
	CMH0	Compare Register 0, High Byte	D3H	00H
	CMH1	Compare Register 1, High Byte	D5H	00H
	CMH2	Compare Register 2, High Byte	D7H	00H
	CMH3	Compare Register 3, High Byte	E3H	00H
	CMH4	Compare Register 4, High Byte	E5H	00H
	CMH5	Compare Register 5, High Byte	E7H	00H
	CMH6	Compare Register 6, High Byte	F3H	00H
	CMH7	Compare Register 7, High Byte	F5H	00H
	CML0	Compare Register 0, Low Byte	D2H	00H
	CML1	Compare Register 1, Low Byte	D4H	00H
	CML2	Compare Register 2, Low Byte	D6H	00H
	CML3	Compare Register 3, Low Byte	E2H	00H
	CML4	Compare Register 4, Low Byte	E4H	00H
	CML5	Compare Register 5, Low Byte	E6H	00H
	CML6	Compare Register 6, Low Byte	F2H	00H
	CML7	Compare Register 7, Low Byte	F4H	00H
	CMSEL	Compare Input Select	F7H	00H
	CRCH	Comp./Rel./Capt. Register High Byte	CBH	00H
	CRCL	Comp./Rel./Capt. Register Low Byte	CAH	00H
	COMSETL	Compare Set Register Low Byte	A1H	00H
	COMSETH	Compare Set Register, High Byte	A2H	00H
	COMCLRL	Compare Clear Register, Low Byte	A3H	00H
	COMCLRH	Compare Clear Register, High Byte	A4H	00H
	SETMSK	Compare Set Mask Register	A5H	00H
	CLRMSK	Compare Clear Mask Register	A6H	00H
	CTCON ²⁾	Compare Timer Control Register	E1H	0X00 0000 _B ³⁾
	CTRELH	Compare Timer Rel. Register, High Byte	DFH	00H
	CTRELL	Compare Timer Rel. Register, Low Byte	DEH	00H
	TH2	Timer 2, High Byte	CDH	00H
	TL2	Timer 2, Low Byte	CCH	00H
	T2CON ²⁾	Timer 2 Control Register	C8H ¹⁾	00H
	IRCON0 ²⁾	Interrupt Request Control Register 0	C0H ¹⁾	00H

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) 'X' means that the value is undefined and the location is reserved

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	80H ¹⁾	FFH
	P1	Port 1	90H ¹⁾	FFH
	P2	Port 2	A0H ¹⁾	FFH
	P3	Port 3	B0H ¹⁾	FFH
	P4	Port 4	E8H ¹⁾	FFH
	P5	Port 5	F8H ¹⁾	FFH
	P6	Port 6	FAH	FFH
	P7	Port 7, Analog/Digital Input	DBH	-
	P8	Port 8, Analog/Digital Input, 4-bit	DDH	-
XRAM	XPAGE	Page Address Register for Extended On-Chip RAM	91H	00H
	SYSCON ²⁾	System/XRAM Control Register	B1H	XXXX XX01B ³⁾
Serial Channels	ADCON0 ²⁾	A/D Converter Control Register	D8H ¹⁾	00H
	PCON ²⁾	Power Control Register	87H	00H
	S0BUF	Serial Channel 0 Buffer Register	99H	XXH ³⁾
	S0CON	Serial Channel 0 Control Register	98H ¹⁾	00H
	S0RELL	Serial Channel 0 Reload Reg., Low Byte	AAH	D9H
	S0RELH	Serial Channel 0 Reload Reg., High Byte	BAH	XXXX XX11B ³⁾
	S1BUF	Serial Channel 1 Buffer Register	9CH	XXH ³⁾
	S1CON	Serial Channel 1 Control Register	9BH	0X00 0000B ³⁾
	S1RELL	Serial Channel 1 Reload Reg., Low Byte	9DH	00H
	S1RELH	Serial Channel 1 Reload Reg., High Byte	BBH	XXXX XX11B ³⁾
Watchdog	IENO ²⁾	Interrupt Enable Register 0	A8H ¹⁾	00H
	IEN1 ²⁾	Interrupt Enable Register 1	B8H ¹⁾	00H
	IP0 ²⁾	Interrupt Priority Register 0	A9H	00H
	WDTREL	Watchdog Timer Reload Register	86H	00H
Pow. Sav. Modes	PCON ²⁾	Power Control Register	87H	00H

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) 'X' means that the value is undefined and the location is reserved.

Table 4
Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset ¹⁾	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80 _H ²⁾	P0	FF _H	.7	.6	.5	.4	.3	.2	.1	.0
81 _H	SP	07 _H	.7	.6	.5	.4	.3	.2	.1	.0
82 _H	DPL	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
83 _H	DPH	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
83 _H	WDTREL	00 _H	WDT- PSEL	.6	.5	.4	.3	.2	.1	.0
87 _H	PCON	00 _H	SMOD	PDS	IDLS	SD	GF1	GF0	PDE	IDLE
88 _H ²⁾	TCON	00 _H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89 _H	TMOD	00 _H	GATE	C/̄T	M1	M0	GATE	C/̄T	M1	M0
8A _H	TL0	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
8B _H	TL1	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
8C _H	TH0	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
8D _H	TH1	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
90 _H ²⁾	P1	FF _H	T2	CLK- OUT	T2EX	INT2	INT6	INT5	INT4	INT3
91 _H	XPAGE	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
92 _H	DPSEL	XXXX- X000 _B	—	—	—	—	—	.2	.1	.0
98 _H ²⁾	S0CON	00 _H	SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0
99 _H	S0BUF	XX _H	.7	.6	.5	.4	.3	.2	.1	.0
9A _H	IEN2	XX00- 00X0 _B	—	—	ECR	ECS	ECT	ECMP	—	ES1
9B _H	S1CON	0X00- 0000 _B	SM	—	SM21	REN1	TB81	RB81	TI1	RI1
9C _H	S1BUF	XX _H	.7	.6	.5	.4	.3	.2	.1	.0
9D _H	S1RELL	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
A0 _H ²⁾	P2	FF _H	.7	.6	.5	.4	.3	.2	.1	.0
A1 _H	COMSETL	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
A2 _H	COMSETH	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
A3 _H	COMCLRL	00 _H	.7	.6	.5	.4	.3	.2	.1	.0

1) 'X' means that the value is undefined and the location is reserved

2) Shaded registers are bit-addressable special function registers

Table 4

Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset ¹⁾	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A4H	COMCLRH	00H	.7	.6	.5	.4	.3	.2	.1	.0
A5H	SETMSK	00H	.7	.6	.5	.4	.3	.2	.1	.0
A6H	CLRMSK	00H	.7	.6	.5	.4	.3	.2	.1	.0
A8H ²⁾	IEN0	00H	EAL	WDT	ET2	ES0	ET1	EX1	ET0	EX0
A9H	IP0	00H	OWDS	WDTS	.5	.4	.3	.2	.1	.0
AAH	S0RELL	D9H	.7	.6	.5	.4	.3	.2	.1	.0
B0H ²⁾	P3	FFH	RD	WR	T1	T0	INT1	INT0	TxD0	RxD0
B1H	SYSCON	XXXX-XX01B	—	—	—	—	—	—	XMAP1	XMAP0
B8H ²⁾	IEN1	00H	EXEN2	SWDT	EX6	EX5	EX4	EX3	EX2	EADC
B9H	IP1	XX00-0000B	—	—	.5	.4	.3	.2	.1	.0
BAH	S0RELH	XXXX-XX11B	—	—	—	—	—	—	.1	.0
BBH	S1RELH	XXXX-XX11B	—	—	—	—	—	—	.1	.0
C0H ²⁾	IRCON0	00H	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	IEX2	IADC
C1H	CCEN	00H	COCA H3	COCAL 3	COCA H2	COCAL 2	COCA H1	COCAL 1	COCA H0	COCA L0
C2H	CCL1	00H	.7	.6	.5	.4	.3	.2	.1	.0
C3H	CCH1	00H	.7	.6	.5	.4	.3	.2	.1	.0
C4H	CCL2	00H	.7	.6	.5	.4	.3	.2	.1	.0
C5H	CCH2	00H	.7	.6	.5	.4	.3	.2	.1	.0
C6H	CCL3	00H	.7	.6	.5	.4	.3	.2	.1	.0
C7H	CCH3	00H	.7	.6	.5	.4	.3	.2	.1	.0
C8H ²⁾	T2CON	00H	T2PS	I3FR	I2FR	T2R1	T2R0	T2CM	T2I1	T2I0
C9H	CC4EN	00H	COCO EN1	COCO N2	COCO N1	COCO N0	COCO EN0	COCA H4	COCA L4	COMO

1) 'X' means that the value is undefined and the location is reserved

2) Shaded registers are bit-addressable special function registers

Table 4

Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset ¹⁾	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CA _H	CRCL	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
CB _H	CRCH	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
CC _H	TL2	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
CD _H	TH2	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
CE _H	CCL4	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
CF _H	CCH4	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
D0 _H ²⁾	PSW	00 _H	CY	AC	F0	RS1	RS0	OV	F1	P
D1 _H	IRCON1	00 _H	ICMP7	ICMP6	ICMP5	ICMP4	ICMP3	ICMP2	ICMP1	ICMP0
D2 _H	CML0	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
D3 _H	CMH0	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
D4 _H	CML1	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
D5 _H	CMH1	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
D6 _H	CML2	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
D7 _H	CMH2	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
D8 _H ²⁾	ADCON0	00 _H	BD	CLK	ADEX	BSY	ADM	MX2	MX1	MX0
D9 _H	ADDATH	00 _H	.9	.8	.7	.6	.5	.4	.3	.2
DA _H	ADDATL	00XX-XXXX _B	.1	.0	—	—	—	—	—	—
DB _H	P7	—	.7	.6	.5	.4	.3	.2	.1	.0
DC _H	ADCON1	0XXX-0000 _B	ADCL	—	—	—	MX3	MX2	MX1	MX0
DD _H	P8	—	—	—	—	—	.3	.2	.1	.0
DE _H	CTRELL	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
DF _H	CTRELLH	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
E0 _H ²⁾	ACC	00 _H	.7	.6	.5	.4	.3	.2	.1	.0
E1 _H	CTCON	0X00.0000 _B	T2PS1	—	ICR	ICS	CTF	CLK2	CLK1	CLK0
E2 _H	CML3	00 _H	.7	.6	.5	.4	.3	.2	.1	.0

1) 'X' means that the value is undefined and the location is reserved

2) Shaded registers are bit-addressable special function registers

Table 4
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset ¹⁾	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E3H	CMH3	00H	.7	.6	.5	.4	.3	.2	.1	.0
E4H	CML4	00H	.7	.6	.5	.4	.3	.2	.1	.0
E5H	CMH4	00H	.7	.6	.5	.4	.3	.2	.1	.0
E6H	CML5	00H	.7	.6	.5	.4	.3	.2	.1	.0
E7H	CMH5	00H	.7	.6	.5	.4	.3	.2	.1	.0
E8H ²⁾	P4	FFH	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
E9H	MD0	XXH	.7	.6	.5	.4	.3	.2	.1	.0
EAH	MD1	XXH	.7	.6	.5	.4	.3	.2	.1	.0
EBH	MD2	XXH	.7	.6	.5	.4	.3	.2	.1	.0
ECH	MD3	XXH	.7	.6	.5	.4	.3	.2	.1	.0
EDH	MD4	XXH	.7	.6	.5	.4	.3	.2	.1	.0
EEH	MD5	XXH	.7	.6	.5	.4	.3	.2	.1	.0
EFH	ARCON	0XXX. XXXXB	MDEF	MDOV	SLR	SC.4	SC.3	SC.2	SC.1	SC.0
F0H ²⁾	B	00H	.7	.6	.5	.4	.3	.2	.1	.0
F2H	CML6	00H	.7	.6	.5	.4	.3	.2	.1	.0
F3H	CMH6	00H	.7	.6	.5	.4	.3	.2	.1	.0
F4H	CML7	00H	.7	.6	.5	.4	.3	.2	.1	.0
F5H	CMH7	00H	.7	.6	.5	.4	.3	.2	.1	.0
F6H	CMEN	00H	.7	.6	.5	.4	.3	.2	.1	.0
F7H	CMSEL	00H	.7	.6	.5	.4	.3	.2	.1	.0
F8H ²⁾	P5	FFH	CCM7	CCM6	CCM5	CCM4	CCM3	CCM2	CCM1	CCM0
FAH	P6	FFH	.7	.6	.5	.4	.3	TxD1	RxD1	ADST

1) 'X' means that the value is undefined and the location is reserved

2) Shaded registers are bit-addressable special function registers

Digital I/O Ports

The C517A allows for digital I/O on 56 lines grouped into 7 bidirectional 8-bit ports. Each port bit consists of a latch, an output driver and an input buffer. Read and write accesses to the I/O ports P0 through P6 are performed via their corresponding special function registers P0 to P6.

The output drivers of port 0 and 2 and the input buffers of port 0 are also used for accessing external memory. In this application, port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the port 2 pins continue emitting the P2 SFR contents.

Analog Input Ports

Ports 7 (8-bit) and 8 (4-bit) are input ports only and provide two functions. When used as digital inputs, the corresponding SFR P7 and P8 contains the digital value applied to the port 7/8 lines. When used for analog inputs the desired analog channel is selected by a four-bit field in SFR ADCON1. Of course, it makes no sense to output a value to these input-only ports by writing to the SFR P7 or P8. This will have no effect.

If a digital value is to be read, the voltage levels are to be held within the input voltage specifications (V_{IL}/V_{IH}). Since P7 and P8 are not bit-addressable, all input lines of P7 and P8 are read at the same time by byte instructions.

Nevertheless, it is possible to use port 7 and 8 simultaneously for analog and digital input. However, care must be taken that all bits of P7 and P8 that have an undetermined value caused by their analog function are masked.

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 5**:

Table 5
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD		Input Clock	
		M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	$f_{osc}/12 \times 32$	$f_{osc}/24 \times 32$
1	16-bit timer/counter	1	1		
2	8-bit timer/counter with 8-bit autoreload	1	0		
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	1	1	$f_{osc}/12$	$f_{osc}/24$

In the “timer” function (C/T = ‘0’) the register is incremented every machine cycle. Therefore the count rate is $f_{osc}/12$.

In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{osc}/24$. External inputs INT0 and INT1 (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 9** illustrates the input clock logic.

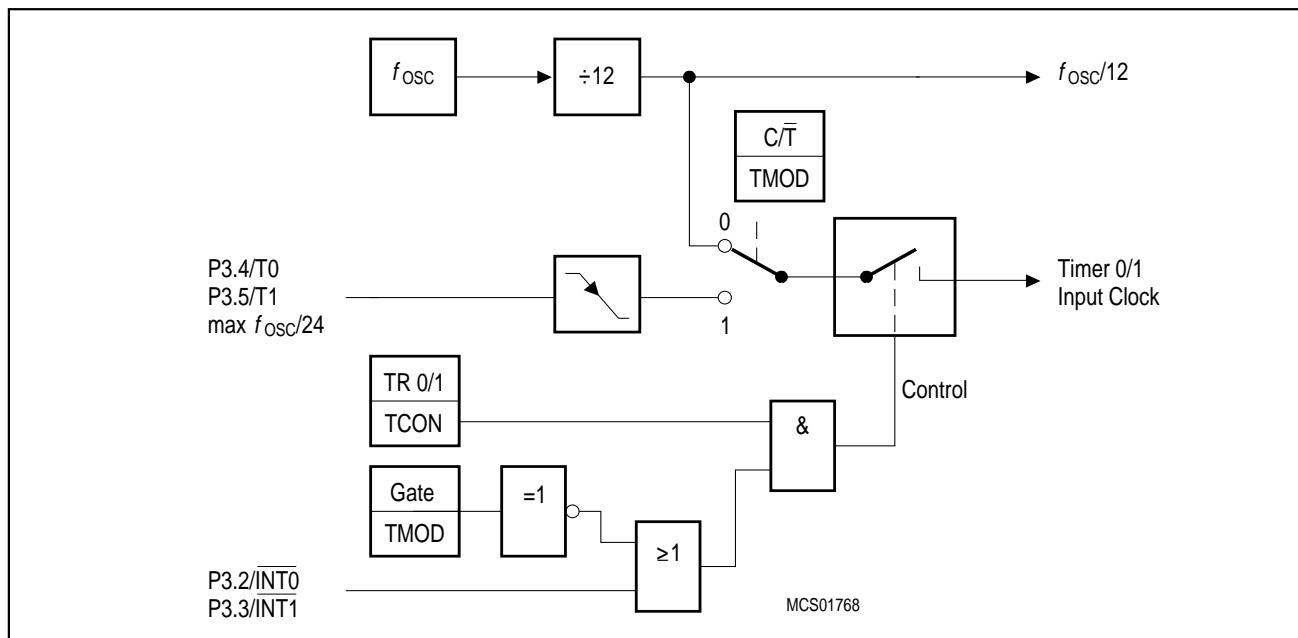


Figure 9
Timer/Counter 0 and 1 Input Clock Logic

Compare / Capture Unit (CCU)

The compare/capture unit is one of the C517A's most powerful peripheral units for use in all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc. The CCU consists of two 16-bit timer/counters with automatic reload feature and an array of 13 compare or compare/capture registers. A set of six control registers is used for flexible adapting of the CCU to a wide variety of user's applications.

The block diagram in **figure 10** shows the general configuration of the CCU. All CC1 to CC4 registers and the CRC register are exclusively assigned to timer 2. Each of the eight compare registers CM0 through CM7 can either be assigned to timer 2 or to the faster compare timer, e.g. to provide up to 8 PWM output channels. The assignment of the CMx registers - which can be done individually for every single register - is combined with an automatic selection of one of the two possible compare modes.

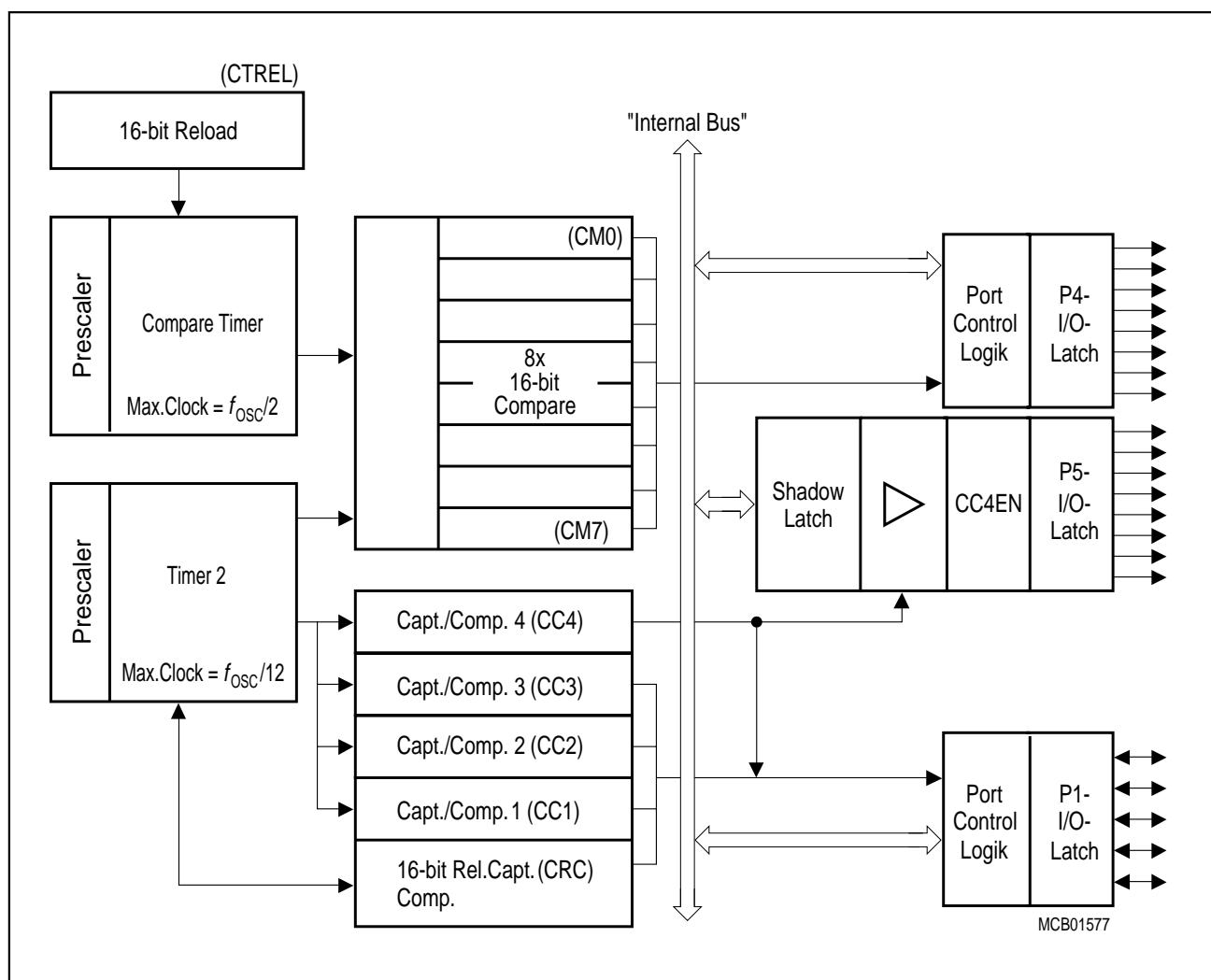


Figure 10
Timer 2 Block Diagram

The main functional blocks of the CCU are:

- Timer 2 with $f_{osc}/12$ input clock, 2-bit prescaler, 16-bit reload, counter/gated timer mode and overflow interrupt request.
- Compare timer with $f_{osc}/2$ input clock, 3-bit prescaler, 16-bit reload and overflow interrupt request.
- Compare/(reload) capture register array consisting of four different kinds of registers:
one 16-bit compare/reload/capture register,
three 16-bit compare/capture registers,
one 16-bit compare/capture register with additional “concurrent compare” feature,
eight 16-bit compare registers with timer-overflow controlled loading.

Table 6 shows the possible configurations of the CCU and the corresponding compare modes which can be selected. The following sections describe the function of these configurations.

Table 6
CCU Configurations

Assigned Timer	Compare Register	Compare Output at	Possible Modes
Timer 2	CRCH/CRCL	P1.0/INT3/CC0	Compare mode 0, 1 + Reload
	CCH1/CCL1	P1.1/INT4/CC1	Compare mode 0, 1 / capture
	CCH2/CCL2	P1.2/INT5/CC2	Compare mode 0, 1 / capture
	CCH3/CCL3	P1.3/INT6/CC3	Compare mode 0, 1 / capture
	CCH4/CCL4	P1.4/INT2/CC4 P5.0/CCM0 to P5.7/CCM7	Compare mode 1 “Concurrent compare”
	CMH0/CML0 to CMH7/CML7	P4.0/CM0 to P4.7/CM7	Compare mode 0
	COMSET COMCLR	P5.0/CCM0 to P5.7/CCM7	Compare mode 2
	CMH0/CML0 to CMH7/CML7	P4.0/CM0 to P4.7/CM7	Compare mode 1

Timer 2 Operation

Timer Mode: In timer function, the count rate is derived from the oscillator frequency. A prescaler offers the possibility of selecting a count rate of 1/12 or 1/24 of the oscillator frequency.

Gated Timer Mode: In gated timer function, the external input pin P1.7/T2 operates as a gate to the input of timer 2. If T2 is high, the internal clock input is gated to the timer. T2 = 0 stops the counting procedure. The external gate signal is sampled once every machine cycle.

Event Counter Mode: In the event counter function, the timer 2 is incremented in response to a 1-to-0 transition at its corresponding external input pin P1.7/T2. In this function, the external input is sampled every machine cycle. The maximum count rate is 1/24 of the oscillator frequency.

Reload of Timer 2: Two reload modes are selectable:

In mode 0, when timer 2 rolls over from all 1's to all 0's, it not only sets TF2 but also causes the timer 2 registers to be loaded with the 16-bit value in the CRC register, which is preset by software. In mode 1, a 16-bit reload from the CRC register is caused by a negative transition at the corresponding input pin P1.5/T2EX.

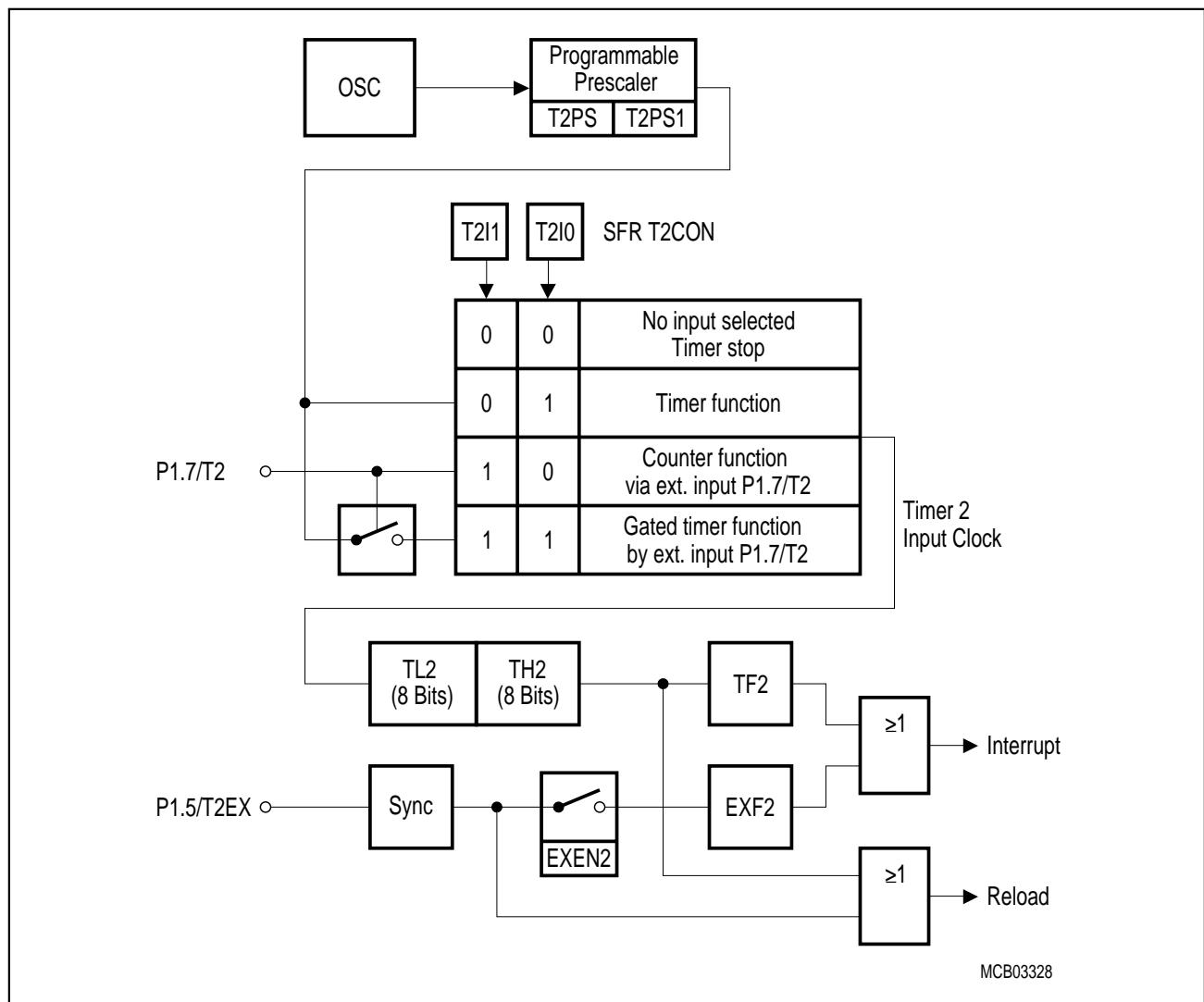


Figure 11
Block Diagram of Timer 2

Compare Timer Operation

The compare timer receives its input clock from a programmable prescaler which provides input frequencies, ranging from $f_{osc}/2$ up to $f_{osc}/256$. The compare timer is, once started, a free-running 16-bit timer, which on overflow is automatically reloaded by the contents of a 16-bit reload register. The compare timer has - as any other timer in the C517A - their own interrupt request flags CTF. These flags are set when the timer count rolls over from all ones to the reload value. **Figure 12** shows the block diagram of compare timer and compare timer 1.

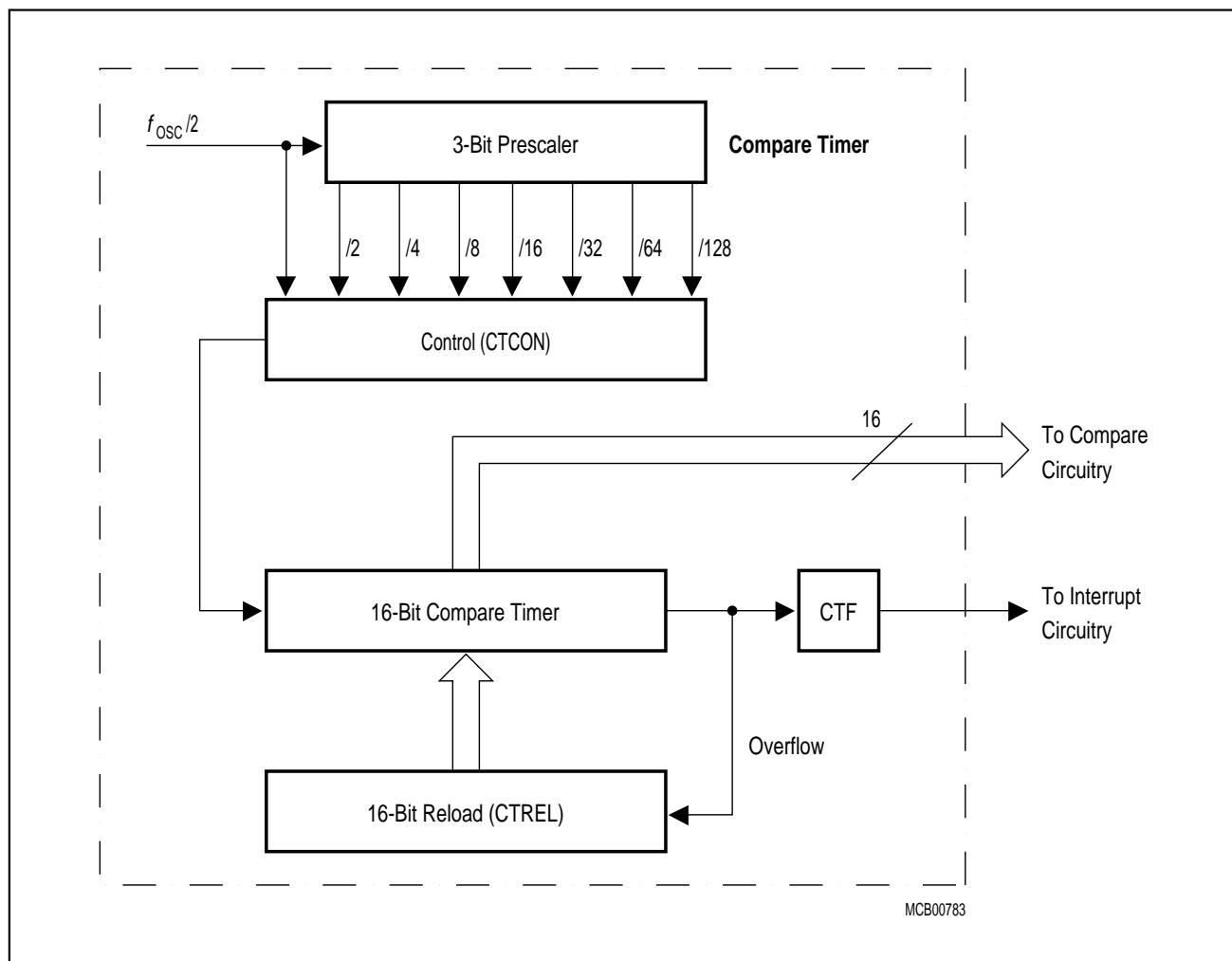


Figure 12
Compare Timer Block Diagram

Compare Modes

The compare function of a timer/register combination operates as follows: the 16-bit value stored in a compare or compare/capture register is compared with the contents of the timer register; if the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin and an interrupt can be generated.

Compare Mode 0

In compare mode 0, upon matching the timer and compare register contents, the output signal changes from low to high. It goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only and writing to the port will have no effect. **Figure 13** shows a functional diagram of a port circuit when used in compare mode 0. The port latch is directly controlled by the timer overflow and compare match signals. The input line from the internal bus and the write-to-latch line of the port latch are disconnected when compare mode 0 is enabled.

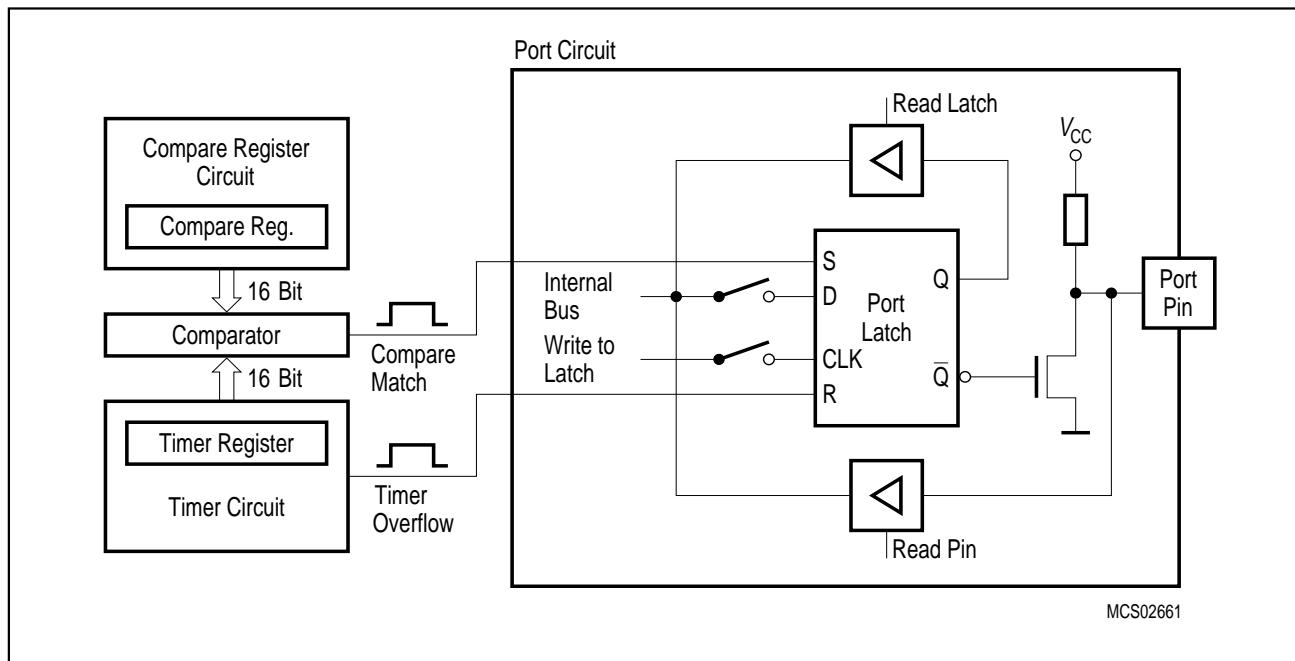


Figure 13
Port Latch in Compare Mode 0

Compare Mode 1

If compare mode 1 is enabled and the software writes to the appropriate output latch at the port, the new value will not appear at the output pin until the next compare match occurs. Thus, it can be chosen whether the output signal has to make a new transition (1-to-0 or 0-to-1, depending on the actual pin-level) or should keep its old value at the time when the timer value matches the stored compare value.

In compare mode 1 (see **figure 14**) the port circuit consists of two separate latches. One latch (which acts as a “shadow latch”) can be written under software control, but its value will only be transferred to the port latch (and thus to the port pin) when a compare match occurs.

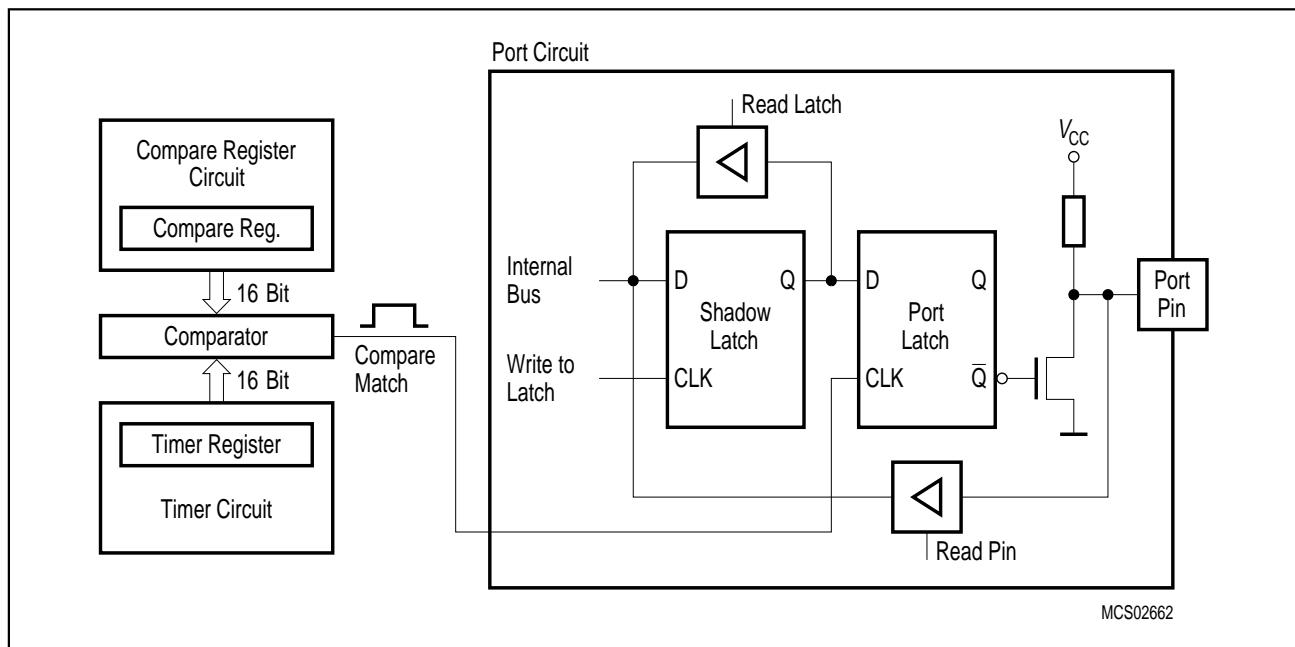


Figure 14
Compare Function in Compare Mode 1

Compare Mode 2

In the compare mode 2 the port 5 pins are under control of compare/capture register CC4, but under control of the compare registers COMSET and COMCLR. When a compare match occurs with register COMSET, a high level appears at the pins of port 5 when the corresponding bits in the mask register SETMSK are set. When a compare match occurs with register COMCLR, a low level appears at the pins of port 5 when the corresponding bits in the mask register CLRMSK are set.

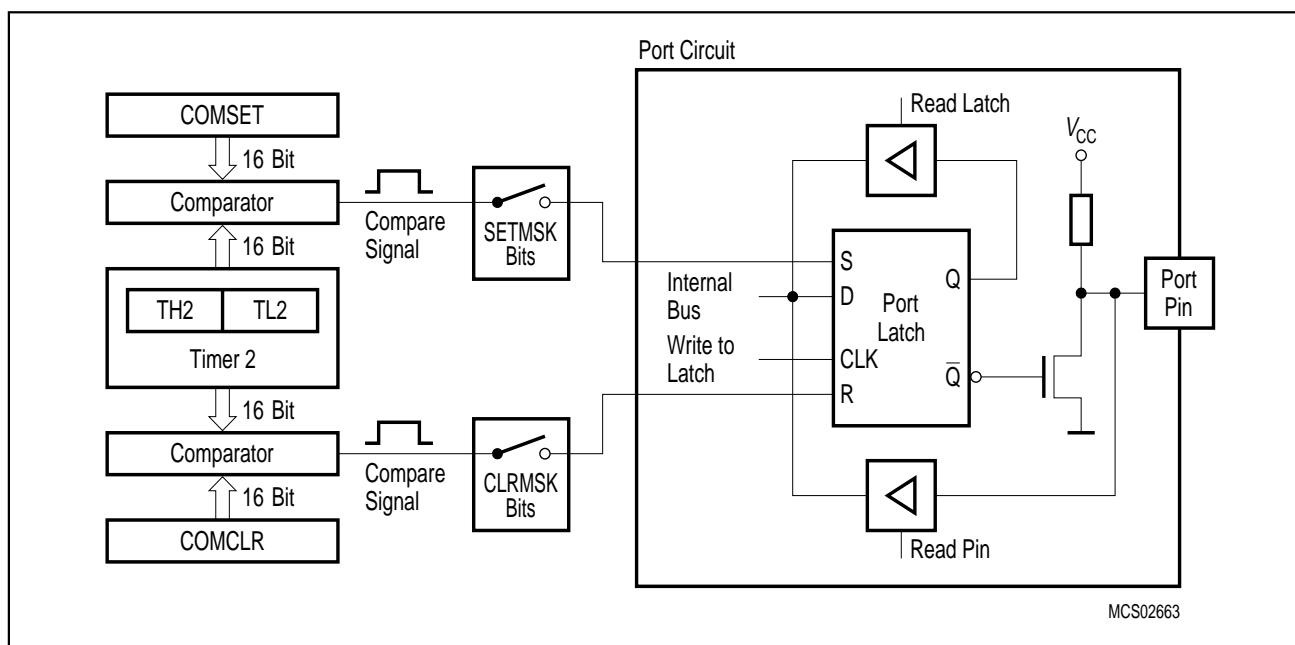


Figure 15
Compare Function of Compare Mode 2

Multiplication / Division Unit (MDU)

This on-chip arithmetic unit of the C517A provides fast 32-bit division, 16-bit multiplication as well as shift and normalize features. All operations are unsigned integer operations. **Table 7** describes the five general operations the MDU is able to perform.

Table 7
MDU Operation Characteristics

Operation	Result	Remainder	Execution Time
32bit/16bit	32bit	16bit	$6 t_{CY}^{1)}$
16bit/16bit	16bit	16bit	$4 t_{CY}^{1)}$
16bit x 16bit	32bit	—	$4 t_{CY}^{1)}$
32-bit normalize	—	—	$6 t_{CY}^{2)}$
32-bit shift L/R	—	—	$6 t_{CY}^{2)}$

1) $1 t_{CY} = 12 t_{CLCL} = 1$ machine cycle = 500 ns at 24 MHz oscillator frequency

2) The maximal shift speed is 6 shifts per machine cycle

The MDU consists of seven special function registers (MD0-MD5, ARCON) which are used as operand, result, and control registers. The three operation phases are shown in **figure 16**.

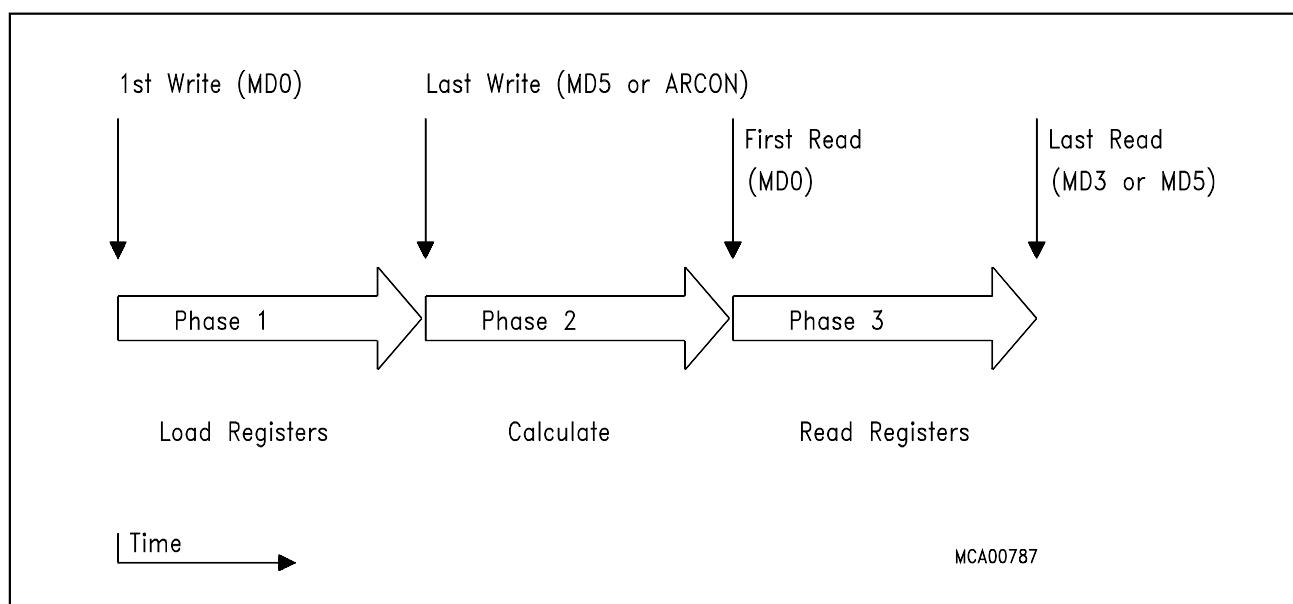


Figure 16
Operating Phases of the MDU

For starting an operation, registers MD0 to MD5 and ARCON must be written to in a certain sequence according **table 8** and **9**. The order the registers are accessed determines the type of the operation. A shift operation is started by a final write operation to SFR ARCON.

Table 8
Programming the MDU for Multiplication and Division

Operation	32Bit/16Bit		16Bit/16Bit		16Bit x 16Bit	
First Write	MD0	D'endL	MD0	D'endL	MD0	M'andL
	MD1	D'end	MD1	D'endH	MD4	M'orL
	MD2	D'end				
	MD3	D'endH	MD4	D'orL	MD1	M'andH
	MD4	D'orL				
Last Write	MD5	D'orH	MD5	D'orH	MD5	M'orH
First Read	MD0	QuoL	MD0	QuoL	MD0	PrL
	MD1	Quo	MD1	QuoH	MD1	
	MD2	Quo				
	MD3	QuoH	MD4	RemL	MD2	
	MD4	RemL				
Last Read	MD5	RemH	MD5	RemH	MD3	PrH

Abbreviations:

D'end : Dividend, 1st operand of division
 D'or : Divisor, 2nd operand of division
 M'and : Multiplicand, 1st operand of multiplication
 M'or : Multiplicator, 2nd operand of multiplication
 Pr : Product, result of multiplication
 Rem : Remainder
 Quo : Quotient, result of division
 ...L : means, that this byte is the least significant of the 16-bit or 32-bit operand
 ...H : means, that this byte is the most significant of the 16-bit or 32-bit operand

Table 9
Programming of the MDU for a Shift or Normalize Operation

Operation	Normalize, Shift Left, Shift Right	
First write	MD0	least significant byte
	MD1	.
	MD2	.
	MD3	most significant byte
Last write	ARCON	start of conversion
First read	MD0	least significant byte
	MD1	.
	MD2	.
Last read	MD3	most significant byte

Serial Interfaces 0 and 1

The C517A has two serial interfaces which are functionally nearly identical concerning the asynchronous modes of operation. The two channels are full-duplex, meaning they can transmit and receive simultaneously. The serial channel 0 is completely compatible with the serial channel of the C501 (one synchronous mode, three asynchronous modes). Serial channel 1 has the same functionality in its asynchronous modes, but the synchronous mode and the fixed baud rate UART mode is missing.

The operating modes of the serial interfaces is illustrated in **table 10**. The possible baudrates can be calculated using the formulas given in **table 11**.

Table 10
Operating Modes of Serial Interface 0 and 1

Serial Interface	Mode	S0CON		S1CON	Description
		SM0	SM1		
0	0	0	0	—	Shift register mode Serial data enters and exits through RxD0; TxD0 outputs the shift clock; 8-bit are transmitted/received (LSB first); fixed baud rate
	1	0	1	—	8-bit UART, variable baud rate 10 bits are transmitted (through TxD0) or received (at RxD0)
	2	1	0	—	9-bit UART, fixed baud rate 11 bits are transmitted (through TxD0) or received (at RxD0)
	3	1	1	—	9-bit UART, variable baud rate Like mode 2
1	A	—	—	0	9-bit UART; variable baud rate 11 bits are transmitted (through TxD1) or received (at RxD1)
	B	—	—	1	8-bit UART; variable baud rate 10 bits are transmitted (through TxD1) or received (at RxD1)

For clarification some terms regarding the difference between "baud rate clock" and "baud rate" should be mentioned. In the asynchronous modes the serial interfaces require a clock rate which is 16 times the baud rate for internal synchronization. Therefore, the baud rate generators/timers have to provide a "baud rate clock" (output signal in **figure 17** and **figure 18**) to the serial interface which - there divided by 16 - results in the actual "baud rate". Further, the abbreviation f_{osc} refers to the oscillator frequency (crystal or external clock operation).

The variable baud rates for modes 1 and 3 of the serial interface 0 can be derived from either timer 1 or a dedicated baud rate generator (see **figure 17**). The variable baud rates for modes A and B of the serial interface 1 are derived from a dedicated baud rate generator as shown in **figure 18**.

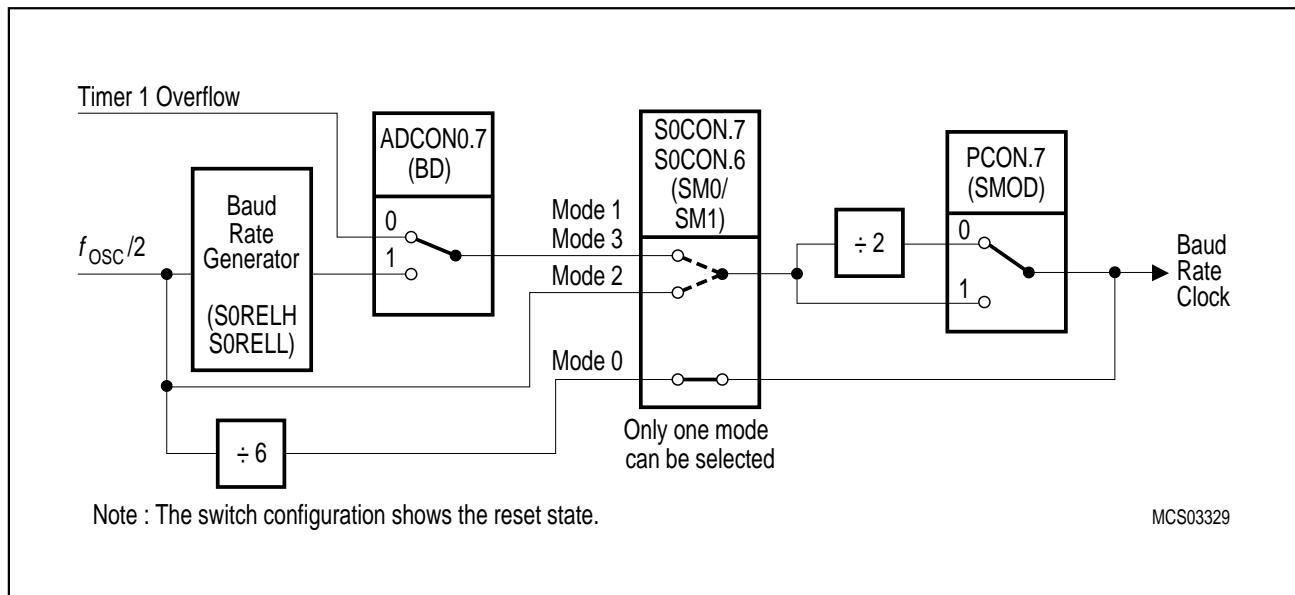


Figure 17
Serial Interface 0 : Baud Rate Generation Configuration

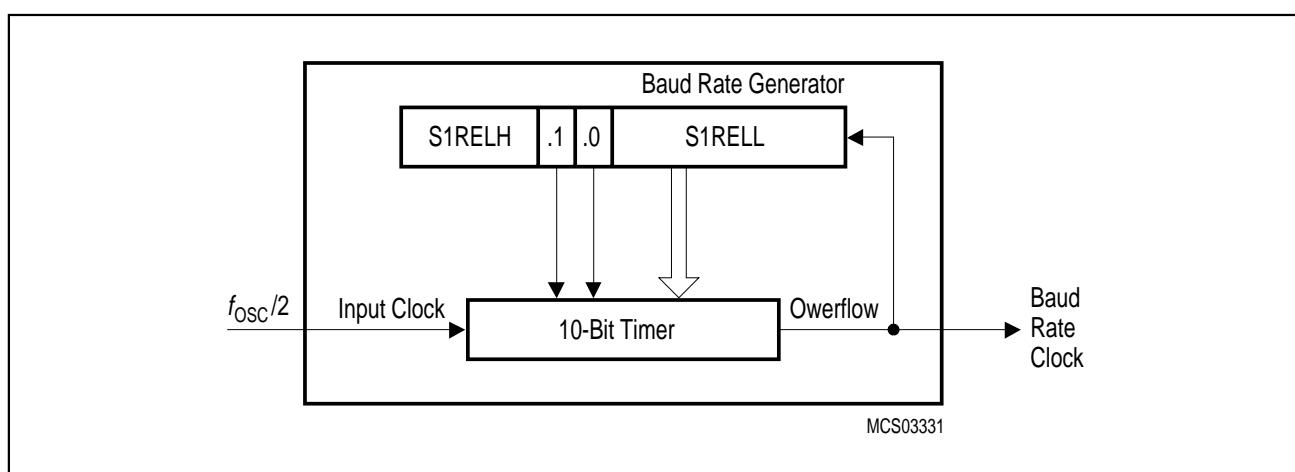


Figure 18
Serial Interface 1 : Baud Rate Generator Configuration

The baud rate generator block in **figure 17** has the same structure (10-bit auto-reload timer) as the baud rate generator block which is shown in detail in **figure 18**.

Table 11 below lists the values/formulas for the baud rate calculation of serial interface 0 and 1 with its dependencies of the control bits BD and SMOD.

Table 11
Serial Interfaces - Baud Rate Dependencies

Serial Interface Operating Modes	Active Control Bits		Baud Rates
	SMOD	BD	
Mode 0 (Shift Register)	–	–	Fixed baud rate clock fosc/12
Mode 1 (8-bit UART) Mode 3 (9-bit UART)	X	0	Timer 1 overflow is used for baud rate generation; SMOD controls a divide-by-2 option. Baud rate = $2^{\text{SMOD}} \times \text{timer 1 overflow rate} / 32$
		1	Baud rate generator is used for baud rate generation; SMOD controls a divide-by-2 option Baud rate = $2^{\text{SMOD}} \times \text{oscillator frequency} / 64 \times (\text{baud rate gen. overflow rate})$
Mode 2 (9-bit UART)	X	–	Fixed baud rate clock fosc/32 (SMOD=1) or fosc/64 (SMOD=0)
Mode A (9-bit UART) Mode B (8-bit UART)	–	–	Baud rate generator is used for baud rate generation; SMOD controls a divide-by-2 option Baud rate = $\text{oscillator frequency} / 32 \times (\text{baud rate gen. overflow rate})$

10-Bit A/D Converter

The C517A provides an A/D converter with the following features:

- 12 multiplexed input channels (port 7, 8), which can also be used as digital inputs
- 10-bit resolution
- Single or continuous conversion mode
- Internal or external start-of-conversion trigger capability
- Interrupt request generation after each conversion
- Using successive approximation conversion technique via a capacitor array
- Built-in hidden calibration of offset and linearity errors

The A/D converter operates with a successive approximation technique and uses self calibration mechanisms for reduction and compensation of offset and linearity errors. The externally applied reference voltage range has to be held on a fixed value within the specifications. The main functional blocks of the A/D converter are shown in **figure 19**.

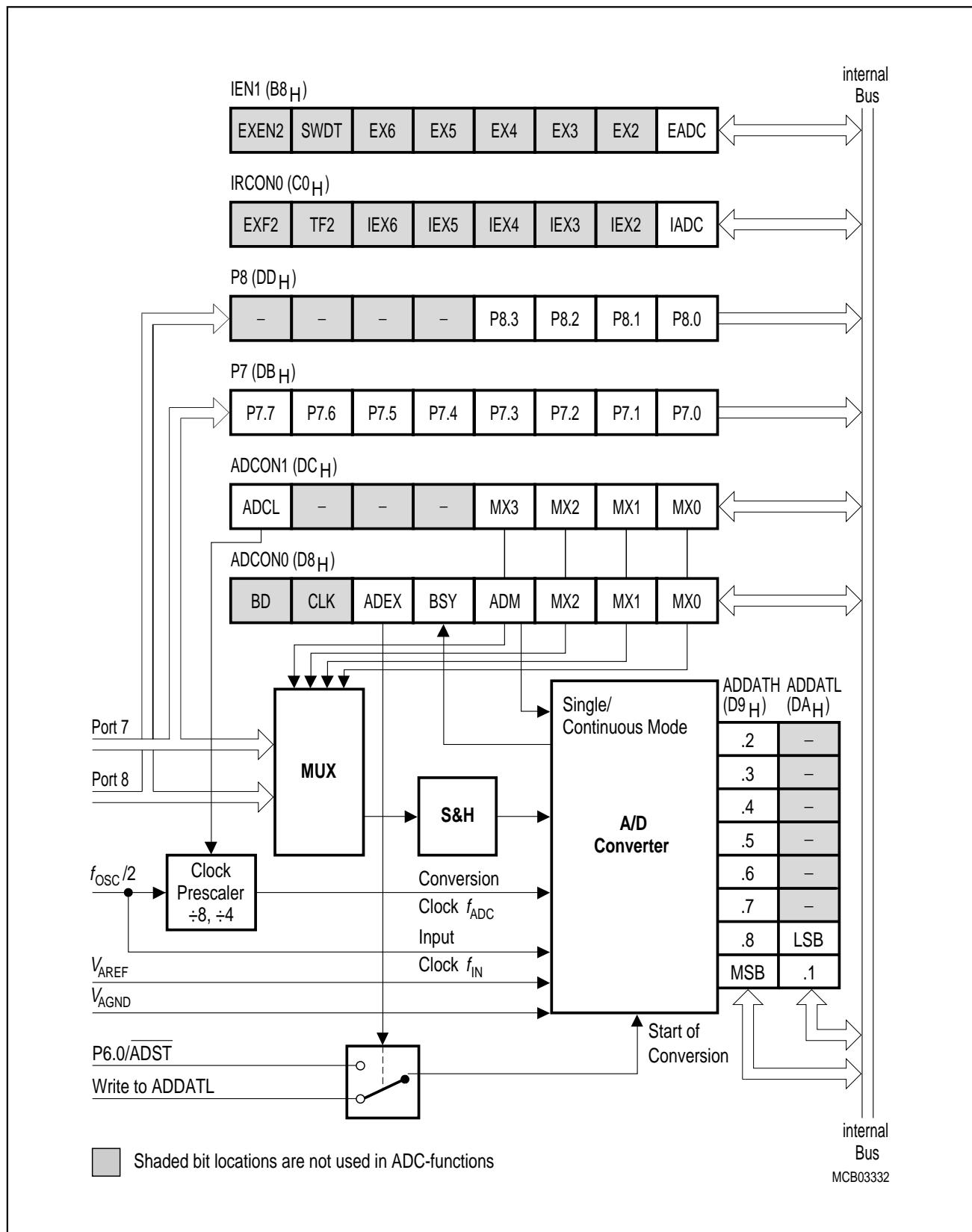


Figure 19
A/D Converter Block Diagram

Interrupt System

The C517A provides 17 interrupt sources with four priority levels. Ten interrupts can be generated by the on-chip peripherals (timer 0, timer 1, timer 2, compare timer, compare match/set/clear, A/D converter, and serial interface 0 and 1) and seven interrupts may be triggered externally (P3.2/INT0, P3.3/INT1, P1.4/INT2, P1.0/INT3, P1.1/INT4, P1.2/INT5, P1.3/INT6).

This chapter shows the interrupt structure, the interrupt vectors and the interrupt related special function registers. **Figure 20** to **22** give a general overview of the interrupt sources and illustrate the request and the control flags which are described in the next sections.

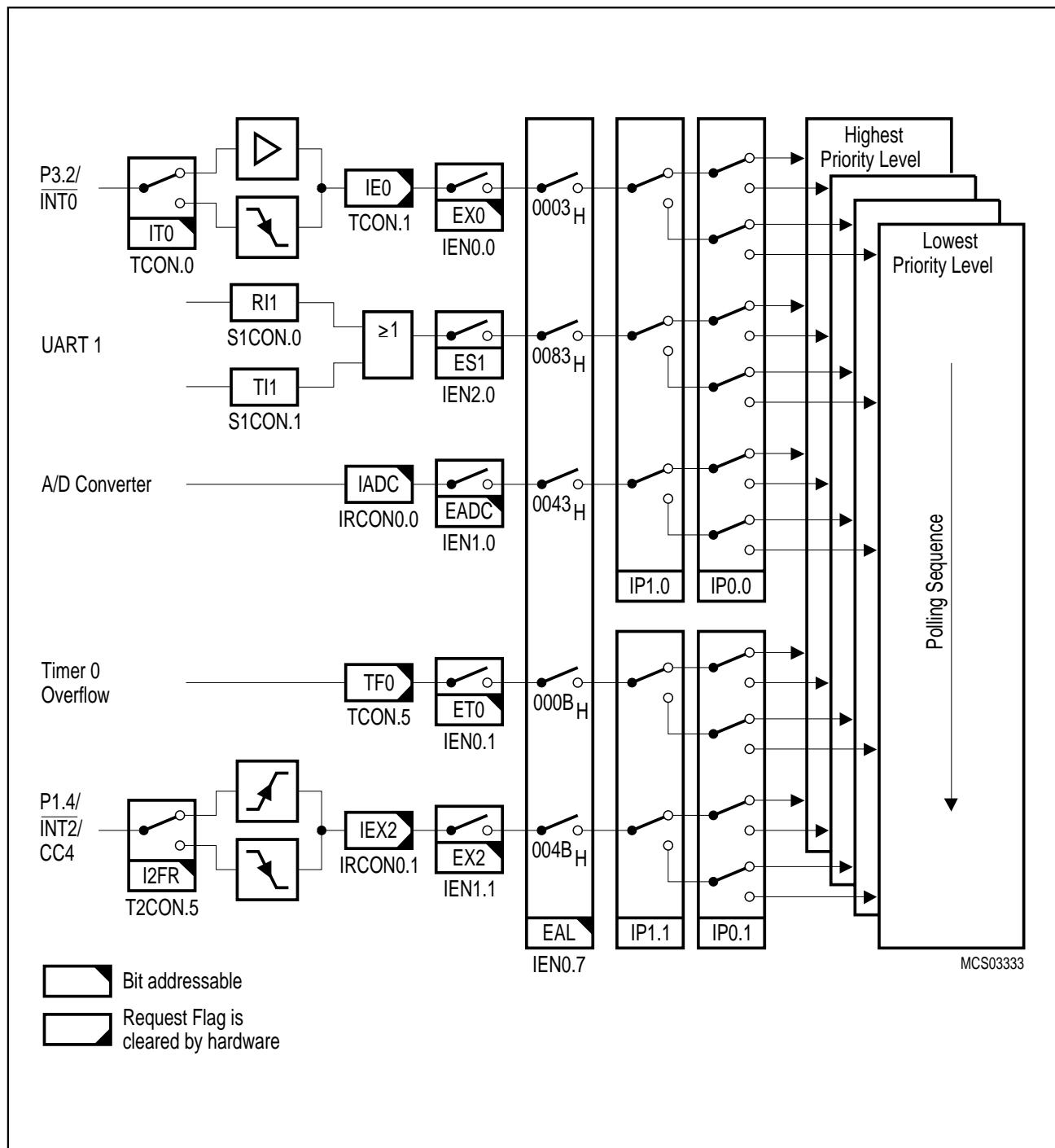


Figure 20
Interrupt Structure, Overview (Part 1)

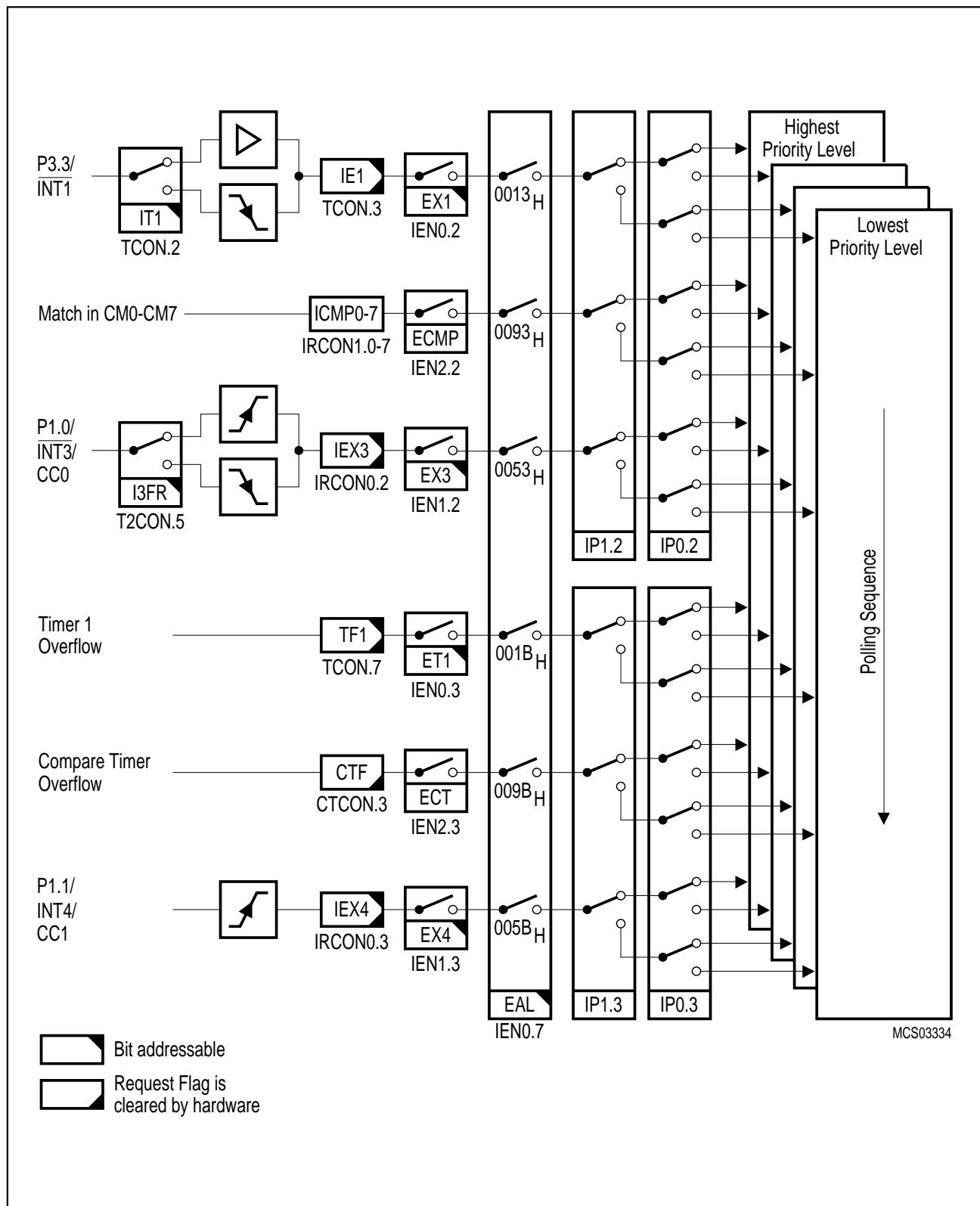


Figure 21
Interrupt Structure, Overview (Part 2)

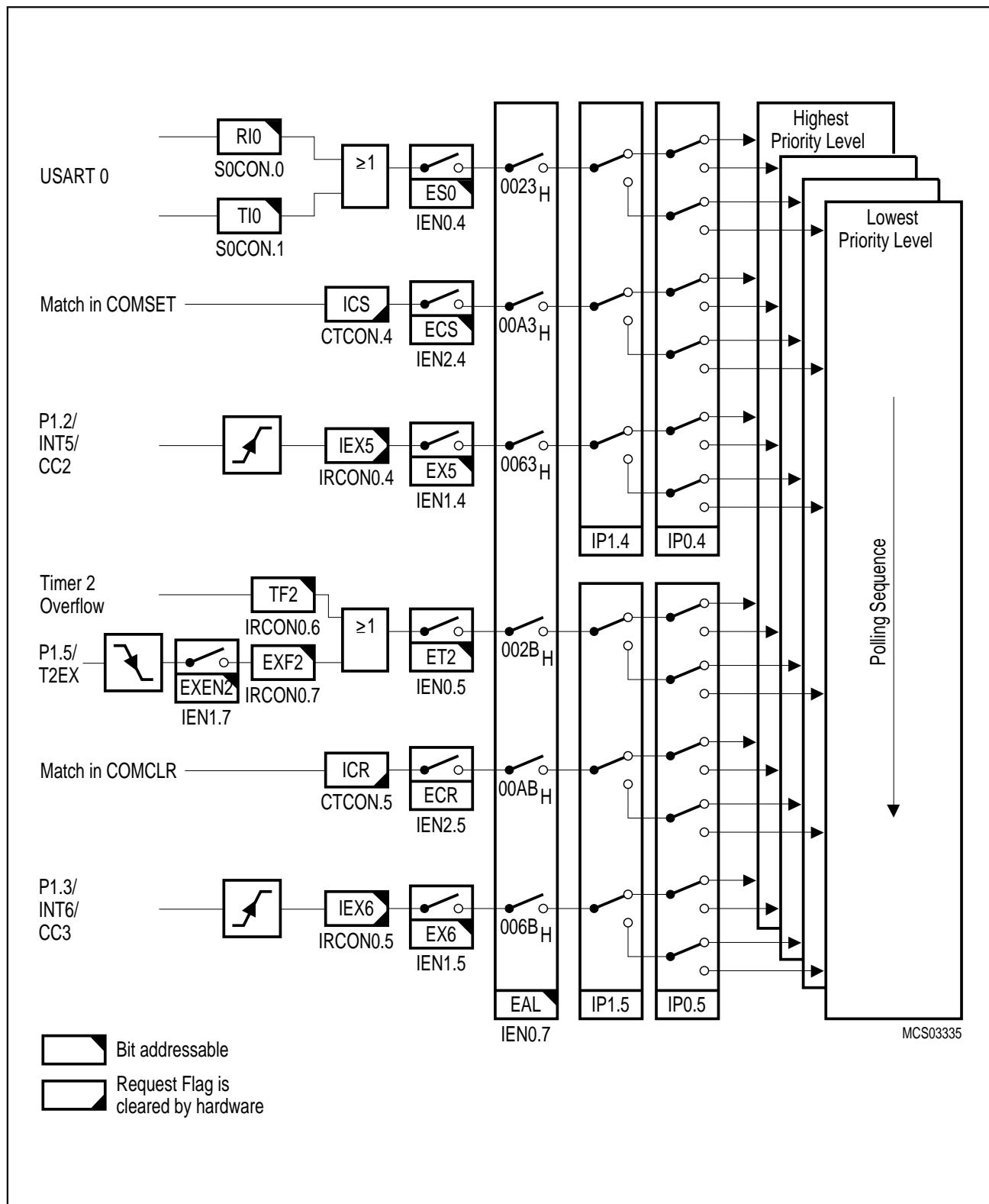


Figure 22
Interrupt Structure, Overview (Part 3)

Table 12
Interrupt Source and Vectors

Interrupt Source	Interrupt Vector Address	Interrupt Request Flags
External Interrupt 0	0003 _H	IE0
Timer 0 Overflow	000B _H	TF0
External Interrupt 1	0013 _H	IE1
Timer 1 Overflow	001B _H	TF1
Serial Channel 0	0023 _H	RI0 / TI0
Timer 2 Overflow / Ext. Reload	002B _H	TF2 / EXF2
A/D Converter	0043 _H	IADC
External Interrupt 2	004B _H	IEX2
External Interrupt 3	0053 _H	IEX3
External Interrupt 4	005B _H	IEX4
External Interrupt 5	0063 _H	IEX5
External Interrupt 6	006B _H	IEX6
Serial Channel 1	0083 _H	RI1 / TI1
Compare Match Interrupt of Compare Registers CM0-CM7 assigned to Timer 2	0093 _H	ICMP0 - ICMP7
Compare Timer Overflow	009B _H	CTF
Compare Match Interrupt of Compare Register COMSET	00A3 _H	ICS
Compare Match Interrupt of Compare Register COMCLR	00AB _H	ICR

Fail Safe Mechanisms

The C517A offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure:

- a programmable watchdog timer (WDT), with variable time-out period from 512 μ s up to approx. 1.1 s at 12 MHz. (256 μ s up to approx. 0.65 s at 24 MHz)
- an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state in case the on-chip oscillator fails; it also provides the clock for a fast internal reset after power-on.

The watchdog timer in the C517A is a 15-bit timer, which is incremented by a count rate of $f_{osc}/24$ up to $f_{osc}/384$. The system clock of the C517A is divided by two prescalers, a divide-by-two and a divide-by-16 prescaler. For programming of the watchdog timer overflow rate, the upper 7 bit of the watchdog timer can be written. **Figure 23** shows the block diagram of the watchdog timer unit.

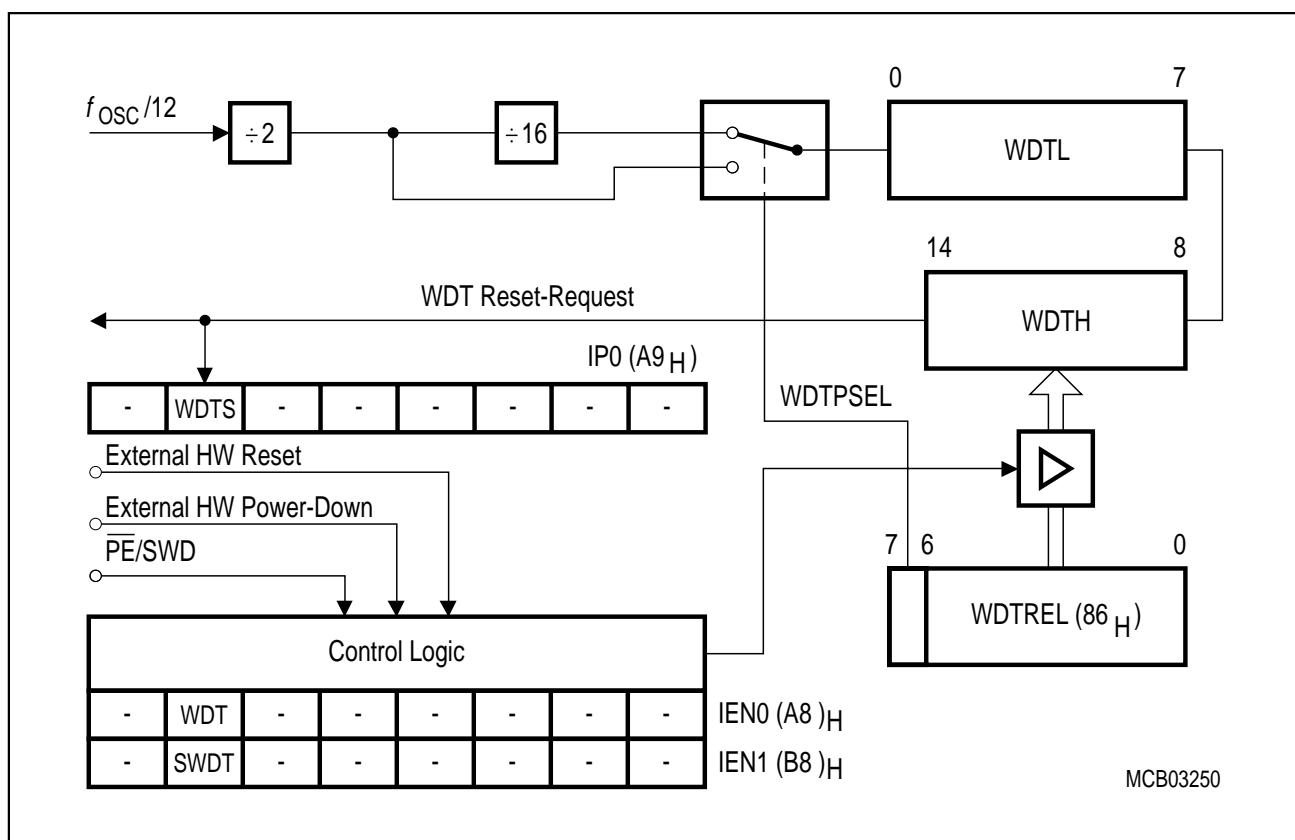


Figure 23
Block Diagram of the Watchdog Timer

The watchdog timer can be started by software (bit SWDT) or by hardware through pin PE/SWD, but it cannot be stopped during active mode of the C517A. If the software fails to refresh the running watchdog timer an internal reset will be initiated on watchdog timer overflow. For refreshing of the watchdog timer the content of the SFR WDTREL is transferred to the upper 7-bit of the watchdog timer. The refresh sequence consists of two consecutive instructions which set the bits WDT and SWDT each. The reset cause (external reset or reset caused by the watchdog) can be examined by software (flag WDTS). It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor.

Oscillator Watchdog

The oscillator watchdog unit serves for four functions:

- **Monitoring of the on-chip oscillator's function**

The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part executes a final reset phase of typ. 1 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.

- **Fast internal reset after power-on**

The oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. The oscillator watchdog unit also works identically to the monitoring function.

- **Restart from the hardware power down mode.**

If the hardware power down mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete hardware power down sequence; however, the watchdog works identically to the monitoring function.

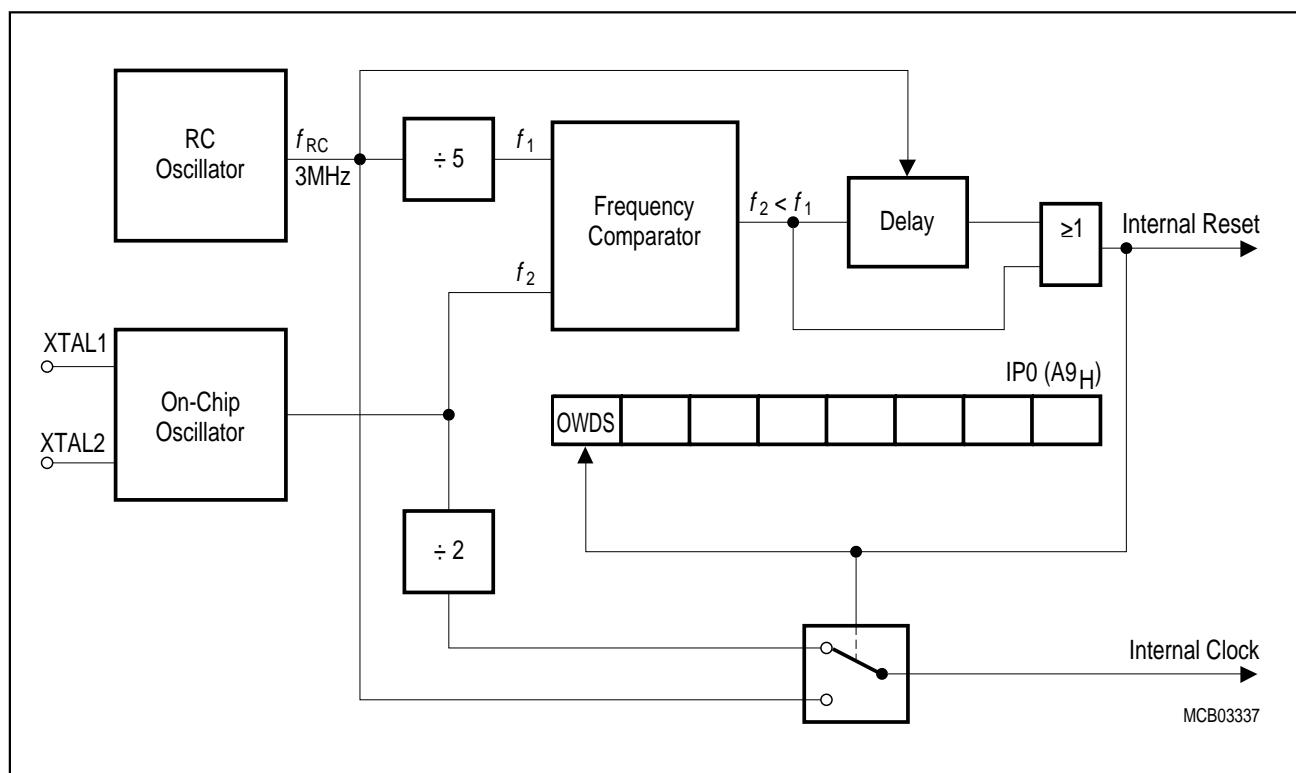


Figure 24
Block Diagram of the Oscillator Watchdog

Power Saving Modes

The C517A provides two basic power saving modes, the idle mode and the power down mode. Additionally, a slow down mode is available. This power saving mode reduces the internal clock rate in normal operating mode and it can be also used for further power reduction in idle mode.

- **Idle mode**

The CPU is gated off from the oscillator. All peripherals are still provided with the clock and are able to work. Idle mode is entered by software and can be left by an interrupt or reset.

- **Slow down mode**

The controller keeps up the full operating functionality, but its normal clock frequency is internally divided by 8. This slows down all parts of the controller, the CPU and all peripherals, to 1/8th of their normal operating frequency and also reduces power consumption.

- **Software power down mode**

The operation of the C517A is completely stopped and the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current. This power down mode is entered by software and can be left by reset or by a short low pulse at pin P3.2/INT0.

- **Hardware Power down mode**

If pin HWPD gets active (low level) the part enters the hardware power down mode and starts a complete internal reset sequence. Thereafter, both oscillators of the chip are stopped and the port pins and several control lines enter a floating state.

In the power down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the power down mode is invoked, and that V_{CC} is restored to its normal operating level, before the power down mode is terminated. **Table 13** gives a general overview of the entry and exit procedures of the power saving modes.

Table 13
Power Saving Modes Overview

Mode	Entering 2-Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H ORL PCON, #20H	Occurrence of an interrupt from a peripheral unit	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Slow Down Mode	In normal mode: ORL PCON,#10H	ANL PCON,#0EFH or Hardware Reset	Internal clock rate is reduced to 1/8 of its nominal frequency
	With idle mode: ORL PCON,#01H ORL PCON, #30H	Occurrence of an interrupt from a peripheral unit Hardware reset	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with 1/8 of its nominal frequency
Software Power Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillator is stopped; contents of on-chip RAM and SFR's are maintained;
		Short low pulse at pin P3.2/INT0	
Hardware Power Down Mode	HWPD = 0	HWPD = 1	Oscillator is stopped; internal reset is executed;

Absolute Maximum Ratings

Ambient temperature under bias (T_A)	– 40 to 125 °C
Storage temperature (T_{stg})	– 65 °C to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS})	– 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS})	– 0.5 V to V_{CC} +0.5 V
Input current on any pin during overload condition	– 10 mA to 10 mA
Absolute sum of all input currents during overload condition	100 mA
Power dissipation	TBD

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.*

DC Characteristics

$V_{CC} = 5 \text{ V} + 10\%, - 15\%$; $V_{SS} = 0 \text{ V}$	$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$	for the SAB-C517A
	$T_A = - 40 \text{ to } 85 \text{ }^\circ\text{C}$	for the SAF-C517A
	$T_A = - 40 \text{ to } 110 \text{ }^\circ\text{C}$	for the SAH-C517A

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage Pins except $\overline{\text{EA}}$, $\overline{\text{RESET}}$, $\overline{\text{HWPD}}$ $\overline{\text{EA}}$ pin $\overline{\text{HWPD}}$ and $\overline{\text{RESET}}$ pins	V_{IL}	- 0.5	$0.2 V_{CC} - 0.1$	V	-
	V_{IL1}	- 0.5	$0.2 V_{CC} - 0.3$	V	-
	V_{IL2}	- 0.5	$0.2 V_{CC} + 0.1$	V	-
Input high voltage pins except $\overline{\text{RESET}}$, XTAL2 and $\overline{\text{HWPD}}$ XTAL2 pin $\overline{\text{RESET}}$ and $\overline{\text{HWPD}}$ pin	V_{IH}				
	V_{IH1}	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V	-
	V_{IH2}	$0.7 V_{CC}$	$V_{CC} + 0.5$	V	-
Output low voltage Ports 1, 2, 3, 4, 5, 6 Port 0, ALE, $\overline{\text{PSEN}}$, $\overline{\text{RO}}$	V_{OL}	-	0.45	V	$I_{OL} = 1.6 \text{ mA}^1)$
	V_{OL1}	-	0.45	V	$I_{OL} = 3.2 \text{ mA}^1)$
Output high voltage Ports 1, 2, 3, 4, 5, 6 Port 0 in external bus mode, ALE, $\overline{\text{PSEN}}$, $\overline{\text{RO}}$	V_{OH}	2.4	-	V	$I_{OH} = - 80 \mu\text{A}$
	V_{OH1}	$0.9 V_{CC}$	-	V	$I_{OH} = - 10 \mu\text{A}$
	V_{OH2}	2.4	-	V	$I_{OH} = - 800 \mu\text{A}$
	V_{OH3}	$0.9 V_{CC}$	-	V	$I_{OH} = - 80 \mu\text{A}^2)$
Logic 0 input current Ports 1, 2, 3, 4, 5, 6	I_{LI}	- 10	- 70	μA	$V_{IN} = 0.45 \text{ V}$
Logical 0-to-1 transition current, Ports 1, 2, 3, 4, 5, 6	I_{TL}	- 65	- 650	μA	$V_{IN} = 2 \text{ V}$
Input leakage current Port 0, 7 and 8, $\overline{\text{EA}}$, $\overline{\text{HWPD}}$	I_{LI}	-	± 1	μA	$0.45 < V_{IN} < V_{CC}$
Input low current to $\overline{\text{RESET}}$ for reset XTAL2 $\overline{\text{PE/SWD}}$, OWE	I_{IL2}	- 10	- 100	μA	$V_{IN} = 0.45 \text{ V}$
	I_{IL3}	-	- 15	μA	$V_{IN} = 0.45 \text{ V}$
	I_{IL4}	-	- 20	μA	$V_{IN} = 0.45 \text{ V}$
Pin capacitance	C_{IO}	-	10	pF	$f_C = 1 \text{ MHz}$, $T_A = 25 \text{ }^\circ\text{C}$
Overload current	I_{OV}	-	± 5	mA	⁷⁾ ⁸⁾

Notes see next page

Power Supply Current

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ. ⁹⁾	max. ¹⁰⁾		
Active mode	18 MHz	I_{CC}	21.3	29.2	mA
	24 MHz	I_{CC}	27.3	37.6	mA
Idle mode	18 MHz	I_{CC}	11.6	16.2	mA
	24 MHz	I_{CC}	14.6	20.4	mA
Active mode with slow-down enabled	18 MHz	I_{CC}	9.5	13.1	mA
	24 MHz	I_{CC}	10.7	14.9	mA
Power-down mode		I_{PD}	15	50	μA
					$V_{CC} = 2 \dots 5.5 \text{ V}^3)$

Notes:

- 1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.
- 2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.
- 3) I_{PD} (power-down mode) is measured under following conditions:
 $EA = \overline{RESET} = \text{Port 0} = \text{Port 7} = \text{Port 8} = V_{CC}$; $XTAL1 = \text{N.C.}$; $XTAL2 = V_{SS}$; $\overline{PE}/\text{SWD} = \text{OWE} = V_{SS}$;
 $HWPD = V_{CC}$ for software power-down mode; $V_{AGND} = V_{SS}$; $V_{AREF} = V_{CC}$; all other pins are disconnected.
 I_{PD} (hardware power-down mode) is independent of any particular pin connection.
- 4) I_{CC} (active mode) is measured with:
 $XTAL2$ driven with t_{CLCH} , $t_{CHCL} = 5 \text{ ns}$, $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; $XTAL1 = \text{N.C.}$;
 $EA = \overline{PE}/\text{SWD} = V_{SS}$; $\text{Port 0} = \text{Port 7} = \text{Port 8} = V_{CC}$; $HWPD = V_{CC}$; $\overline{RESET} = V_{CC}$; all other pins are disconnected.
- 5) I_{CC} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
 $XTAL2$ driven with t_{CLCH} , $t_{CHCL} = 5 \text{ ns}$, $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; $XTAL1 = \text{N.C.}$;
 $\overline{RESET} = V_{CC}$; $HWPD = \text{Port 0} = \text{Port 7} = \text{Port 8} = V_{CC}$; $EA = \overline{PE}/\text{SWD} = V_{SS}$;
all other pins are disconnected;
- 6) I_{CC} (active mode with slow-down mode) is measured with all output pins disconnected and with all peripherals disabled; $XTAL2$ driven with t_{CLCH} , $t_{CHCL} = 5 \text{ ns}$, $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; $XTAL1 = \text{N.C.}$;
 $HWPD = V_{CC}$; $RESET = V_{CC}$; $\text{Port 7} = \text{Port 8} = V_{CC}$; $EA = \overline{PE}/\text{SWD} = V_{SS}$; all other pins are disconnected.
- 7) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{CC} + 0.5 \text{ V}$ or $V_{OV} < V_{SS} - 0.5 \text{ V}$). The supply voltage V_{CC} and V_{SS} must remain within the specified limits. The absolute sum of input currents on all port pins may not exceed 50 mA.
- 8) Not 100% tested, guaranteed by design characterization
- 9) The typical I_{CC} values are periodically measured at $T_A = +25 \text{ }^\circ\text{C}$ and $V_{CC} = 5 \text{ V}$ but not 100% tested.
- 10) The maximum I_{CC} values are measured under worst case conditions ($T_A = 0 \text{ }^\circ\text{C}$ or $-40 \text{ }^\circ\text{C}$ and $V_{CC} = 5.5 \text{ V}$)

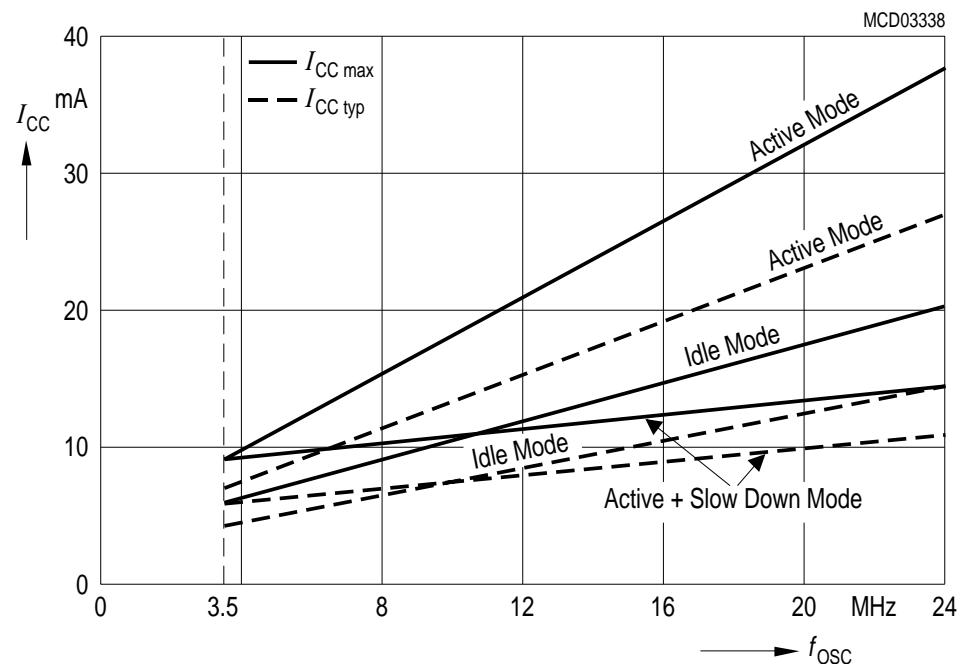


Figure 25
ICC Diagram

Table 14
Power Supply Current Calculation Formulas

Parameter	Symbol	Formula
Active mode	$I_{CC \text{ typ}}$	$1 * f_{OSC} + 3.3$
	$I_{CC \text{ max}}$	$1.4 * f_{OSC} + 4.0$
Idle mode	$I_{CC \text{ typ}}$	$0.5 * f_{OSC} + 2.6$
	$I_{CC \text{ max}}$	$0.7 * f_{OSC} + 3.6$
Active mode with slow-down enabled	$I_{CC \text{ typ}}$	$0.25 * f_{OSC} + 4.95$
	$I_{CC \text{ max}}$	$0.3 * f_{OSC} + 7.7$

Note: f_{osc} is the oscillator frequency in MHz. I_{CC} values are given in mA.

A/D Converter Characteristics

$V_{CC} = 5 \text{ V} + 10\%, - 15\%; V_{SS} = 0 \text{ V}$	$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$	for the SAB-C517A
	$T_A = - 40 \text{ to } 85 \text{ }^\circ\text{C}$	for the SAF-C517A
	$T_A = - 40 \text{ to } 110 \text{ }^\circ\text{C}$	for the SAH-C517A

$$4 \text{ V} \leq V_{AREF} \leq V_{CC} + 0.1 \text{ V}; V_{SS} - 0.1 \text{ V} \leq V_{AGND} \leq V_{SS} + 0.2 \text{ V}$$

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	¹⁾
Sample time	t_S	—	$16 \times t_{IN}$ $8 \times t_{IN}$	ns	Prescaler $\div 8$ Prescaler $\div 4$ ²⁾
Conversion cycle time	t_{ADCC}	—	$96 \times t_{IN}$ $48 \times t_{IN}$	ns	Prescaler $\div 8$ Prescaler $\div 4$ ³⁾
Total unadjusted error	T_{UE}	—	± 2	LSB	$V_{SS} + 0.5 \text{ V} \leq V_{IN} \leq V_{CC} - 0.5 \text{ V}$ ⁴⁾
Internal resistance of reference voltage source	R_{AREF}	—	$t_{ADC} / 250$ - 0.25	k Ω	t_{ADC} in [ns] ^{5) 6)}
Internal resistance of analog source	R_{ASRC}	—	$t_S / 500$ - 0.25	k Ω	t_S in [ns] ^{2) 6)}
ADC input capacitance	C_{AIN}	—	50	pF	⁶⁾

Notes see next page.

Clock calculation table:

Clock Prescaler Ratio	ADCL	t_{ADC}	t_S	t_{ADCC}
$\div 8$	1	$8 \times t_{IN}$	$16 \times t_{IN}$	$96 \times t_{IN}$
$\div 4$	0	$4 \times t_{IN}$	$8 \times t_{IN}$	$48 \times t_{IN}$

Further timing conditions: $t_{ADC} \text{ min} = 500 \text{ ns}$
 $t_{IN} = 2 / f_{OSC} = 2 t_{CLCL}$

Notes:

- 1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.
- 2) During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S . After the end of the sample time t_S , changes of the analog input voltage have no effect on the conversion result.
- 3) This parameter includes the sample time t_S , the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.
- 4) T_{UE} is tested at $V_{AREF} = 5.0$ V, $V_{AGND} = 0$ V, $V_{CC} = 4.9$ V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.
- 5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.
- 6) Not 100% tested, but guaranteed by design characterization.

AC Characteristics (18 MHz)

$V_{CC} = 5 \text{ V} + 10\%, - 15\%; V_{SS} = 0 \text{ V}$	$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$	for the SAB-C517A
	$T_A = - 40 \text{ to } 85 \text{ }^\circ\text{C}$	for the SAF-C517A
	$T_A = - 40 \text{ to } 110 \text{ }^\circ\text{C}$	for the SAH-C517A

(C_L for port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit	
		18 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 18 \text{ MHz}$			
		min.	max.	min.	max.		
ALE pulse width	t_{LHLL}	71	—	$2 t_{CLCL} - 40$	—	ns	
Address setup to ALE	t_{AVLL}	26	—	$t_{CLCL} - 30$	—	ns	
Address hold after ALE	t_{LLAX}	26	—	$t_{CLCL} - 30$	—	ns	
ALE low to valid instruction in	t_{LLIV}	—	122	—	$4 t_{CLCL} - 100$	ns	
ALE to PSEN	t_{LLPL}	31	—	$t_{CLCL} - 25$	—	ns	
PSEN pulse width	t_{PLPH}	132	—	$3 t_{CLCL} - 35$	—	ns	
PSEN to valid instruction in	t_{PLIV}	—	92	—	$3 t_{CLCL} - 75$	ns	
Input instruction hold after PSEN	t_{PXIX}	0	—	0	—	ns	
Input instruction float after PSEN	$t_{PXIZ}^*)$	—	46	—	$t_{CLCL} - 10$	ns	
Address valid after PSEN	$t_{PXAV}^*)$	48	—	$t_{CLCL} - 8$	—	ns	
Address to valid instr in	t_{AVIV}	—	180	—	$5 t_{CLCL} - 98$	ns	
Address float to PSEN	t_{AZPL}	0	—	0	—	ns	

^{*)} Interfacing the C517A to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (18 MHz, cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit	
		18 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 18 \text{ MHz}$			
		min.	max.	min.	max.		
RD pulse width	t_{RLRH}	233	—	$6 t_{CLCL} - 100$	—	ns	
WR pulse width	t_{WLWH}	233	—	$6 t_{CLCL} - 100$	—	ns	
Address hold after ALE	t_{LLAX2}	81	—	$2 t_{CLCL} - 30$	—	ns	
RD to valid data in	t_{RLDV}	—	128	—	$5 t_{CLCL} - 150$	ns	
Data hold after RD	t_{RHDX}	0	—	0	—	ns	
Data float after RD	t_{RHDZ}	—	51	—	$2 t_{CLCL} - 60$	ns	
ALE to valid data in	t_{LLDV}	—	294	—	$8 t_{CLCL} - 150$	ns	
Address to valid data in	t_{AVDV}	—	335	—	$9 t_{CLCL} - 165$	ns	
ALE to WR or RD	t_{LLWL}	117	217	$3 t_{CLCL} - 50$	$3 t_{CLCL} + 50$	ns	
Address valid to WR or RD	t_{AVWL}	92	—	$4 t_{CLCL} - 130$	—	ns	
WR or RD high to ALE high	t_{WHLH}	16	96	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns	
Data valid to WR transition	t_{QVWX}	11	—	$t_{CLCL} - 45$	—	ns	
Data setup before WR	t_{QVWH}	239	—	$7 t_{CLCL} - 150$	—	ns	
Data hold after WR	t_{WHQX}	16	—	$t_{CLCL} - 40$	—	ns	
Address float after RD	t_{RLAZ}	—	0	—	0	ns	

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit	
		Variable Clock Freq. = 3.5 MHz to 18 MHz			
		min.	max.		
Oscillator period	t_{CLCL}	55.6	285.7	ns	
High time	t_{CHCX}	15	$t_{CLCL} - t_{CLCX}$	ns	
Low time	t_{CLCX}	15	$t_{CLCL} - t_{CHCX}$	ns	
Rise time	t_{CLCH}	—	15	ns	
Fall time	t_{CHCL}	—	15	ns	

AC Characteristics (24 MHz)

$V_{CC} = 5 \text{ V} + 10\%, - 15\%; V_{SS} = 0 \text{ V}$	$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$	for the SAB-C517A
	$T_A = - 40 \text{ to } 85 \text{ }^\circ\text{C}$	for the SAF-C517A
	$T_A = - 40 \text{ to } 110 \text{ }^\circ\text{C}$	for the SAH-C517A

(C_L for port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit	
		24 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 24 \text{ MHz}$			
		min.	max.	min.	max.		
ALE pulse width	t_{LHLL}	43	—	$2 t_{CLCL} - 40$	—	ns	
Address setup to ALE	t_{AVLL}	17	—	$t_{CLCL} - 25$	—	ns	
Address hold after ALE	t_{LLAX}	17	—	$t_{CLCL} - 25$	—	ns	
ALE low to valid instruction in	t_{LLIV}	—	80	—	$4 t_{CLCL} - 87$	ns	
ALE to PSEN	t_{LLPL}	22	—	$t_{CLCL} - 20$	—	ns	
PSEN pulse width	t_{PLPH}	95	—	$3t_{CLCL} - 30$	—	ns	
PSEN to valid instruction in	t_{PLIV}	—	60	—	$3 t_{CLCL} - 65$	ns	
Input instruction hold after PSEN	t_{PXIX}	0	—	0	—	ns	
Input instruction float after PSEN	$t_{PXIZ}^*)$	—	32	—	$t_{CLCL} - 10$	ns	
Address valid after PSEN	$t_{PXAV}^*)$	37	—	$t_{CLCL} - 5$	—	ns	
Address to valid instr in	t_{AVIV}	—	148	—	$5 t_{CLCL} - 60$	ns	
Address float to PSEN	t_{AZPL}	0	—	0	—	ns	

^{*)} Interfacing the C517A to devices with float times up to 37 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (24 MHz, cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit	
		24 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 24 \text{ MHz}$			
		min.	max.	min.	max.		
RD pulse width	t_{RLRH}	180	—	$6 t_{CLCL} - 70$	—	ns	
WR pulse width	t_{WLWH}	180	—	$6 t_{CLCL} - 70$	—	ns	
Address hold after ALE	t_{LLAX2}	53	—	$2 t_{CLCL} - 30$	—	ns	
RD to valid data in	t_{RLDV}	—	118	—	$5 t_{CLCL} - 90$	ns	
Data hold after RD	t_{RHDX}	0	—	0	—	ns	
Data float after RD	t_{RHDZ}	—	63	—	$2 t_{CLCL} - 20$	ns	
ALE to valid data in	t_{LLDV}	—	200	—	$8 t_{CLCL} - 133$	ns	
Address to valid data in	t_{AVDV}	—	220	—	$9 t_{CLCL} - 155$	ns	
ALE to WR or RD	t_{LLWL}	75	175	$3 t_{CLCL} - 50$	$3 t_{CLCL} + 50$	ns	
Address valid to WR or RD	t_{AVWL}	67	—	$4 t_{CLCL} - 97$	—	ns	
WR or RD high to ALE high	t_{WHLH}	17	67	$t_{CLCL} - 25$	$t_{CLCL} + 25$	ns	
Data valid to WR transition	t_{QVWX}	5	—	$t_{CLCL} - 37$	—	ns	
Data setup before WR	t_{QVWH}	170	—	$7 t_{CLCL} - 122$	—	ns	
Data hold after WR	t_{WHQX}	15	—	$t_{CLCL} - 27$	—	ns	
Address float after RD	t_{RLAZ}	—	0	—	0	ns	

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit	
		Variable Clock Freq. = 3.5 MHz to 24 MHz			
		min.	max.		
Oscillator period	t_{CLCL}	41.7	285.7	ns	
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns	
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns	
Rise time	t_{CLCH}	—	12	ns	
Fall time	t_{CHCL}	—	12	ns	

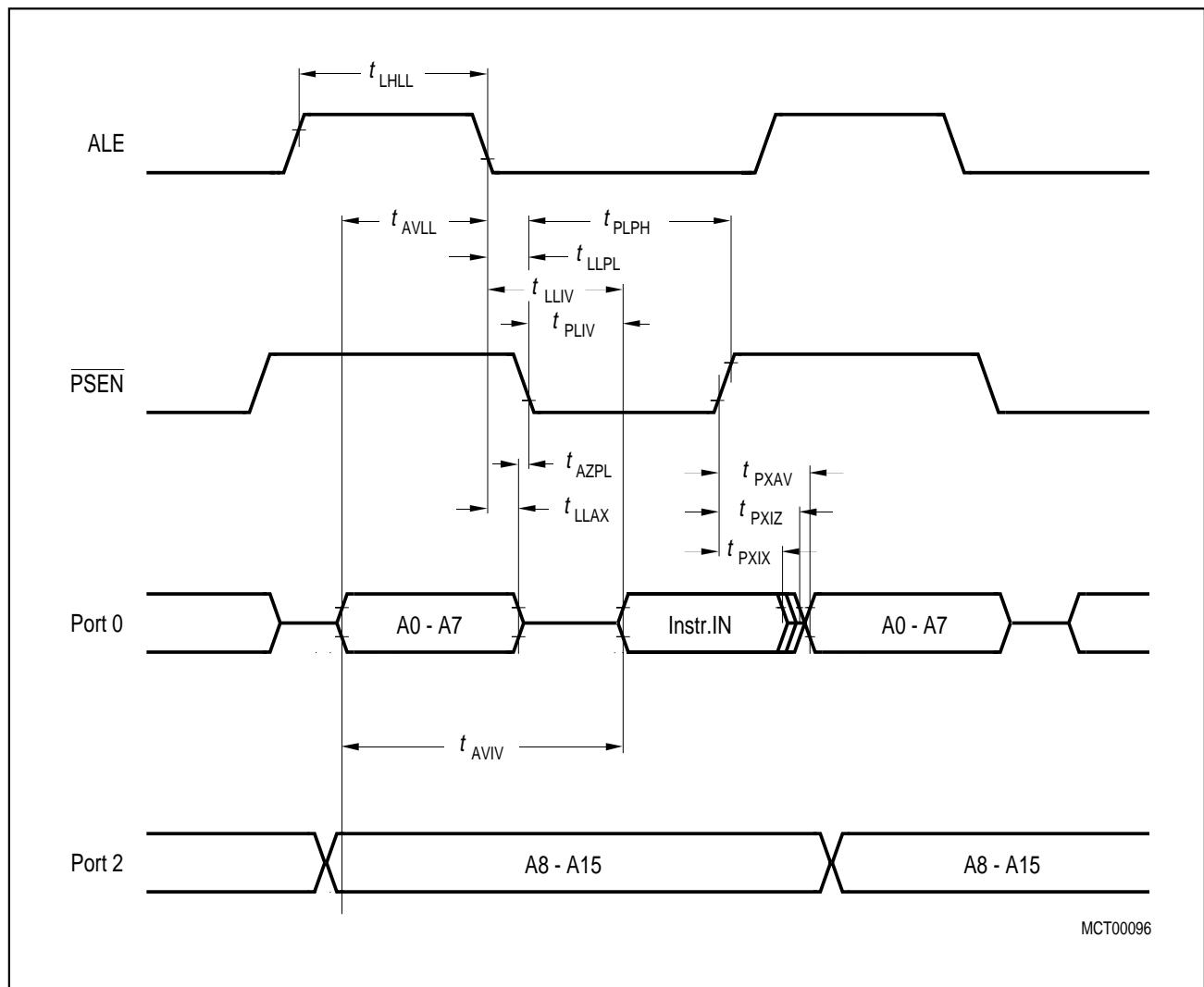


Figure 26
Program Memory Read Cycle

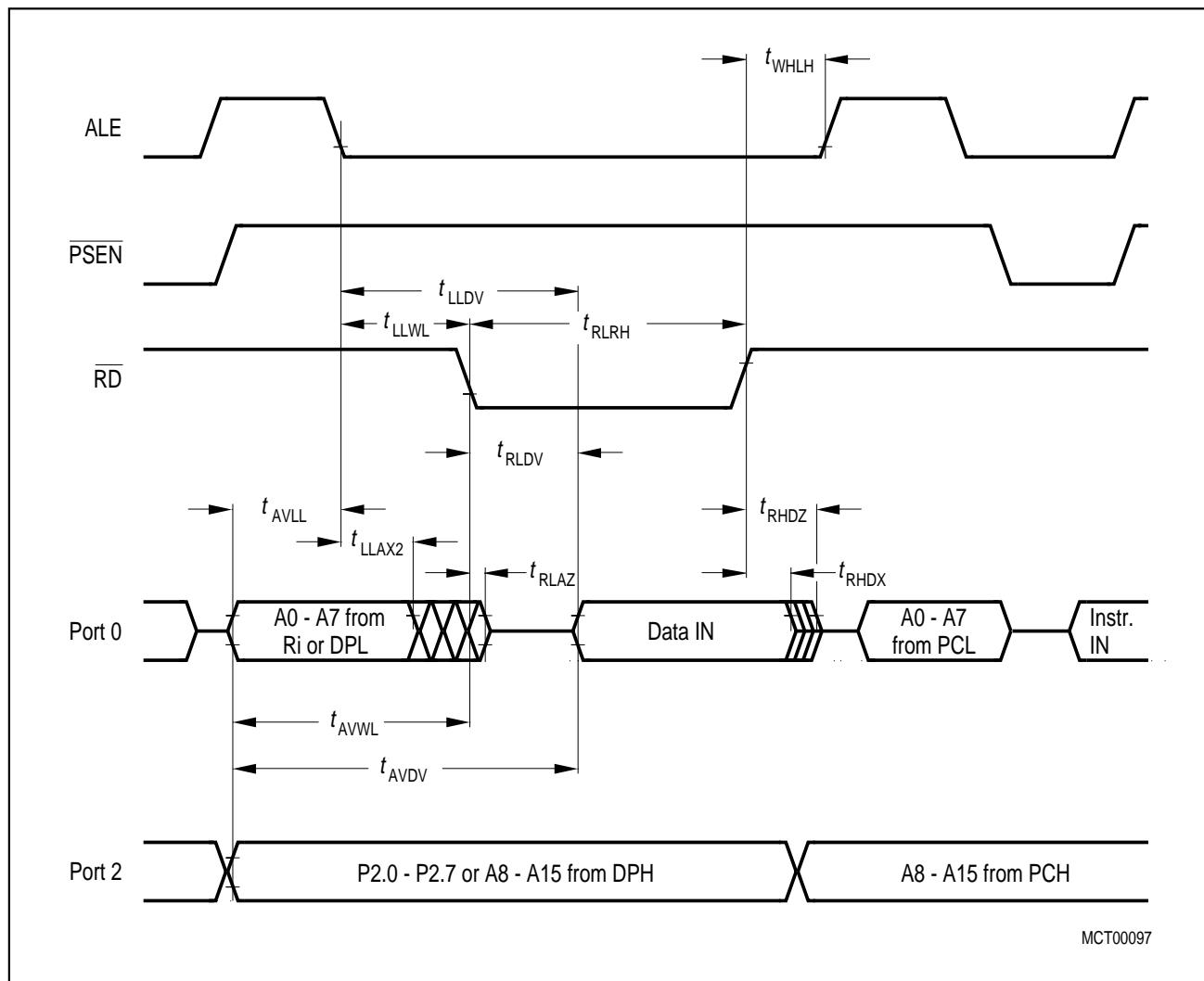


Figure 27
Data Memory Read Cycle

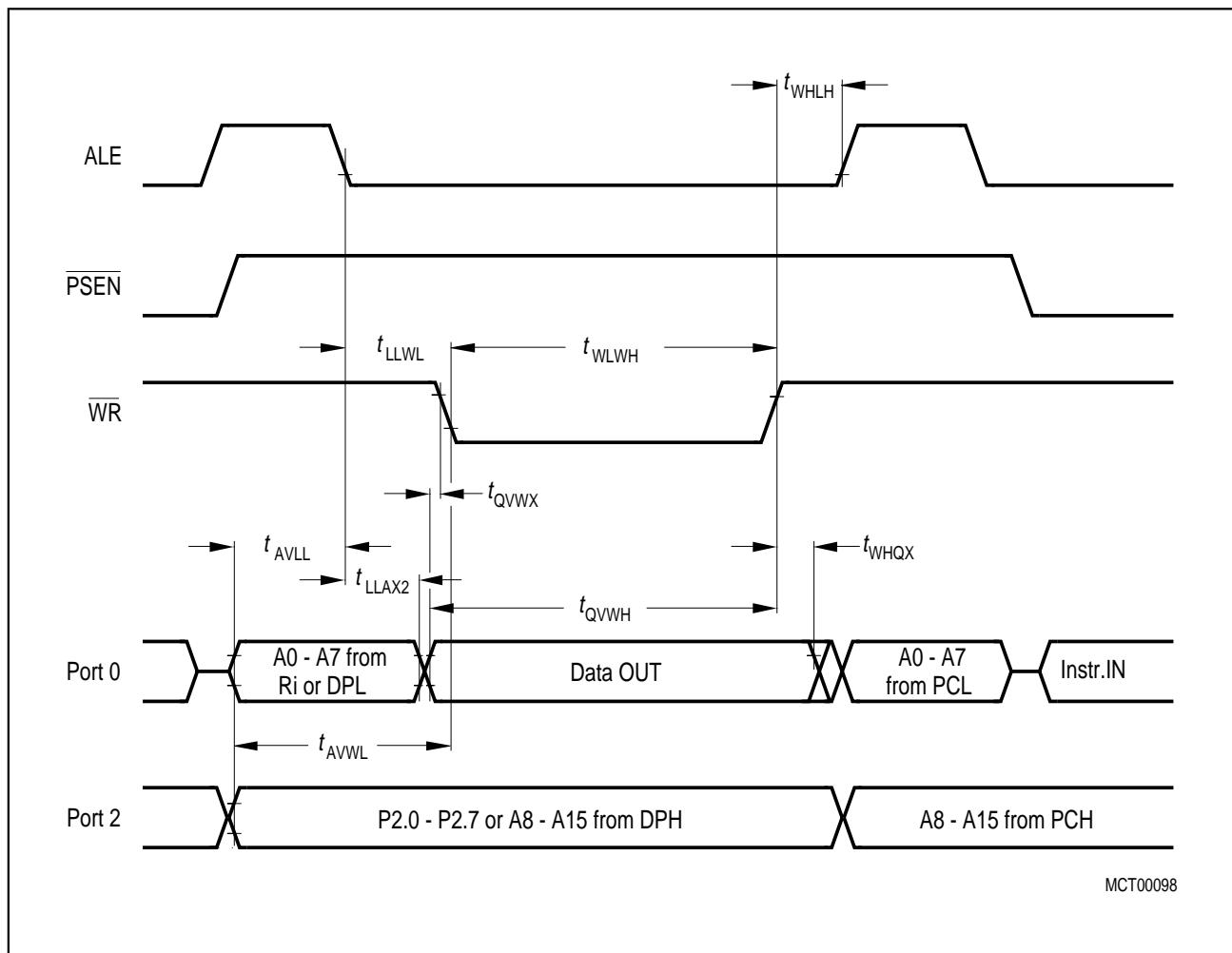


Figure 28
Data Memory Write Cycle

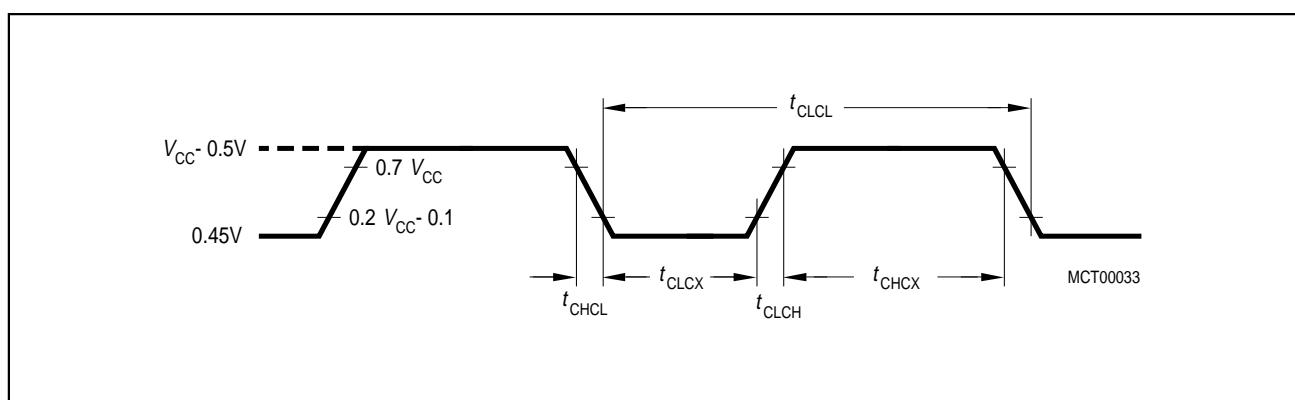


Figure 29
External Clock Drive on XTAL2

ROM Verification Characteristics for the C517A-1RM**ROM Verification Mode 1**

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	—	10 t_{CLCL}	ns

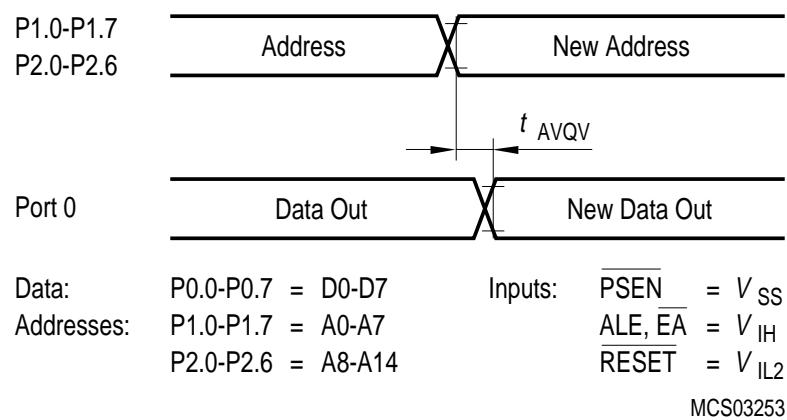


Figure 30
ROM Verification Mode 1

ROM Verification Mode 2

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	t_{AWD}	—	$2 t_{CLCL}$	—	ns
ALE period	t_{ACY}	—	$12 t_{CLCL}$	—	ns
Data valid after ALE	t_{DVA}	—	—	$4 t_{CLCL}$	ns
Data stable after ALE	t_{DSA}	$8 t_{CLCL}$	—	—	ns
P3.5 setup to ALE low	t_{AS}	—	t_{CLCL}	—	ns
Oscillator frequency	$1/ t_{CLCL}$	3.5	—	24	MHz

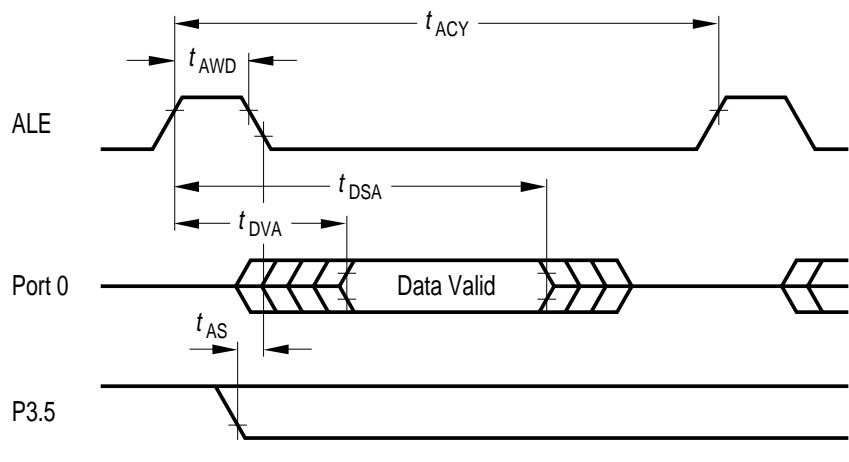
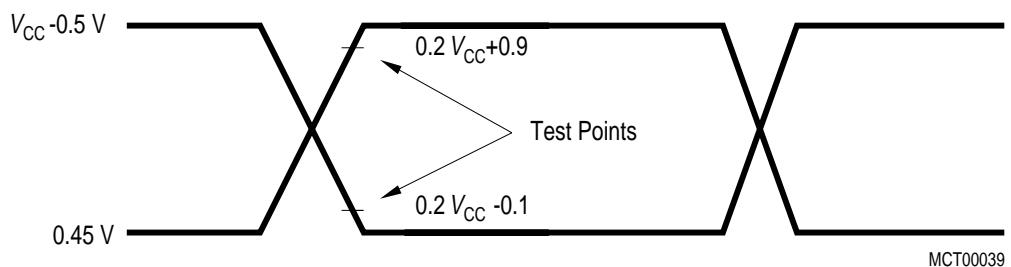
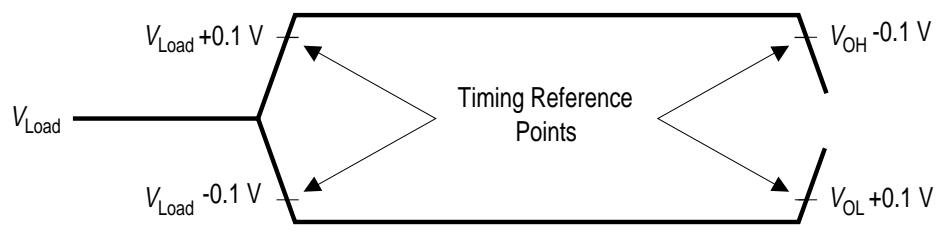


Figure 31
ROM Verification Mode 2



AC Inputs during testing are driven at $V_{CC} - 0.5$ V for a logic '1' and 0.45 V for a logic '0'.
 Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 32
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.
 $I_{OL}/I_{OH} \geq \pm 20$ mA

Figure 33
AC Testing: Float Waveforms

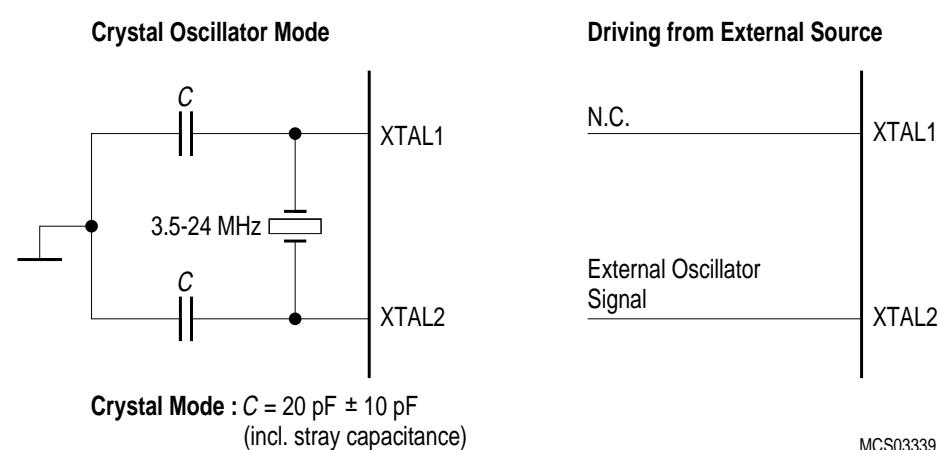
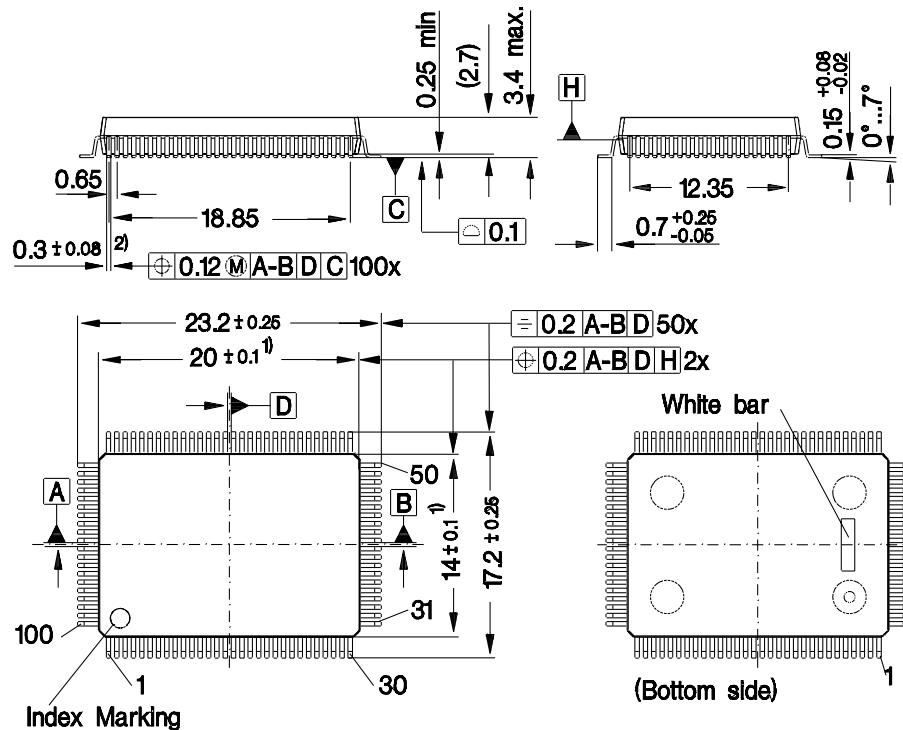


Figure 34
Recommended Oscillator Circuits for Crystal Oscillator

Plastic Package, P-MQFP-100-2 (SMD)
 (Plastic Metric Quad Flat Package)



GPM05623

Figure 35
P-MQFP-100-2 Package Outlines

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our
 Data Book "Package Information"

SMD = Surface Mounted Device

Dimensions in mm